25MA

The Multinational Power Electronics Association

PSMA

Packaging/Manufacturing Committee

April 16th, 2024

John Bultitude, Brian Narveson, Jason Rouse

Co-chairman



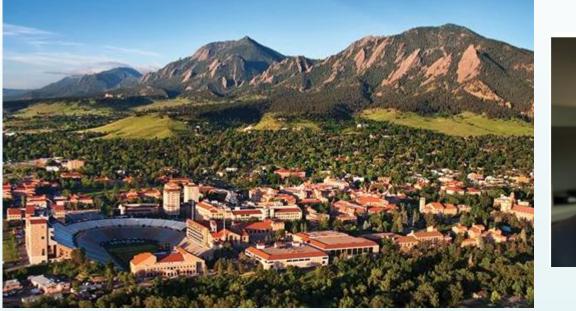
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1985-2020

- 3D-PEIM 2025 Update
 - 3D-PEIM Organizing Committee Update
 - 3D-PEIM Technical Committee Update
- IWIPP 2025 Update
- Pwr Soc 2025 Update
- Power Technology Report on Embedded and Integrated Magnetics- Update
- APEC 2024 Industry Session Summary
- APEC 2025
 - Focus Topic Brainstorm for Packaging and Manufacturing



3D-PEIM 2025



3D-PEIM is held every 2 years to bring together technologists interested in merging of power packaging, circuits, components and manufacturing to create high performance power solutions using 3D packaging technology and manufacturing techniques.

3D-PEIM

- Dr. Faisal Khan Chief Researcher/Scientist NREL General Chairman
- July 8-10, 2025 Sheraton West Denver
- In-person Conference
- Connect with world's top Power Packaging and Manufacturing experts
- PSMA sole Financial Sponsor, IEEE EPS Technical Sponsor



3D-PEIM 2025 Technical Co-chairs Chairs

Sreekant Narumanchi, Ph.D.,

ASME Fellow Group Manager, Advanced Power Electronics and Electric Machines Group Center for Integrated Mobility Sciences National Renewable Energy Laboratory, MS 1633

Email: sreekant.narumanchi@nrel.gov

Jason Rouse Ph.D., Manager Strategic Growth & Ventures Taiyo America Inc.

Email: jhrouse@taiyo-america.com

• Currently we are Recruiting for the Technical Committee to help Organize the Program



IWIPP 2025

- IWIPP International Workshop on Integrated Power Packaging is a biennial IEEE event dedicated to advancing the state of the art in power semiconductor packaging, which is widely recognized as one of the critical factors influencing the performance and reliability of today's power electronics
- IWIPP April 8-10, 2025
- Dr. Andy Lemon General Chairman
- In-person Conference



- University of Alabama, Tuscaloosa, Alabama
- Connect with world's top power, device, integrations and system researchers
- PSMA Board Approved Sponsorship at January 2024 Meeting





IWIPP is Sponsored By:





PwrSoC 2025

- The Packaging Committee supports PwrSoC
- Steering Committee approved a proposal from Prof. Jaeha Kim, Seoul National University.
- Exact Date TBD Sept/Oct 2025



Sponsors







Power Technology Report on Embedded and Integrated Magnetics

- \circ Purpose
 - To provide and up to date reference for member companies on the present state of integrated and embedded magnetics.
 - The report will follow the format of the previous 3 Technology Reports
 - The report will deep dive into the explosion of integrated and embedded PCB magnetics
 - The report would look at
 - What's available today and the applications they are used in.
 - What is in the pipeline for the next 2-3 years.
 - Potential roadmap for the future.
 - What the main roadblocks are.
- Supported by the Packaging and Magnetics Committee
 - Brian Narveson Subcommittee Chair Pkg Committee Co-Chair
 - John Bultitude Yageo Pkg Committee Co-chair
 - Cian O Manthuna –Tyndall Pkg Committee
 - Matt Wilkowski ENA Chip Pkg and Magnetics Committee
 - George Salma Wurth Magnetics Committee
 - Justin Henspeter IBM Packaging Committee
 - Dr. PM Raj Florida International University Packaging Committee
- RFP Reviewed and Complete will be sent out this week.
- Target Publication APEC 2025
- Estimated Cost \$125K-\$150K



APEC 2024 Industry Session - Wednesday February 28

Presentation attendees in range 30-80

IS10 Advances in 3D-Packaging Technology for Power Electronics

Focus:

The PSMA Packaging Committee is organizing and proposing an Industry Session for APEC 2024 that is focused on advances in 3D-Packaging

- Technology for power e such as embedding, wh
- APEC 2024 was well attended range of different applic

eve high packaging densities, packaging needs for a broad er power systems. Application demands for higher density,

of AI higher power syste more efficient power electronics will be described. The latest developments in onshoring of packaging will also be presented. This session will bring together leading academic and industrial researchers in this area. Attendance in RED

Start	Finish	ID	Presentation Title	Presenter	Title/Affiliation
8:30 AM	8:55 AM	IS 10.1	Common Mode Noise and Minimizing Emissions through	Douglas C. Hopkins	Professor in Electrical and Computer Engineering, Director of the
			Packaging Technology 32		Laboratory for Packaging Research in Electronic Energy Systems (PREES), NC State, USA
8:55 AM	9:20 AM	IS 10.2	Packaging for IoT Device Energy Harvesting Solutions – Roadmap	Mike Hayes /	Head of Group ICT for Energy Efficiency, Tyndall National
			and Considerations 31	Brian Zahnstecher	Institute, County Cork, Ireland
					/ Founder & Principal, PowerRox, Niantic, CT, USA
9:20 AM	9:45 AM	IS 10.3	Efficiency improvements for power conversion units by means of	Thomas Gottwald	Vice President Technology Schweizer Electronic AG, Germany
			PCB embedding technology for fast switching devices like SiC and		
			GaN 80		
9:45 AM	10:10 AM	IS 10.4	Innovation and Collaboration in Power Module Packaging and	Thomas Wang	Director of ASE Corporate R&D, ASE, Taiwan
			HVM in the fast-changing world 48		
10:10 AM	10:40AM		BRE	AK	
10:40 AM	11:05 AM	IS 10.5	On-Shoring Power Packaging	Charles Woychik	EHanced Semiconductor, Inc. formerly Sr. Director Advanced
			32		Packaging Platforms at Skywater Technology Foundry, Kissimmee, Florida, USA
11:05 AM	11:30 AM	IS 10.6	Chiplets and Integration in Power Distribution Networks 18	Siddarth	Chipletz, Austin, TX, USA
11.20.414		10 40 7		Ravichandran	Drofessor and Director of Undergraduate Studies
11:30 AM	11:55 AM	15 10.7	AI-Driven Reliability of Solar Power Inverters	Patrick McCluskey	Professor and Director of Undergraduate Studies
			25?		Dept. of Mechanical Engineering
					University of Maryland, College Park, MD USA

APEC 2025 Topic Brainstorm

- At our last meeting we discussed high level topics that would improve attendance at our APEC Session. The following were discussed but need to be refined or added to.
 - Speaker from DARPA to present industry challenges
 - System house to discuss power packaging challenges
 - Packaging alternatives for AI processors or processor boards
 - SiC & GaN Power Packaging
 - Cooling AI power
 - Packaging of power solution for AI requiring 1000A art 1V.



Thank You

Next Committee Meeting Tuesday May 14, 9am Central Time



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- Comparison of Packages
- Efficiency at High Frequency
- Cost Effectiveness
- Electromagnetic Simulations
- Multiphysics Modeling, Design & Packaging
- Advanced Design for Assembly Digital Twin Tools
- Electronic Design Automation
- Design Validation Techniques
- Physical Changes, Temperature 3D Failure Mechanisms and how to avoid them
- Lower Cost materials & Manufacturing processes
- Higher temperatures 175 to 200°C
- Process Time and Cost Down
- Thermal compounds



- Double sided cooling
- HALT testing Auto Reliability
- Cost Effective Modeling
- System Architecture higher end phase redundancy
- Multi-chip processors multi voltages
- Power converters onto processors
 - Control each chip
 - Lower system cost
 - Improved Reliability
 - Magnetics buck regulation
- Integration high current high frequency GPUs
- Power Supply on chip
- Larger Scale Vehicle electrification
- Address problems at many levels chips/module/system how does this differ?



- Panel level packaging of GaN
 - Large Area & volume assembly
 - Optical System Inspection
 - Organic Vs. Glass substrates
- AI models
 - Train the model
 - Reduce time-to-market
- Immersion Cooling
 - Realize higher power and currents
 - Al datacenters
- Convergence trends in Power Packaging Acadamia—Industry
- Power passives as part of tools/database integrated power problem the packaging community needs to own this
- Review ECTC agenda for presenters TSMC, Samsung, Intel, Vicor....



- Integration on chip innovations pushing the technology forward
- How to verify manufacturing process after each stage
- Implement AI for inspection
- Integrated Components
 - Figures of Merit (FOM)
 - Component Level or System Level
 - What is the true FOM for the system
 - What is being optimized
- Validated database of Multiphysics Models
- Multi chip Packaging (Including Power ?)
- Use of AI to anticipate power demand?
- How to get power sources to include in EDA tools?
- How to get power packaging innovations to market faster?
- What is the right power architecture for AI boards?

