FPGA Cost And Efficiency For PV Inverter Power Electronics

APEC 2013
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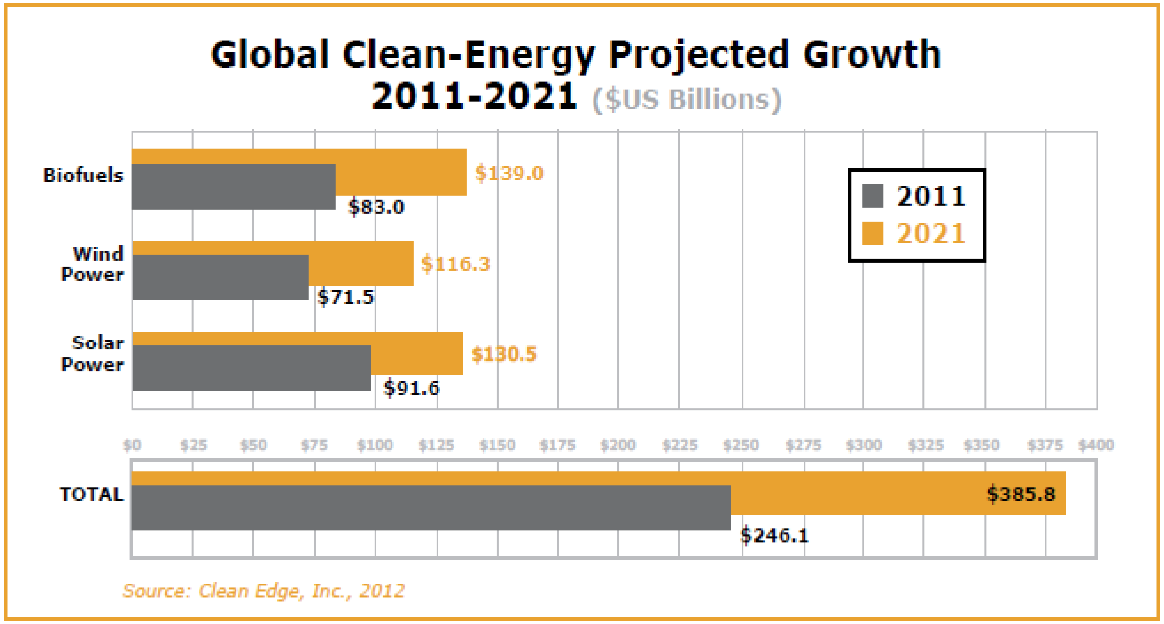
About The Speaker

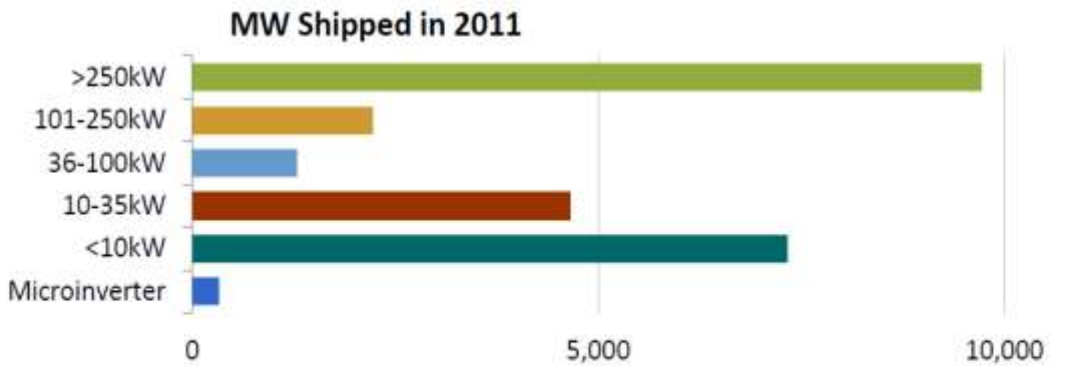
- Jason Chiang is a senior strategic marketing manager in Altera’s MIC Division-Industrial BU in San Jose, California
- Responsible for developing marketing strategies and FPGA solutions for Smart Grid and industrial automation applications
- Prior to rejoining Altera in 2008, Jason held various product marketing and business development roles at PMC-Sierra, P.A. Semi, Hitachi, and several other semiconductor companies
- Holds a BSEE from Cal Poly, San Luis Obispo

Solar Power In Grid Ecosystem



- Solar energy growing from $91.6 billion in 2011 to $130.5 billion by 2021
- Europe still leads market while growth in U.S. and Asia Pacific
- Driven by regional green energy mandates and feed-in-tariffs (FITs)

PV Inverter Preferences, By Type



Source: IMS Research's 2011 PV Inverter Report – Premium Edition

String – 46%

Central – 53%

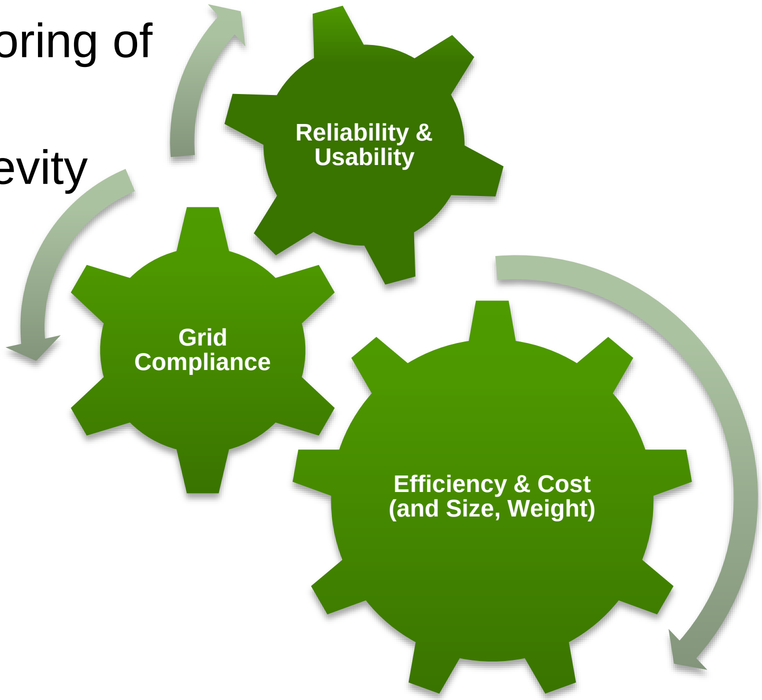
Microinverter– 1%

- Global PV inverters to grow from ~23 GW to over 42 GW by 2015, primarily in residential and commercial
- String inverters expected to dominate inverter types
- Microinverters/power optimizers may capture 15% (~6 GW) of residential by 2015

PV Inverter Emerging Trends

<u>Reliability & Usability</u>

- Fast user interfaces
- More diagnostic functions and communications
- Mobile monitoring of inverters
- Product longevity



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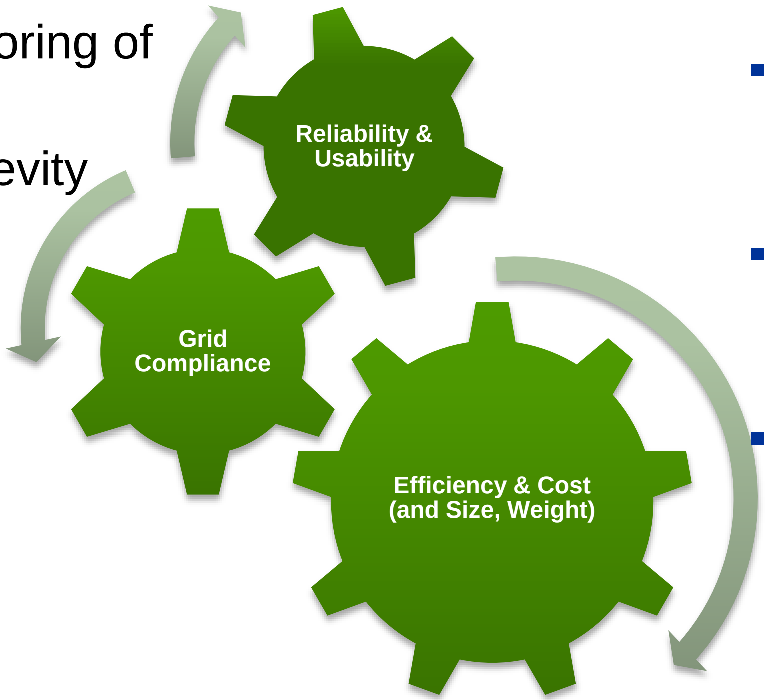

Lower Cost, Increased Efficiency

- Highly efficient multi-level IGBT and wideband gap power topologies
- Advanced digital control & advanced MPPT for efficiency
- Higher switching frequency to enable smaller passive components
- Achieve >20% cost reduction in next generation designs

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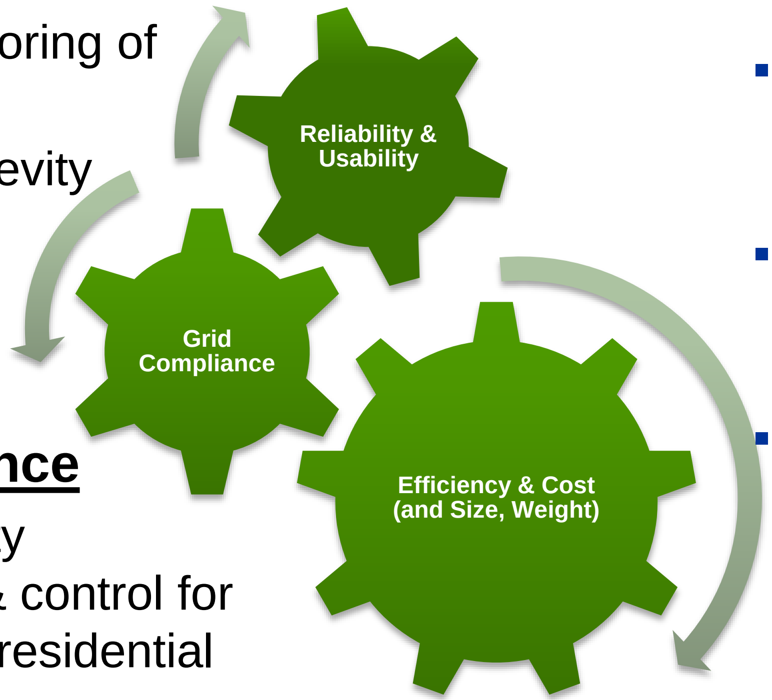

Grid Compliance

- Power quality monitoring & control for commercial/residential
- Grid code compliance for power generation

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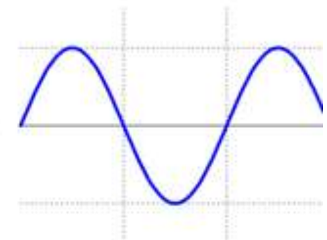
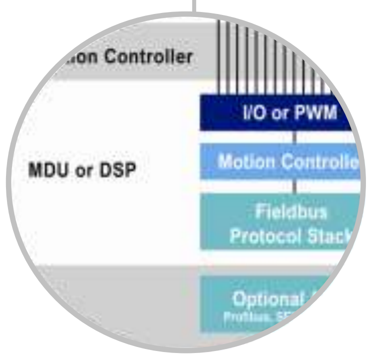
PV Inverter Design Challenges

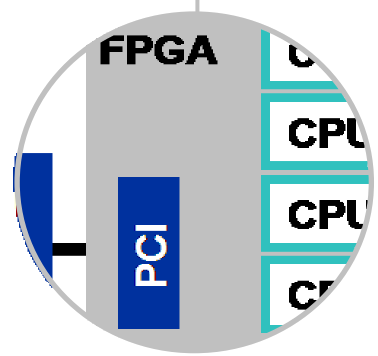
- **Switch Faster** — Scalable High Switching Frequency Design
- **Switch Better** — Modular Complex Topologies 3L/5L Control Loop
- **Switch Cheaper** — Reduce Cost in Passive & Heat Sinks *(using SiC/GaN)*



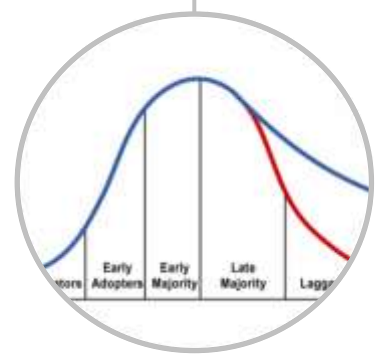
Efficiency
Reliability
Cost of Ownership



Design Flexibility
Platform Integration
Performance



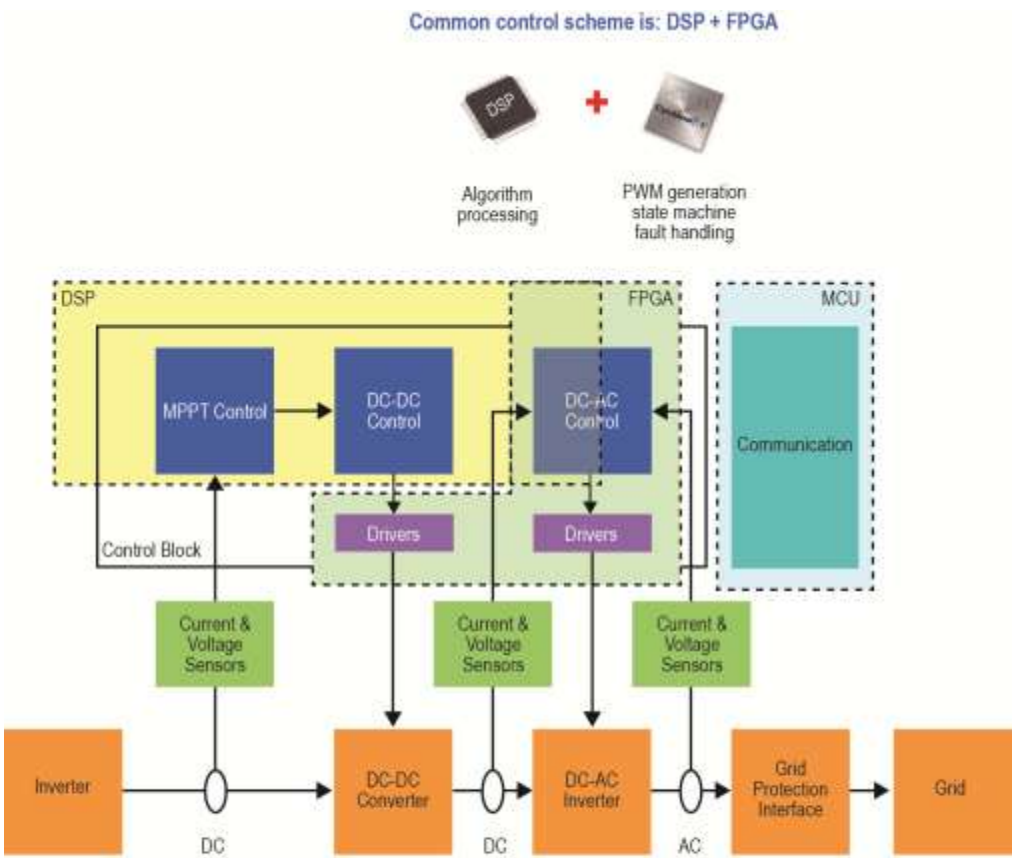
DSP Algorithms
Embedded Processing
Evolving Standards



Long Life Cycle

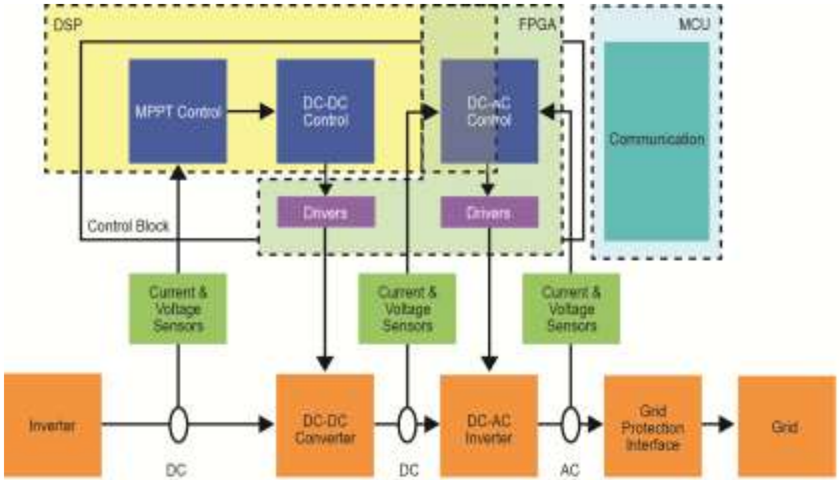
Realm of low-cost FPGAs

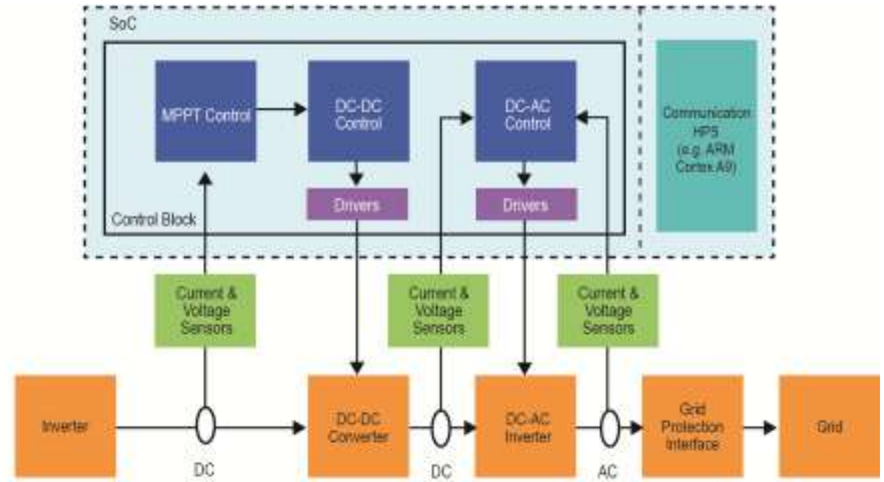
Typical PV Inverter Architecture



- Architectures vary by
  - Inverter power topology
  - Control loop complexity
- DSP for MPPT and DC-DC control
- MCU/DSP with (optional) FPGA for DC-AC control
- MCU/DSP architectures running out of bandwidth for next generation designs

FPGA For Platform Scalability





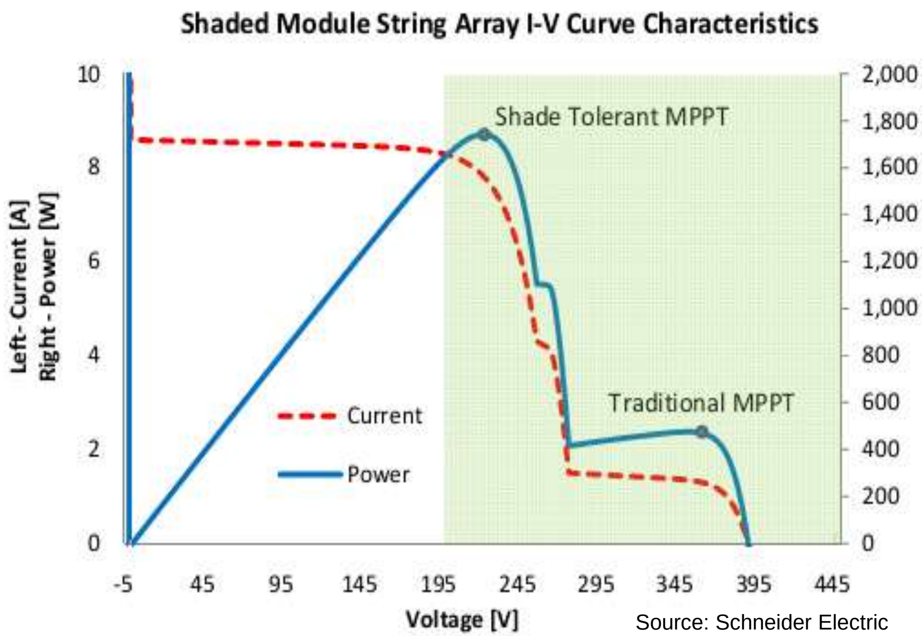
<u>Coprocessor/DSP Offload</u>

- Reuse hardware/software
- Offload to FPGA to speed up complex control loops
- Integrate and scale PWM channels, I/Os, glue logic

<u>System-on-Chip (SoC)</u>

- SoC integration of control loops, PWMs, I/Os, communications,…
- Embedded processing for real-time & apps. control
- Fewer components for reliability, lower cost

Switch Better – FPGA For DC-DC Control



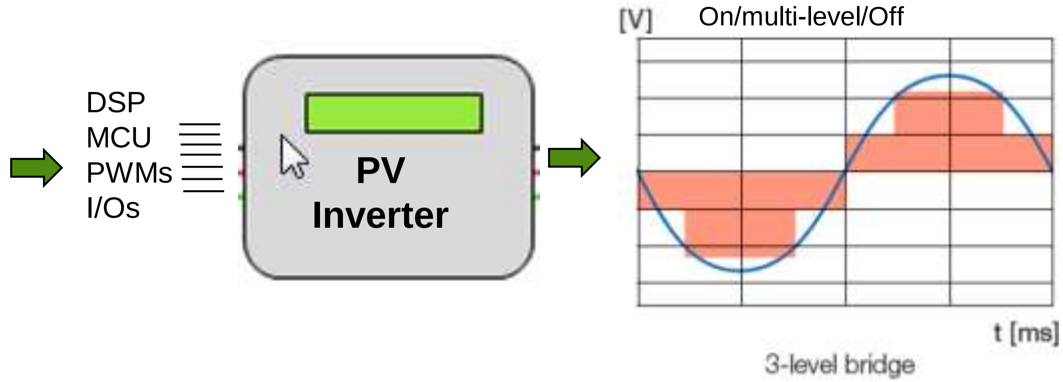
Source: Schneider Electric

Maximizing Current-Voltage (IV) Characteristics

Trend	Requirement
Advanced MPPT	Performance
Low DC voltage ripple	Performance
Overvoltage Protection	Performance & Safety
Overload Protection	Performance & Safety
Anti-theft detection	Flexible I/O

- FPGAs enable Advanced Shade-Tolerant MPPT to sweep for both local and global maxima (channels) to maximize I-V curve
- Low-cost DSPs limited to 1-channel MPPT and limited performance
- MPPT sample code available

Power Stage – 3L IGBT Cost & Efficiency



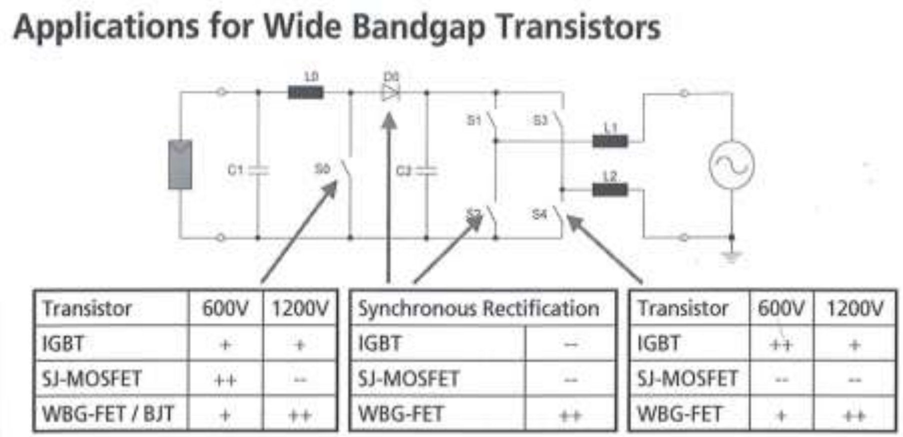
- 3-level IGBTs increase inverter efficiency to > 98%
  - Silicon (IGBT & MOSFET) devices are nearing theoretical limits
- Complex control algorithm with 3L IGBTs for efficiency
  - Lower EMI, better voltage quality, less current ripple (vs. 2L IGBTs)
- Higher precision pulse-width modulation (PWM) inverter control for more efficient energy recovery back into the grid
  - DSP technology struggle with 3-level or more level topologies

IGBT: Insulated Gate Bipolar Transistors

Power Stage – Wideband Gap Materials

- Wideband gap (WBG) power electronics – SiC, GaN

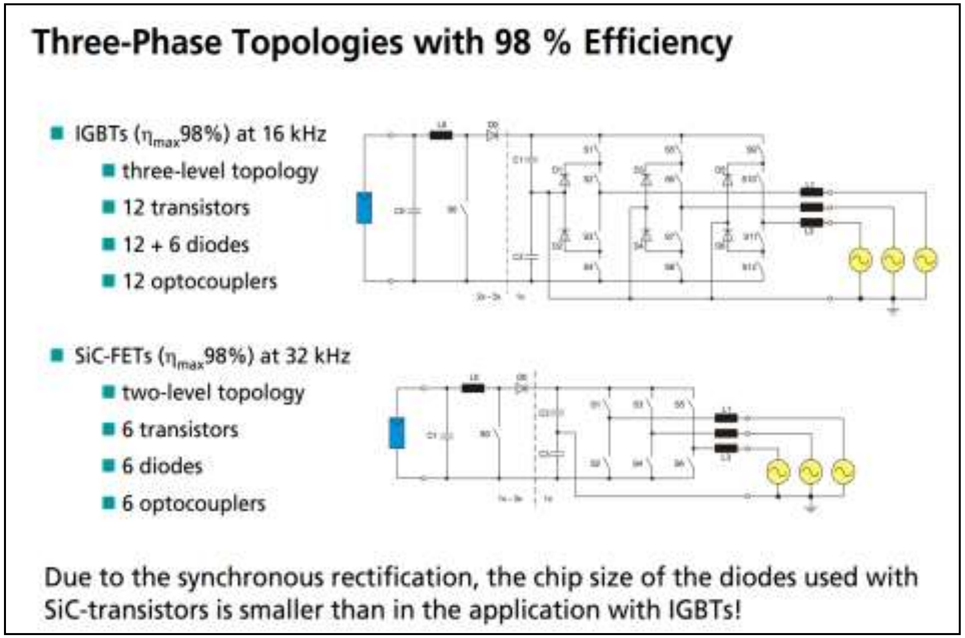
Trend	Requirement
Thermal Ruggedness	WBG Device
Higher Switching Frequency	WBG Device
Higher Breakdown Voltage	WBG Device



Source: Fraunhofer

- Achieve higher efficiency at same level of power topology
- Cost/efficiency and power density ideal for 10kW-40 kW inverters
  - > 600 V high-voltage inverters (SiC devices still cost more than IGBTs)
- Higher switching frequencies (beyond DSP capabilities) to reduce inductive component ratings and cost

Switch Faster/Better – FPGA For DC-AC



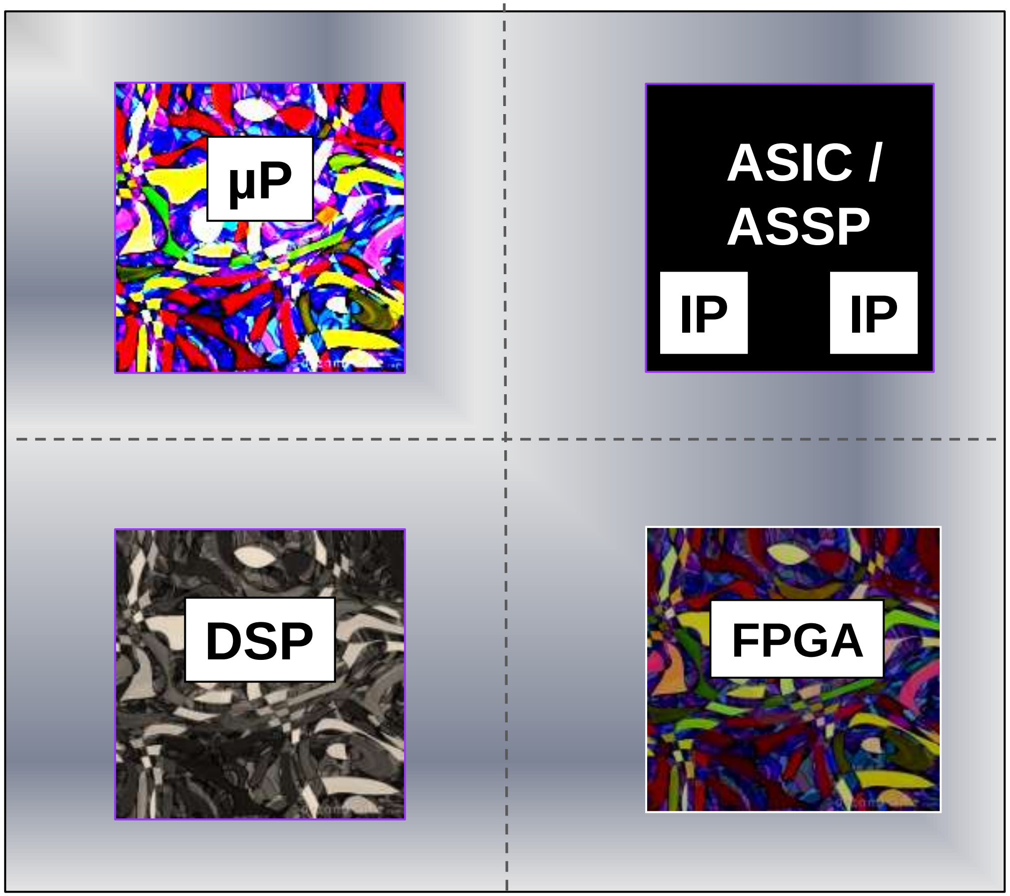
Source: Fraunhofer

Trend	Requirement
High Quality Output Sinewave	Performance
Low Current Distortion (THD)	Performance
Reduced Reactive Power ($\cos\varphi = 1$)	Performance
Overload Protection	Performance
Compliant to grid codes	Flexible I/O & Performance
Compliant to all standards	Flexible I/O & Performance

- Achieve higher efficiency with complex control in FPGA
- Achieve higher efficiency with increased switching frequencies
  - ~50% reduction in inductive component costs with 2x increase in frequency with wideband gap material (Source: Fraunhofer)
- DSPs struggle with multi-level and special topologies

Silicon Convergence – Best of All Worlds

Mixed System Fabric



- Support for legacy code
- Familiar C-code methodology

Wide Application Scope

- Optimized for DSP operations

- Support for high volume applications
- Application-specific IP

Wired Speed Wired Efficiency

- Off-the-shelf availability
- Support for changing standards / reconfigurable systems

FPGA Domain

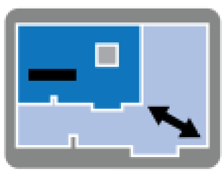
System-Level Benefits of SoC FPGA

Increased system performance

- 4,000 DMIPS for under 1.8W
- Up to 1,600 GMACS, 300 GFLOPS DSP
- >125 Gbps processor to FPGA interconnect
- Cache coherent hardware accelerators

Reduced power consumption

- Up to 30% power savings vs. 2-chip solution

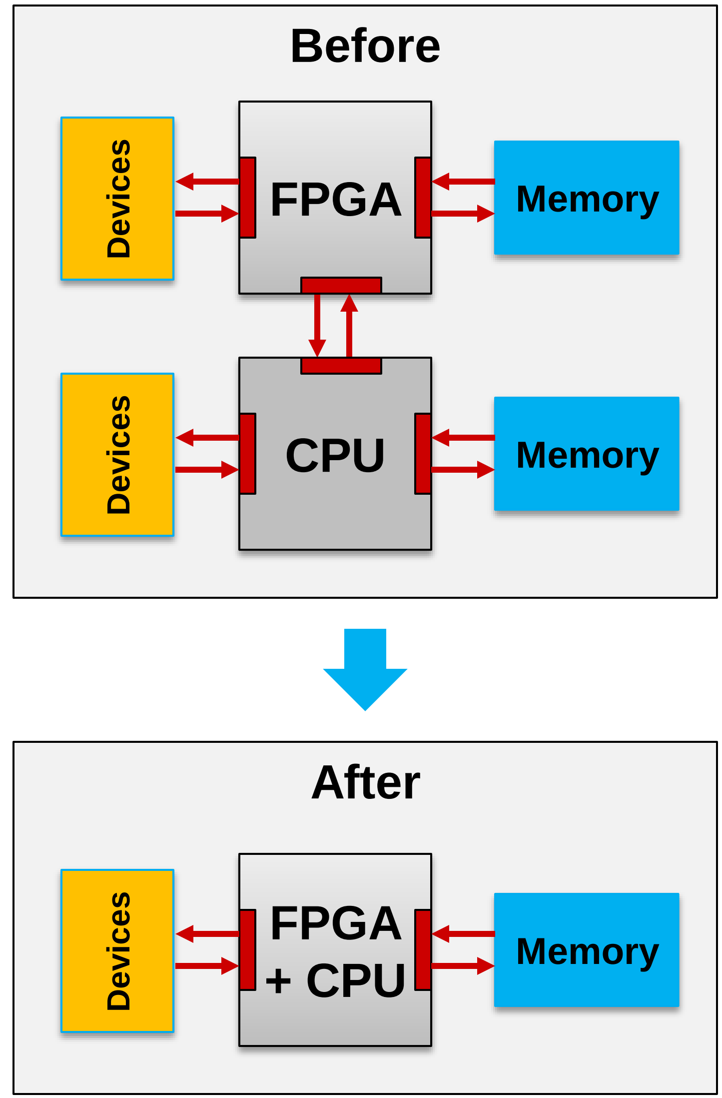


Reduced board size

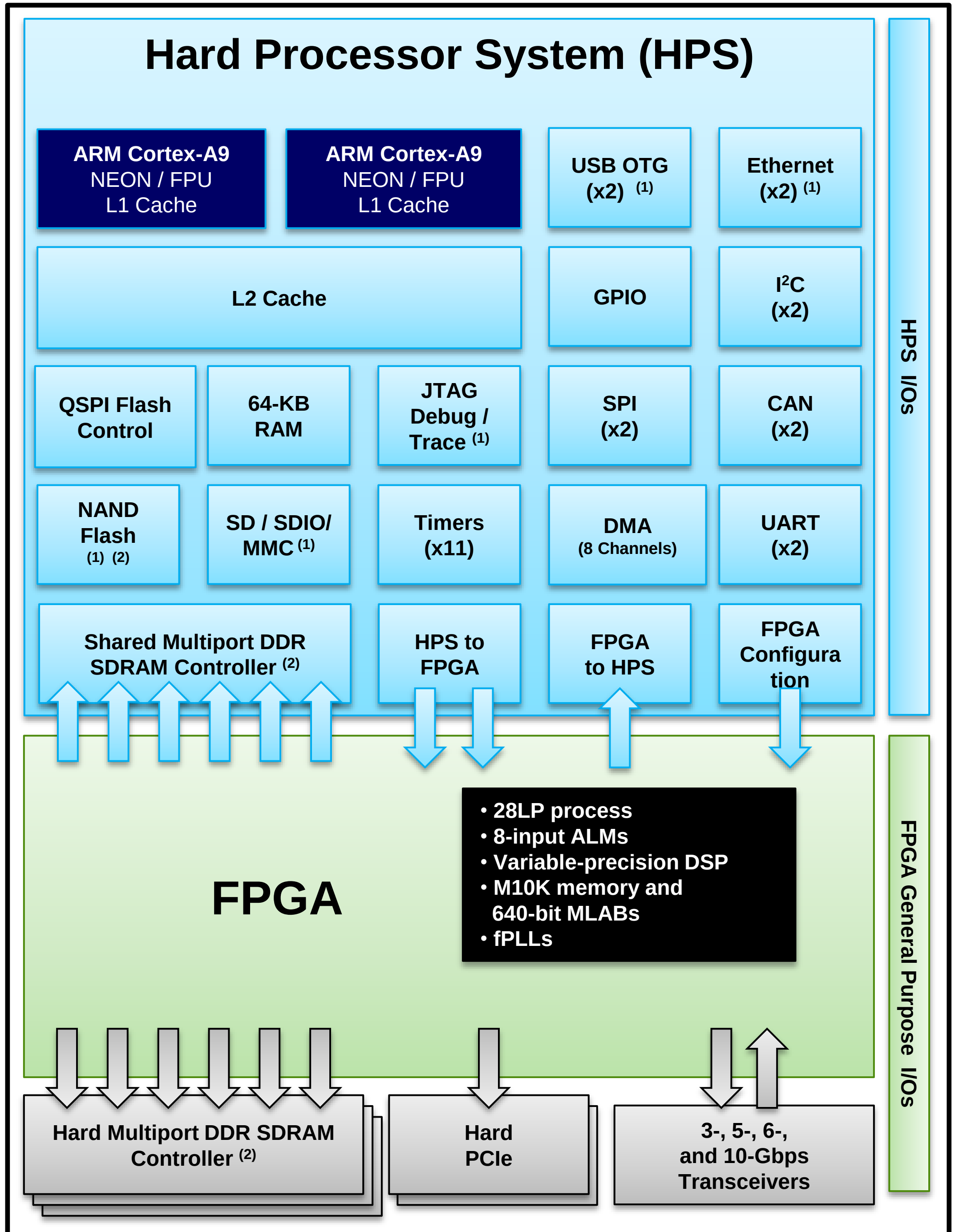
- Up to 55% form factor reduction
- As few as two power rails

Reduced system costs

- Lower component cost
- Reduction in PCB complexity and cost
  - Less routing with fewer layers

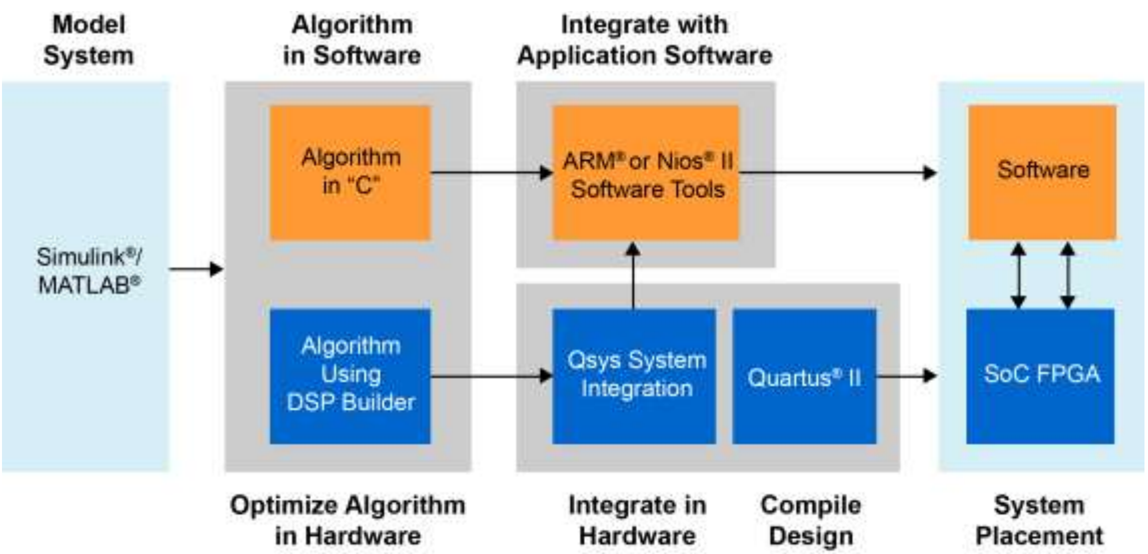


SoC FPGA Example

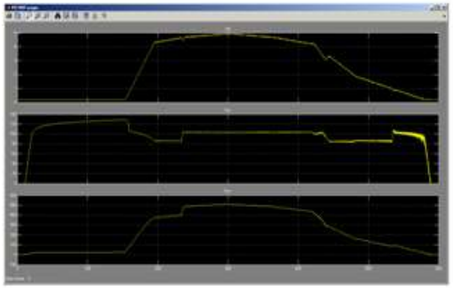


Notes:
(1) Integrated direct memory access (DMA)
(2) Integrated ECC

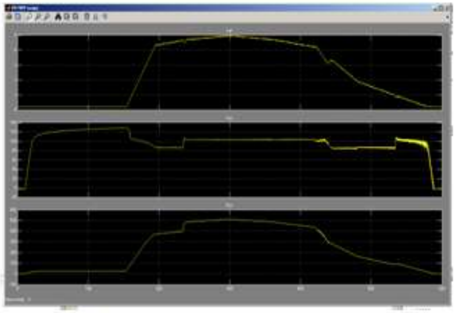
FPGA Tool For DSP System Design



ADSPB Example for MPPT Perturb & Observe (P&O)



Output characteristics of DSP Builder implementation of P&O MPPT Algorithm



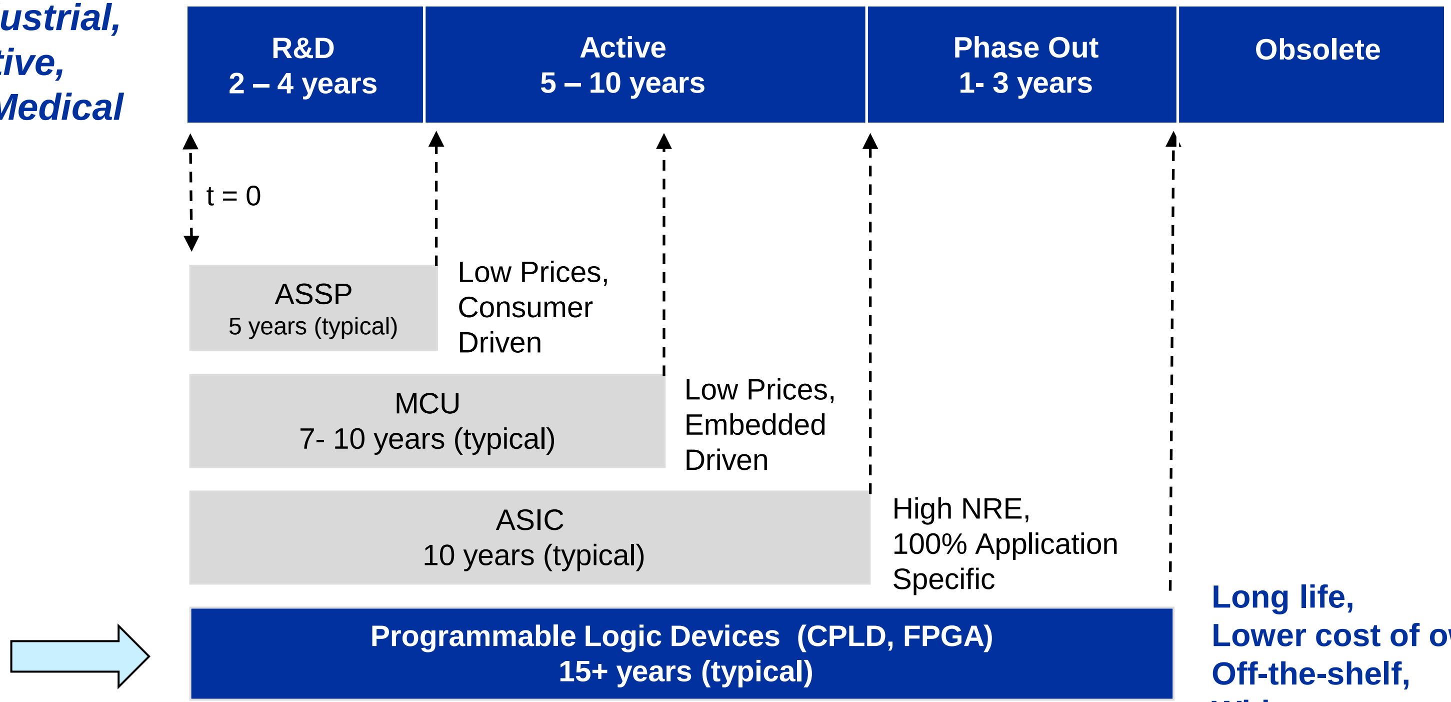
Output characteristics of software implementation of P&O MPPT Algorithm

- Move from Simulink model into FPGA design
- MPPT perturb & observe example shown

Commitment To Long Life Cycles

Alignment to application lifecycle dynamics

Military, Industrial, Automotive, Computer, Medical



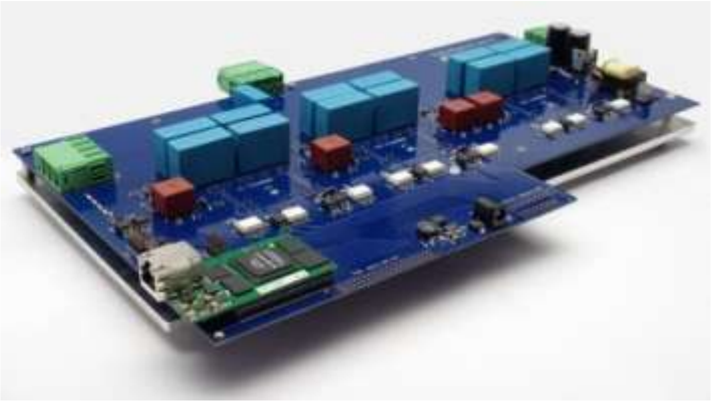
Long life,
Lower cost of ownership,
Off-the-shelf,
Wide customer base

PCN procedure meets or exceeds industry standards (JEDEC, ISO-9000, etc.)

Example 1: PV inverters need to last 25 years to match panel warranties
Example 2: Average substation equipment (e.g., in NA) is > 40 years old

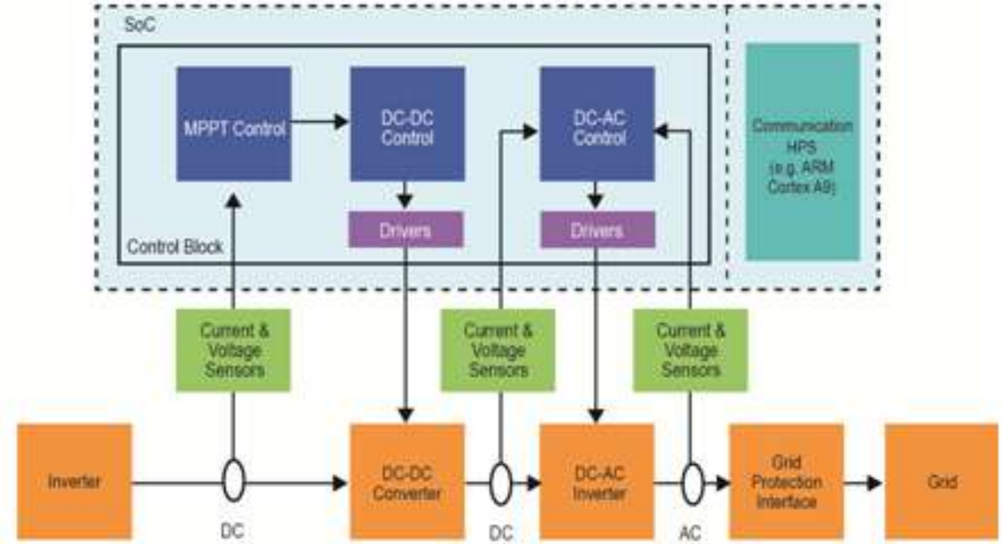
PV Inverter Reference Design Example

- State-of-the-art 3-phase/3-level inverter reference design
  - Ideal for 3~ Solar Inverter
  - Reduced current ripple
  - Reduced EMI
  - Reduced passives (size, weight and cost)
- Reasonable 3-Level IGBT resource usage



Function	IP	Size	Performance	IO
Inverter Control on Cyclone FPGA	MPPT & DC-DC control (Single Channel P&O)	<1K LEs	100 MHz	1x Voltage Sensor 1x Current Sensor
	DC-AC control (Switching Frequency 16kHz, capable up to 50kHz)	14K LEs		PWM (3L IGBTs): 12 Gate Signals 6 Vcc Fault Signals 3 Current & 2 DC Voltage ΣΔ signals

Summary



- Switch Better/Cheaper – Increased efficiency using FPGA control loop & multi-level IGBTs
- Switch Faster/Cheaper – Increased switching frequency and further reduce inductive component costs with FPGAs & wideband gap materials
- Switch Easier – From simulation to FPGA implementation using Simulink to FPGA tool flow
- Manage Life Cycle – FPGAs stay in production for a long time
- Migrate Smoother – Partition hardware/software and recompile IP for next generation FPGAs and SoCs

Thank You