SP1.5.6: High-Efficiency Power Electronics Switching for Alternative Energy Applications

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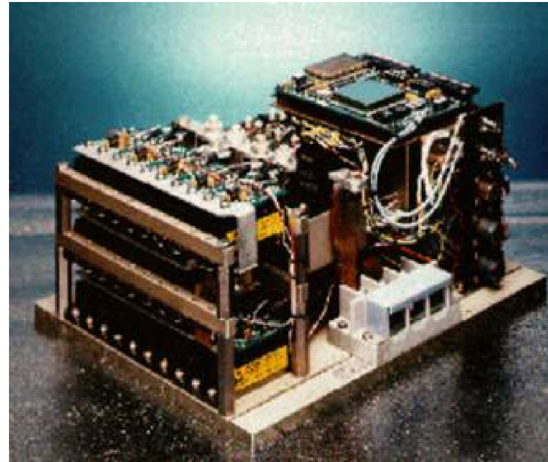
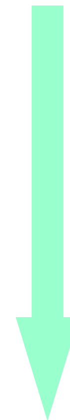
Need More Efficient Semiconductor Power Switch



Silicon Power Switch

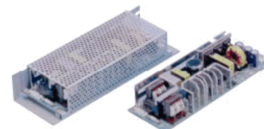
50,000 cm^3
18 kg



Shenai's Figure of Merit -

$$Q_{F2} = \lambda \sigma_A E_M$$

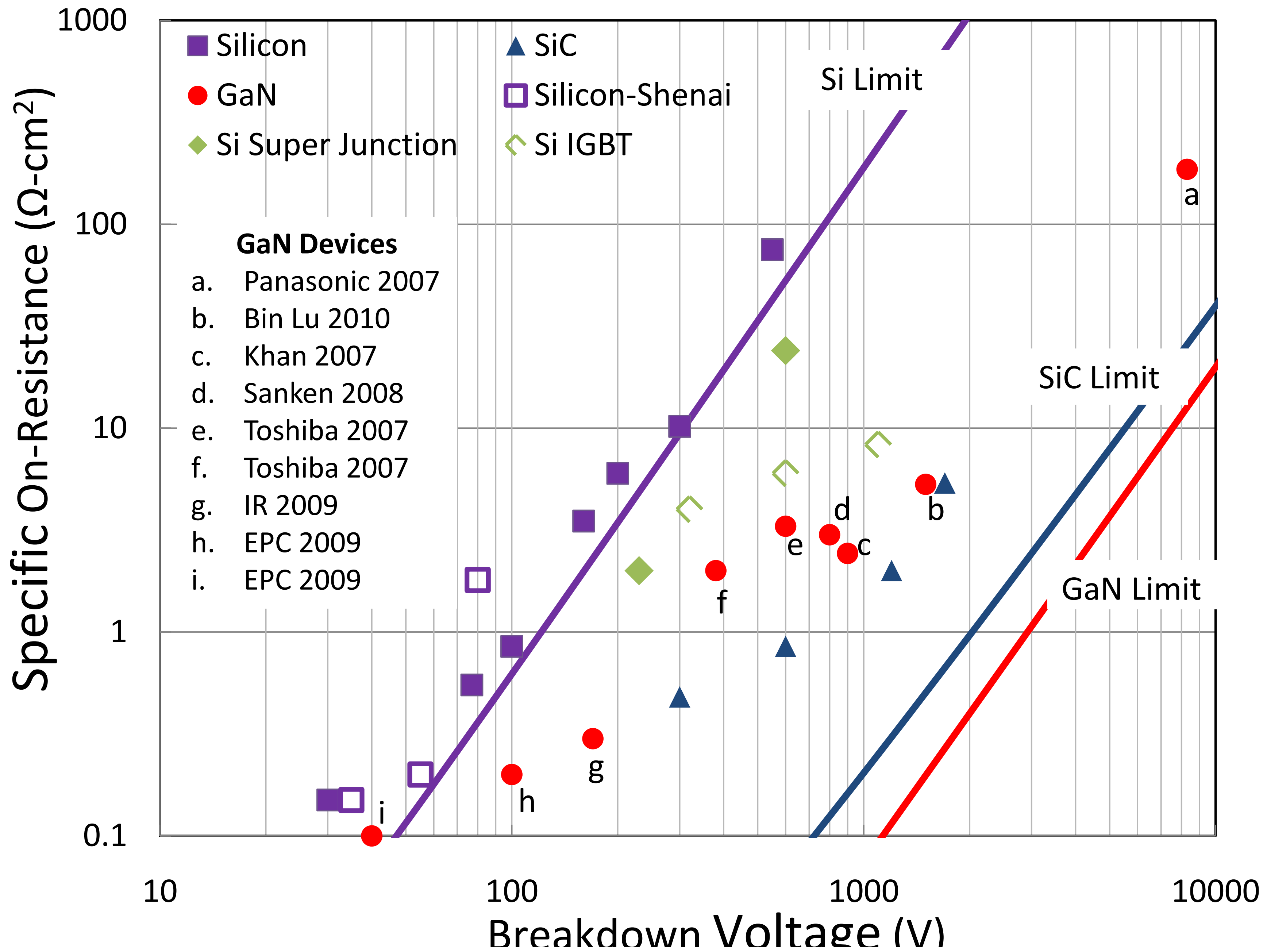
2400x improvement



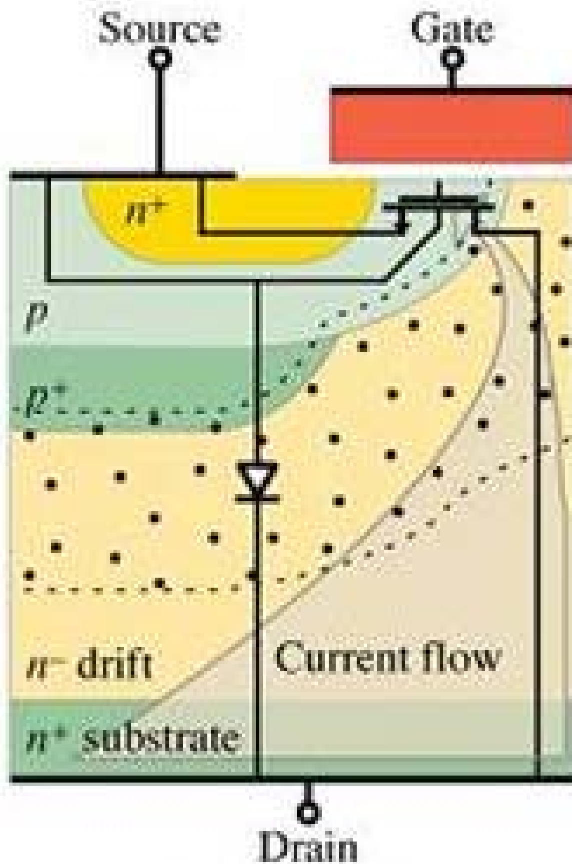
SiC or GaN Power Switch

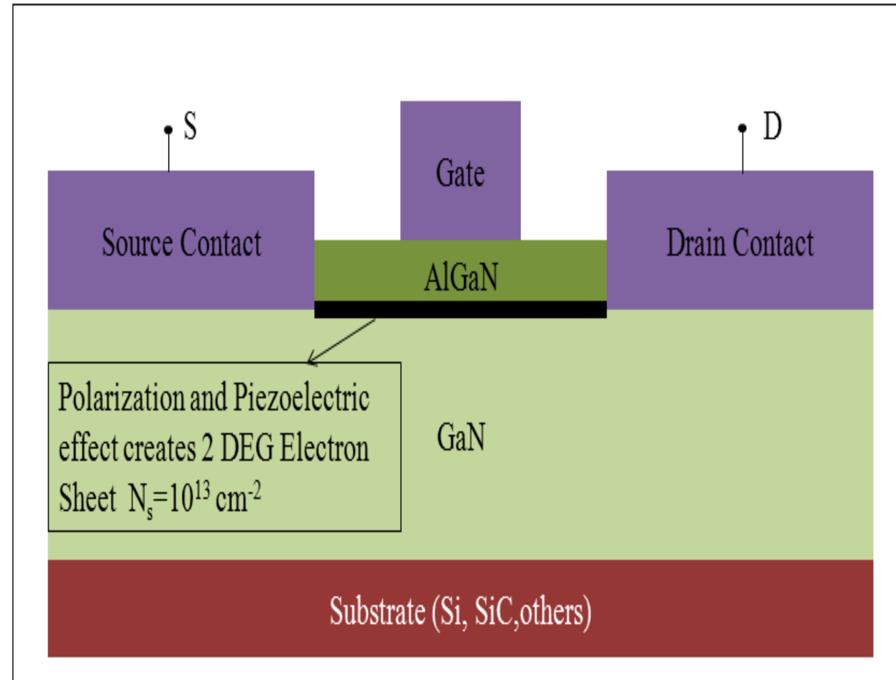
4,500 cm^3
0.2 kg

K. Shenai *et al*, *IEEE Trans. Electron Devices,* pp. 1811-1823, 1989


Silicon
SiC
GaN
Silicon-Shenai
Si Super Junction
Si IGBT
Si Limit
SiC Limit
GaN Limit
GaN Devices
a. Panasonic 2007
b. Bin Lu 2010
c. Khan 2007
d. Sanken 2008
e. Toshiba 2007
f. Toshiba 2007
g. IR 2009
h. EPC 2009
i. EPC 2009
a
b
c
d
e
f
g
h
i
Specific On-Resistance (Ω-cm²)
1000
100
10
1
0.1
10
100
1000
10000
Breakdown Voltage (V)

Vertical vs. Lateral Devices





Silicon Vertical DMOSFET

$$R_{sp} = \frac{4V_B^2}{\varepsilon_s \mu E_c^3}$$

GaN Lateral HEMT

K. Shenai *et al, IEEE Trans. Electron Devices,* pp. 1811-1823, 1989

Point-of-Load (POL) Converter Application in Cell Phones

2

10 – 20%

External LDO, SMPS

Backlight Driver
High Voltage
Low Current

PA Driver
High Power

1

60 – 70%

Hybrid SMPS

3

Hybrid SMPS

Battery Charger
Low Voltage
High Current

4

10 – 20%

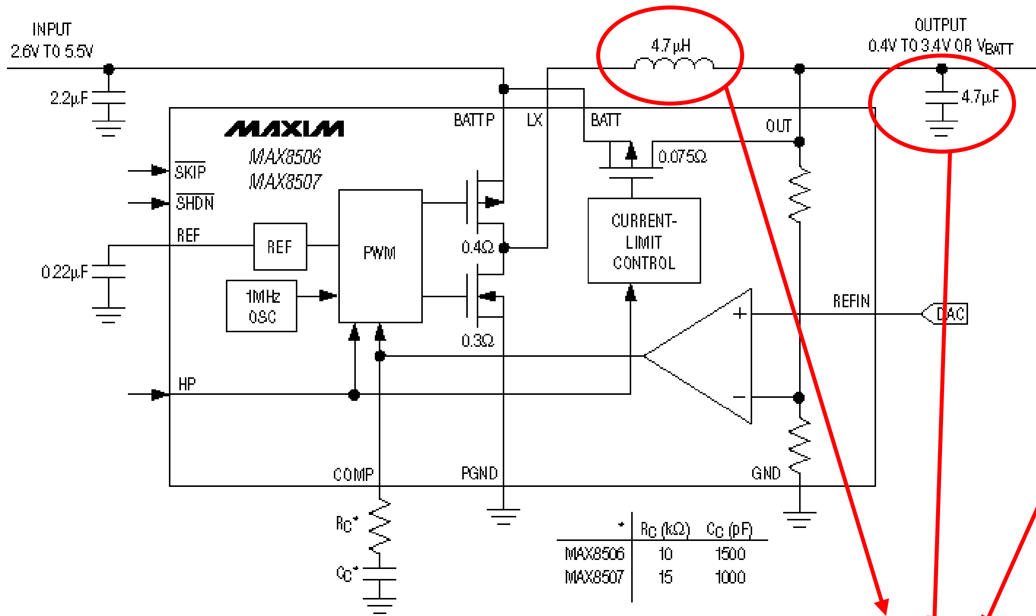
Integrated LDO, SC, CP

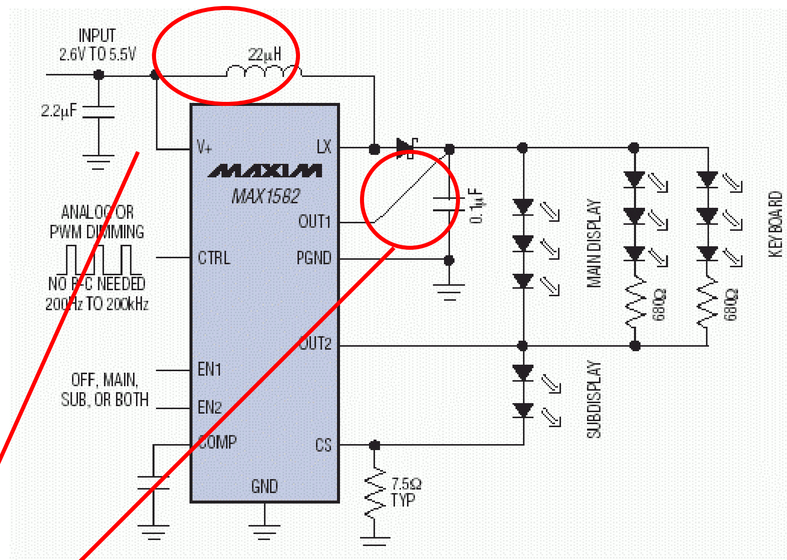
Baseband
(DSP, Arm, Audio amp, …)
High Speed

Point-of-Load (POL) Converter Integration

Maxim 8506-8508 in a Cell Phone PA Power Supply

Maxim 1582 in a Notebook White LED Power Supply

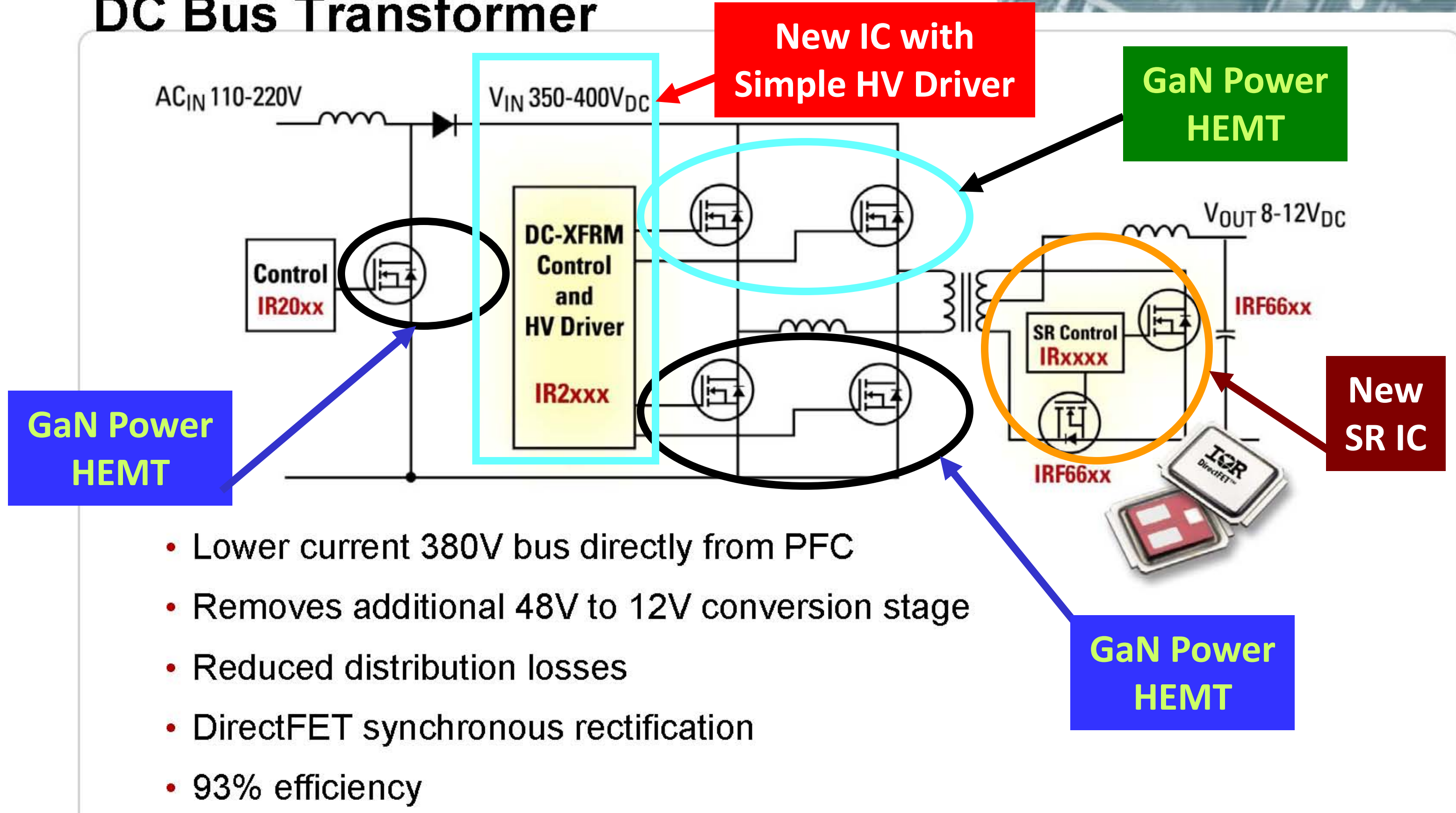




Large External Passives

High-frequency (@ > 1 MHz) switch-mode power conversion facilitates on-chip integration of passive elements.

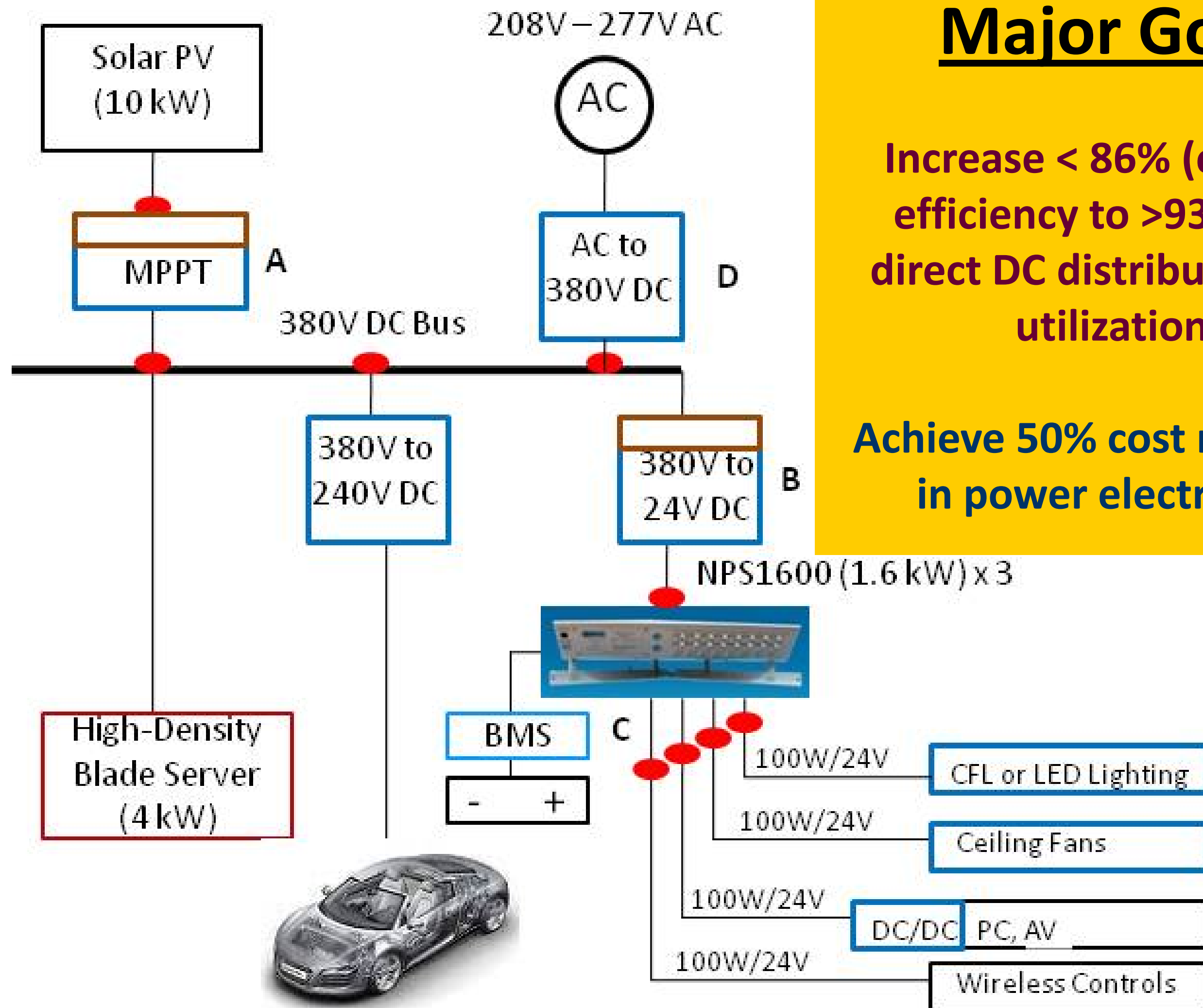
More Integrated Solution in High-End Computer Servers



Replace with Efficient Power Switches and IC, Eliminate HV Driver

Increase Overall Efficiency to 93%, Reduce Cost by 60%

10 kW Distributed Smart DC Solar Microgrid



Major Goal:

Increase < 86% (current) efficiency to >93% with direct DC distribution and utilization.

Achieve 50% cost reduction in power electronics.

Monitoring Point

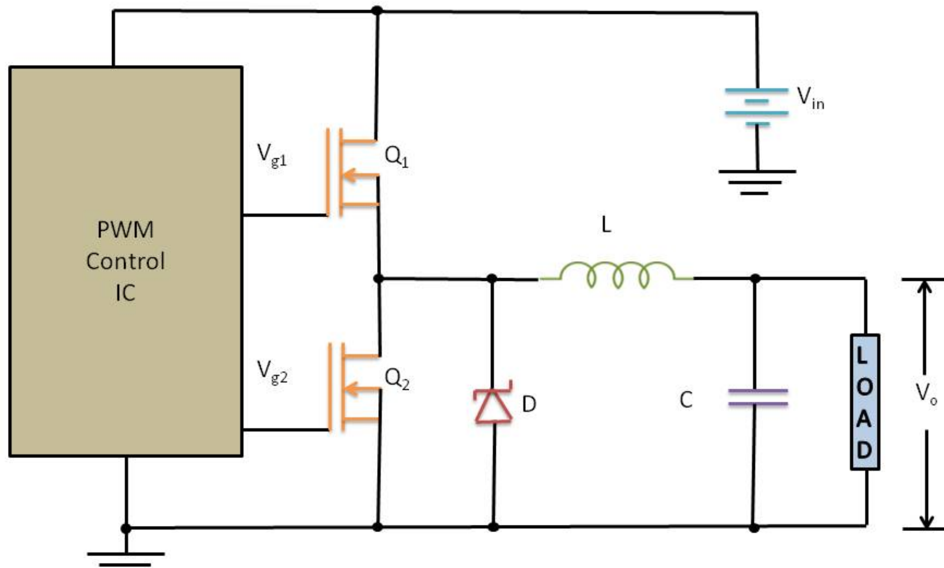
Nextek Power Systems

University of Toledo

A: Maximum Power Point Tracker (MPPT)
B: 380V/24V DC/DC Converter
C: Battery Management System
D: 10 kW AC/DC Rectifier

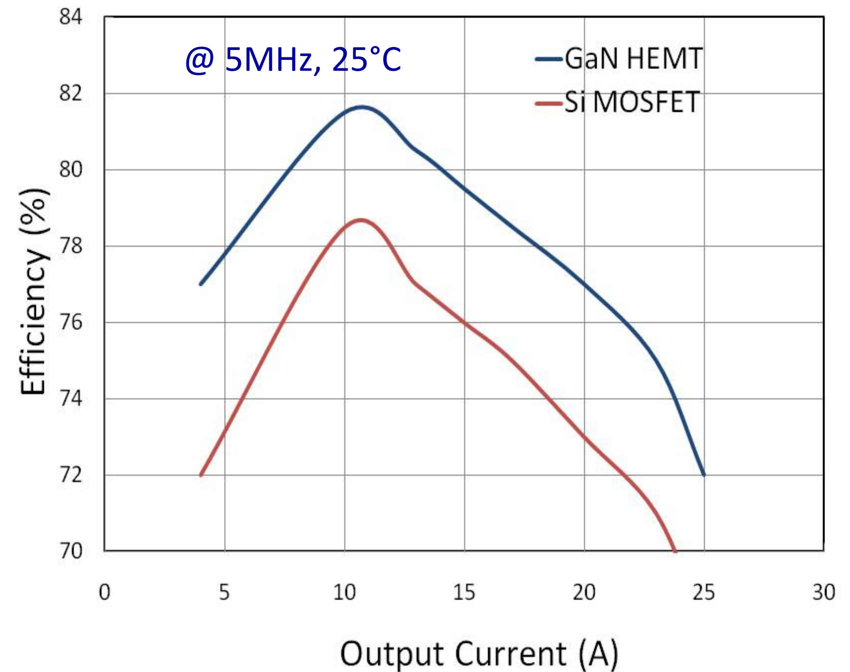
24V DC is distributed via Emerge ™ Alliance DC Flex Zone Ceiling grid

High-Efficiency Point-of-Load (POL) DC-DC Converter



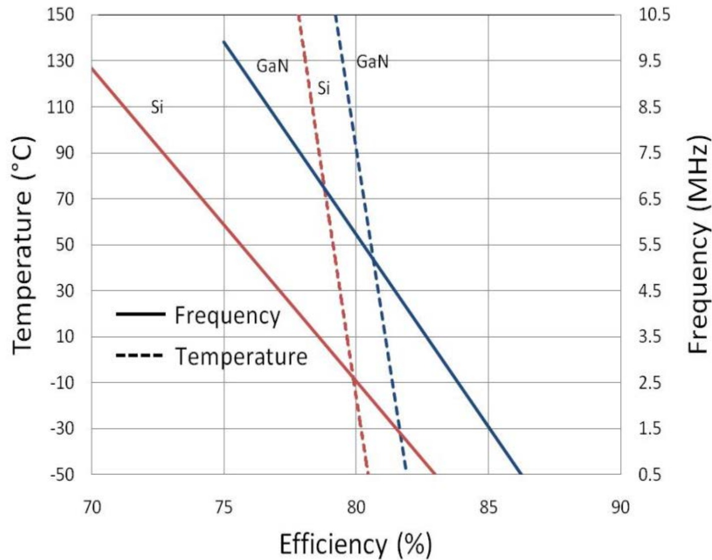
12V/1V, 10W Synchronous Buck Converter

Device	V_{BR} (V)	V_T (V)	$R_{DS(on)}$ (mΩ)	C_{ISS} (nF)	C_{OSS} (nF)	C_{RSS} (pF)	Q_G (nC)
Best Silicon MOSFET	30	1.6	6	2.3	2	300	40
Best GaN E-Mode HEMT	40	1.4	16	0.3	0.32	50	3

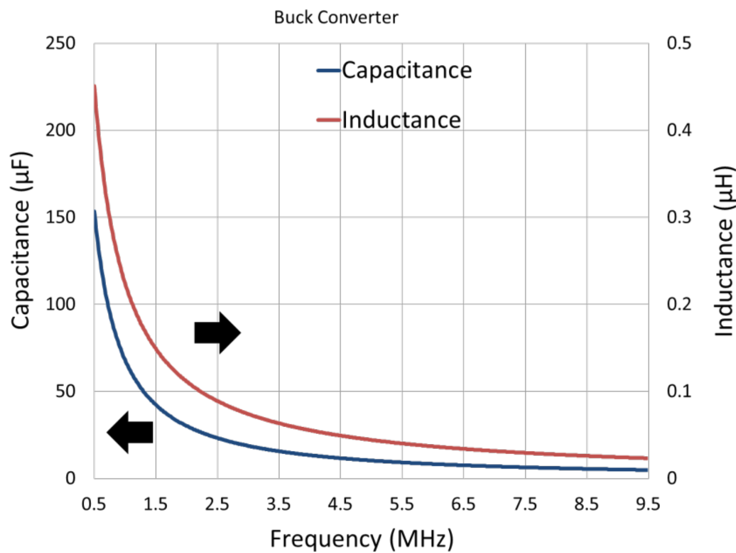


K. Shenai, *Proc. IEEE Int. Electron Devices and Solid-State Circuits (EDSSC) Conference*, Hong Kong, Dec. 2010 (**invited paper**)

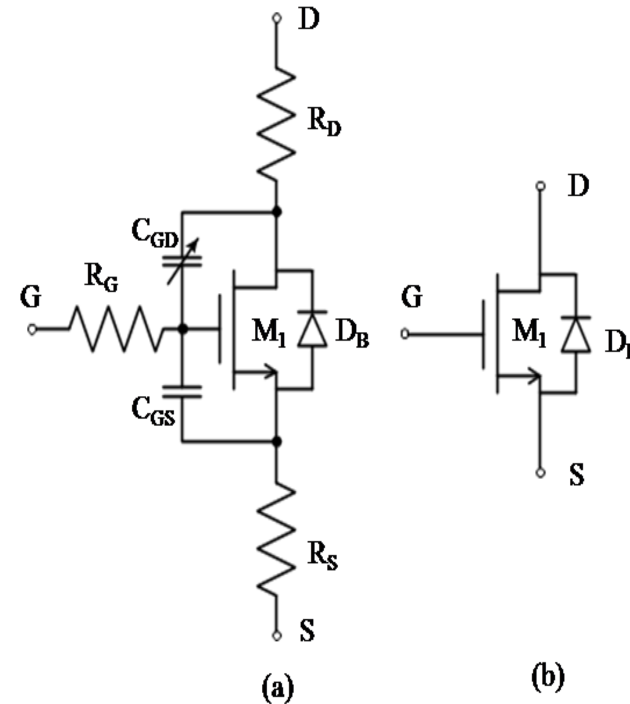
12V/1V, 10W Point-of-Load (POL) DC-DC Converter



vs. Frequency @ 25°C; vs. Temperature @ 5MHz



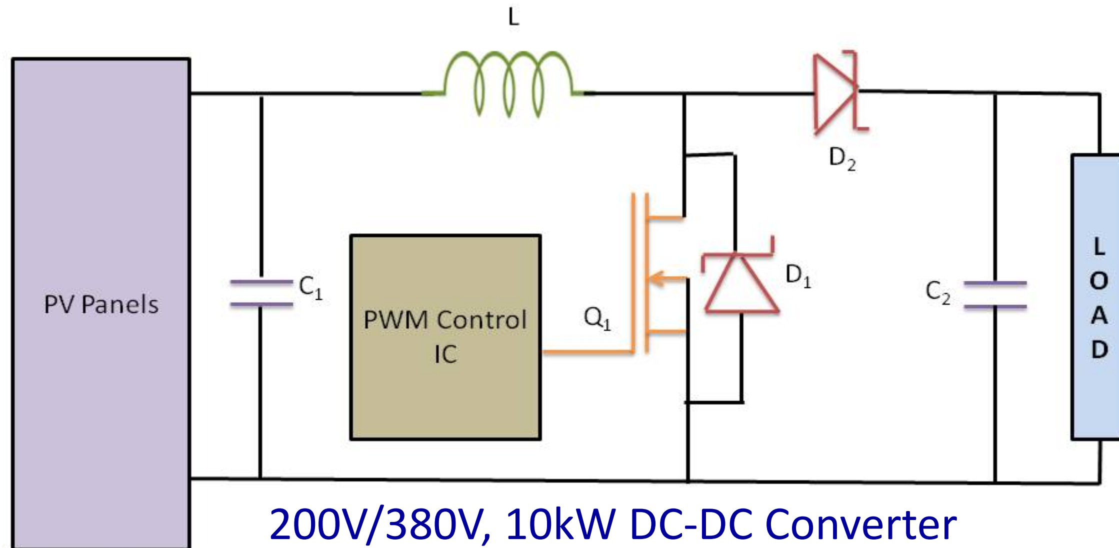
Circuit Simulation Model



K. Shenai, *IEEE Trans. Power Electronics*, vol. 6, no. 3, pp. 539-547, July 1991.

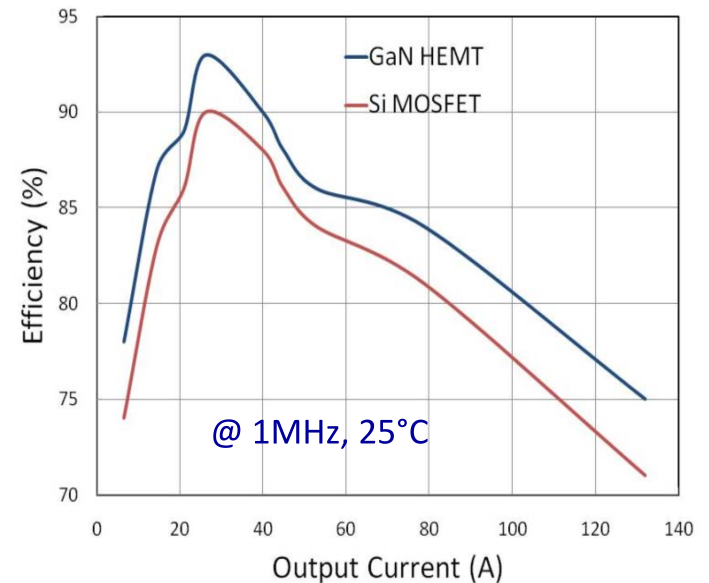
K. Shenai, *Proc. IEEE Int. Electron Devices and Solid-State Circuits (EDSSC) Conference*, Hong Kong, Dec. 2010 (**invited paper**)

High-Efficiency Boost Converter



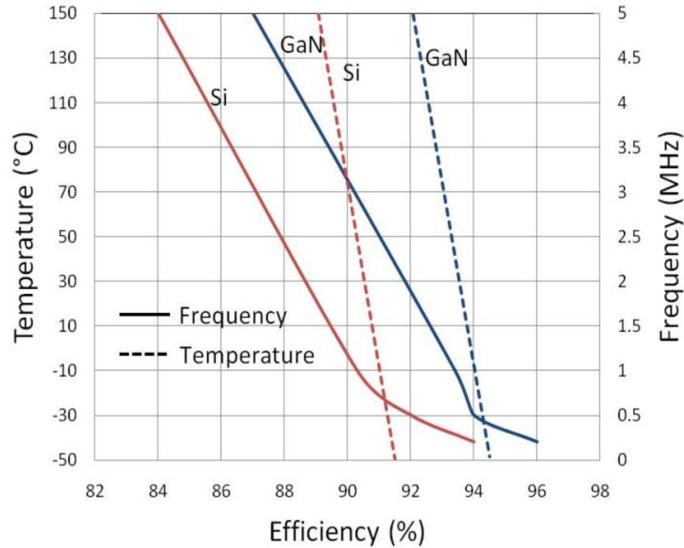
200V/380V, 10kW DC-DC Converter

Device	V_{BR} (V)	V_T (V)	R_{ON} (mΩ)	C_{ISS} (nF)	C_{OSS} (nF)	C_{RSS} (nF)	Q_G (nC)
Best Commercial Silicon MOSFET	600	3	99	4.5	20	1.8	60
Scaled GaN E-Mode FET	600	1.4	40	1.5	2.1	0.3	45

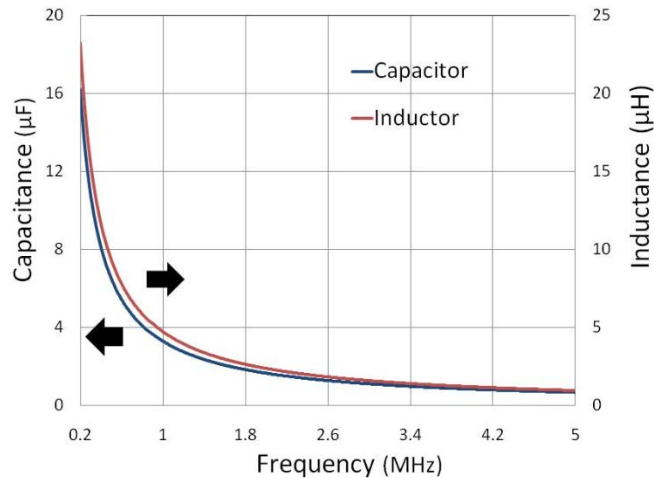


K. Shenai, *Proc. IEEE Int. Electron Devices and Solid-State Circuits (EDSSC) Conference*, Hong Kong, Dec. 2010 (**invited paper**)

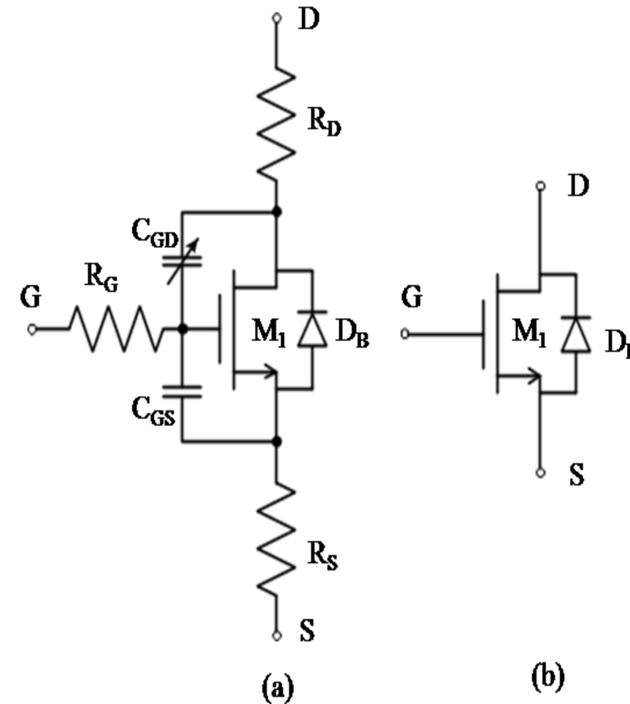
200V/380V, 10kW DC-DC Converter



vs. Frequency @ 25°C; vs. Temperature @ 1MHz



Circuit Simulation Model



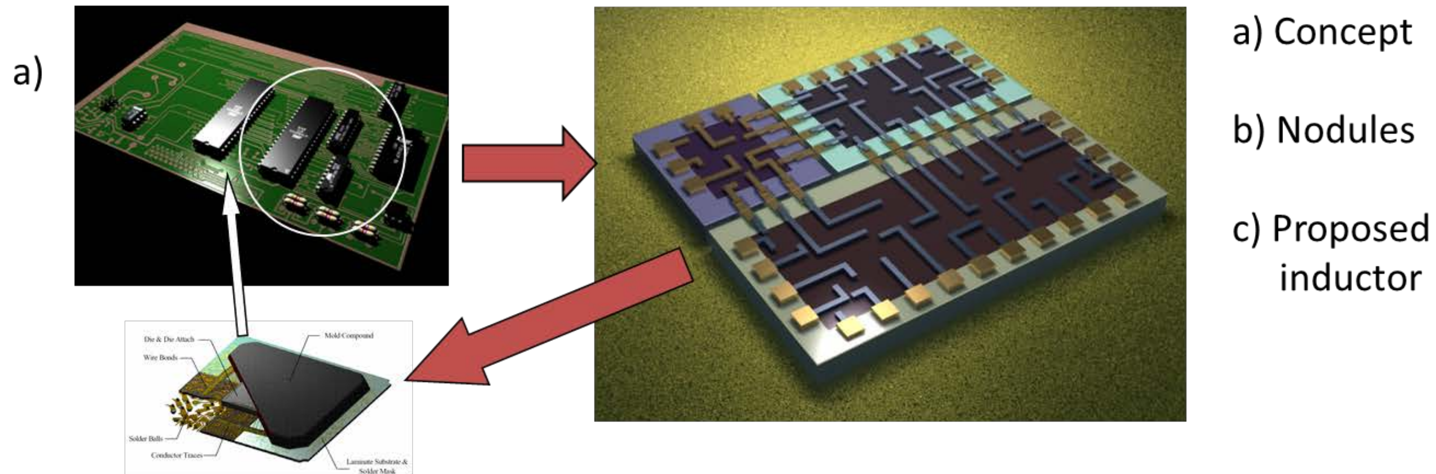
K. Shenai, *IEEE Trans. Power Electronics*, vol. 6, no. 3, pp. 539-547, July 1991.

K. Shenai, *Proc. IEEE Int. Electron Devices and Solid-State Circuits (EDSSC) Conference*, Hong Kong, Dec. 2010 (**invited paper**)

Chip-Scale Power Integration

Notre Dame "Quilt Packaging"

a)

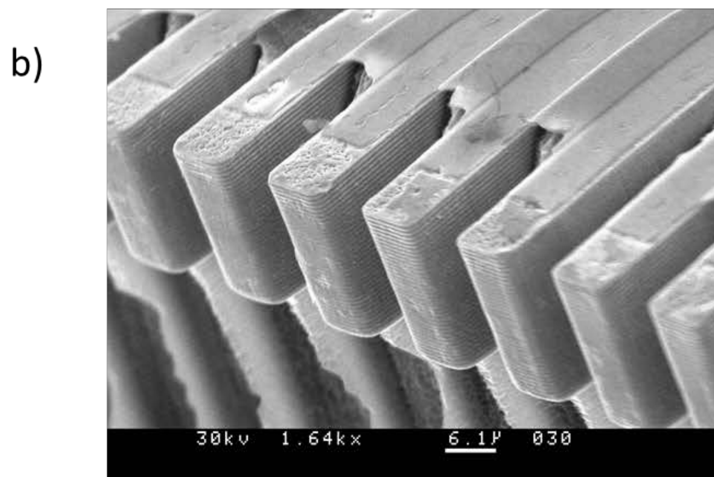


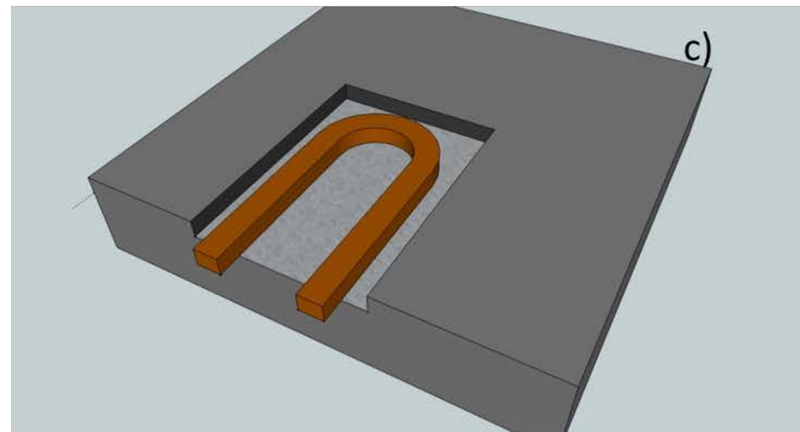
a) Concept

b) Nodules

c) Proposed inductor

b)



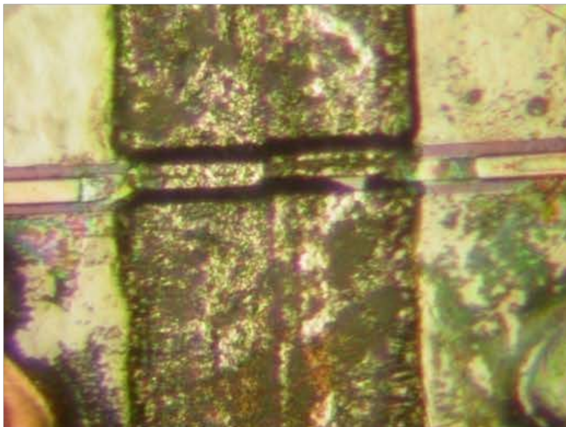


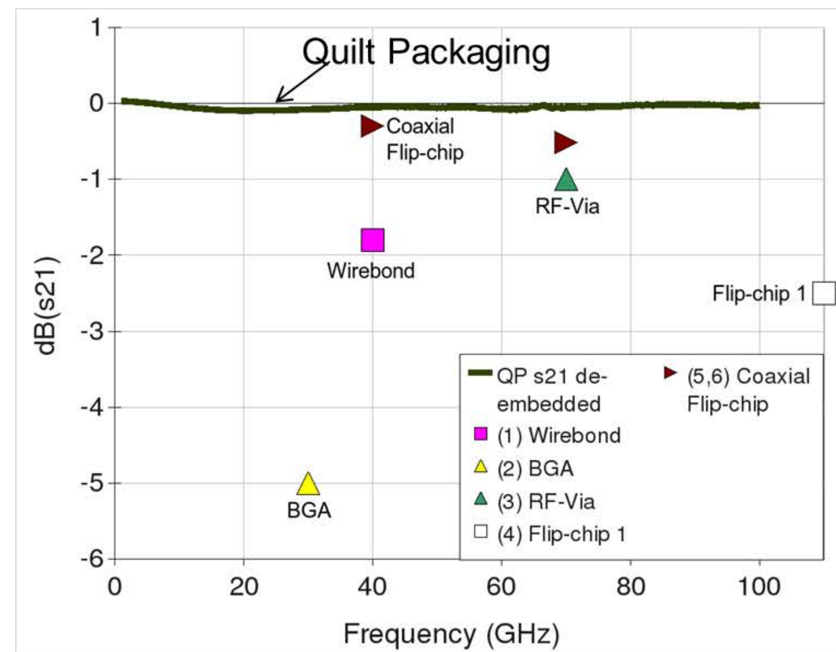
Collaborators: Dr. Gary H. Bernstein (University of Notre Dame) and Dr. Jayne Wu (University of Tennessee)

Chip-Scale Power Integration

QP Allows World-Record Chip-to-Chip Bandwidth

- De-embedded insertion loss compared with recent papers on wire bonds, ball grid array, MS-to-CPW RF-via, flip chip.
- 0.25 dB lower than coaxial flip-chip via at 40 GHz
- 1.7 dB lower than standard flip-chip at 110 GHz
- 0.8 dB lower than RF-via at 70 GHz

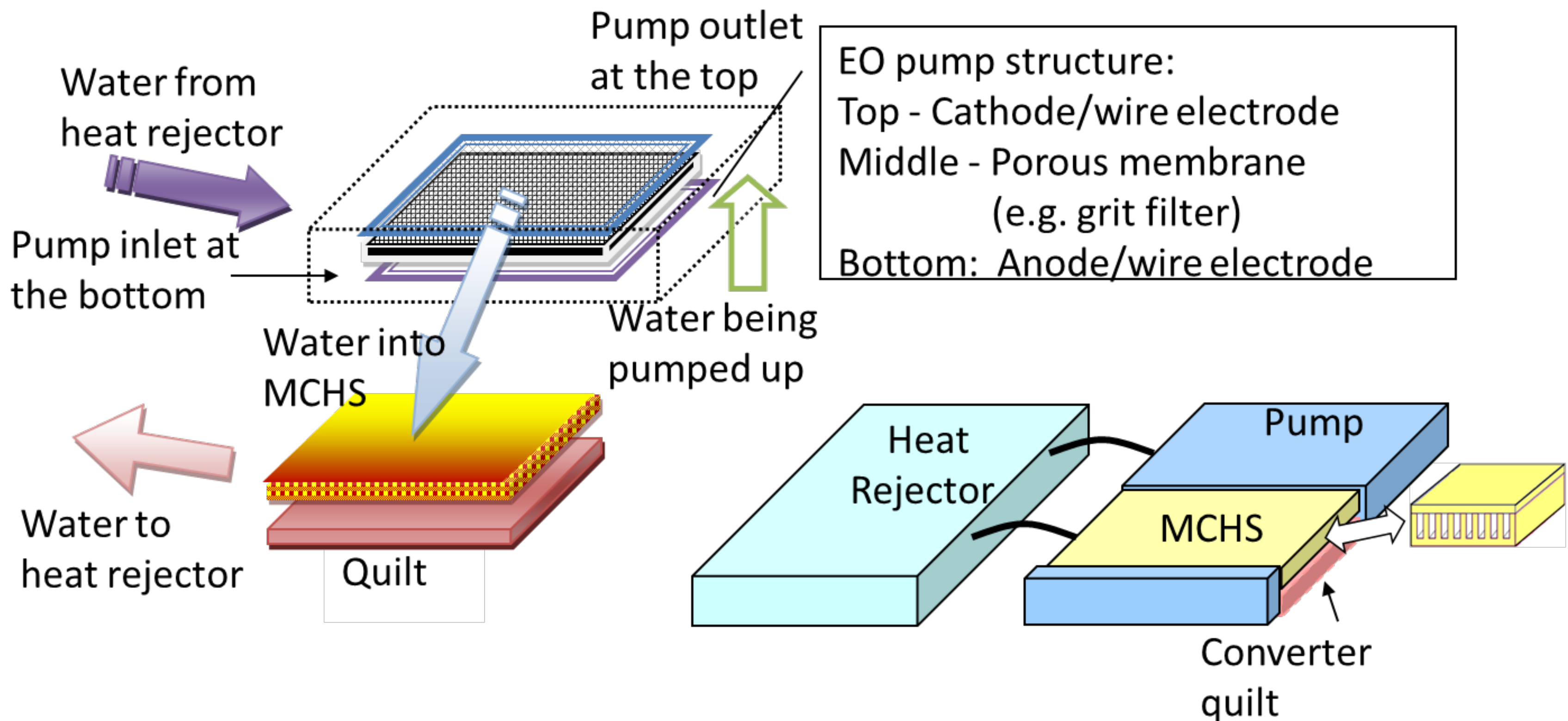




Collaborator: Dr. Gary H. Bernstein (University of Notre Dame)

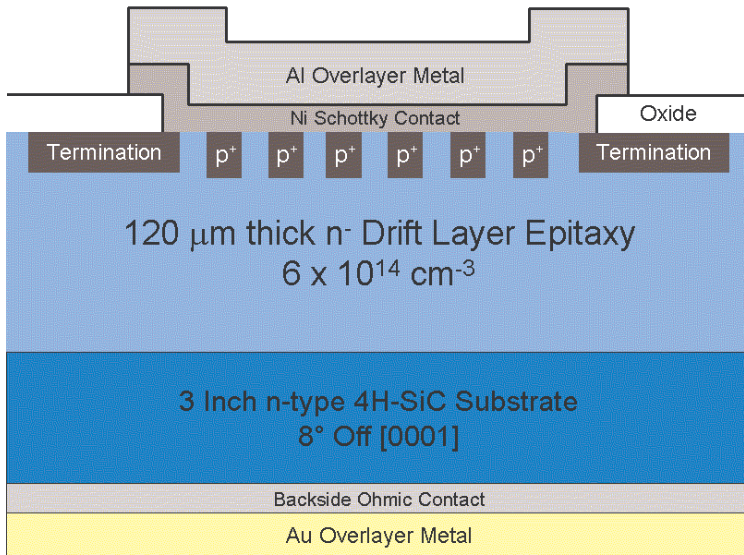
Power Chip Cooling

Electro Osmotic DC Micro Cooling



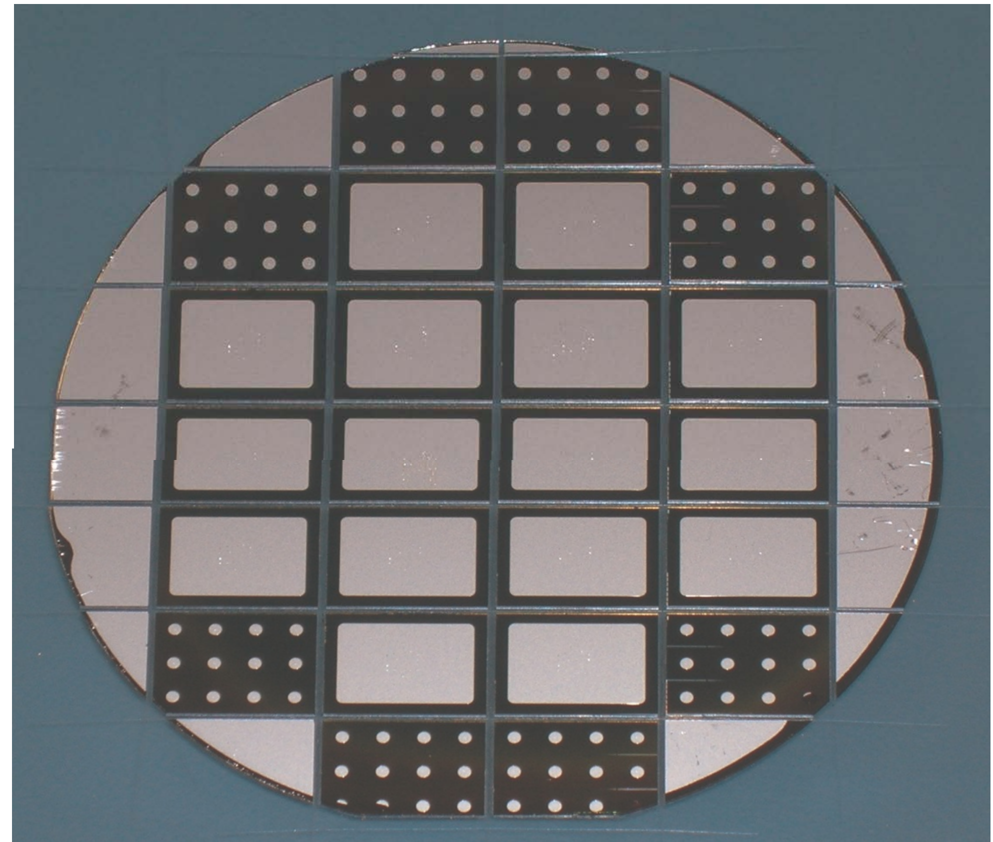
Collaborator: Dr. Jayne Wu (University of Tennessee at Knoxville)

Current Status of Best R&D SiC JBS Rectifier



Cross section of 10 kV SiC JBS rectifier – Not commercially available

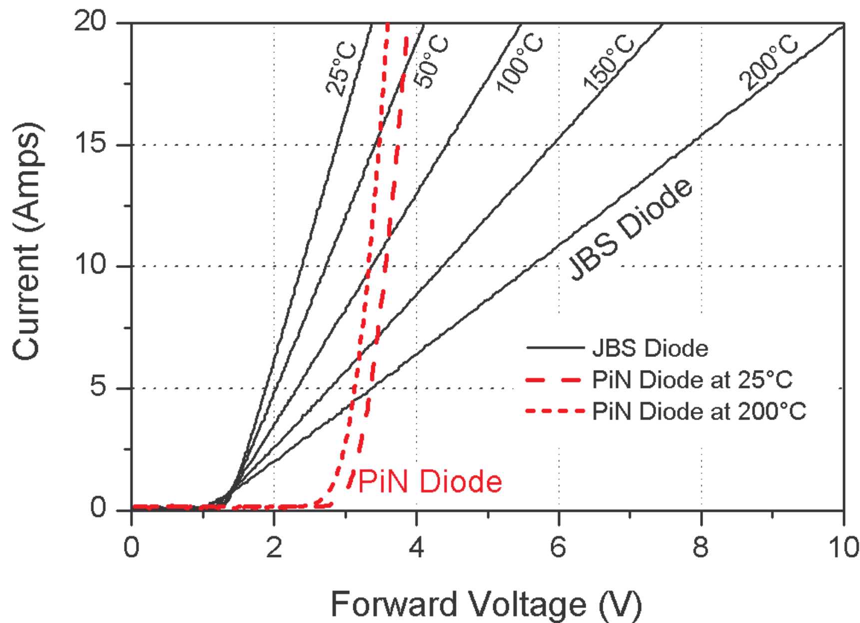
Device fabricated on best R&D 3 inch SiC PVT wafers with nearly zero micro pipes and lowest screw dislocation density

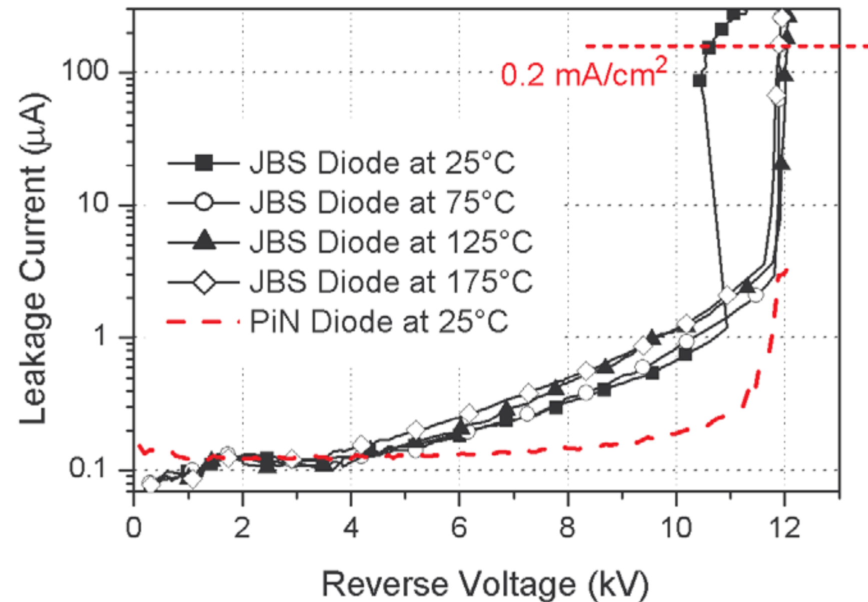


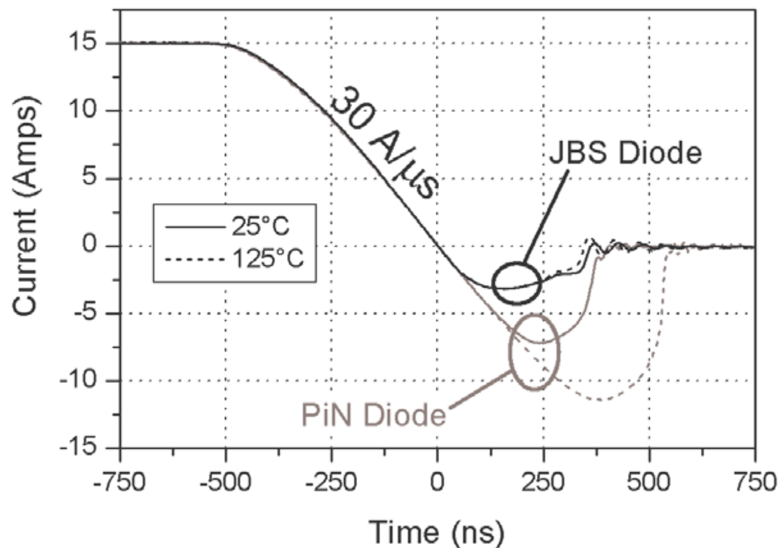
10 kV/20A SiC JBS rectifier on 3 inch wafers– Not commercially available

Hull et al, *Mat. Res. Forum,* vols. 600-603, pp. 931-934, 2009 - Cree & NIST paper

Current Status of Best R&D SiC JBS Rectifier







Breakdown voltage derated by 40%

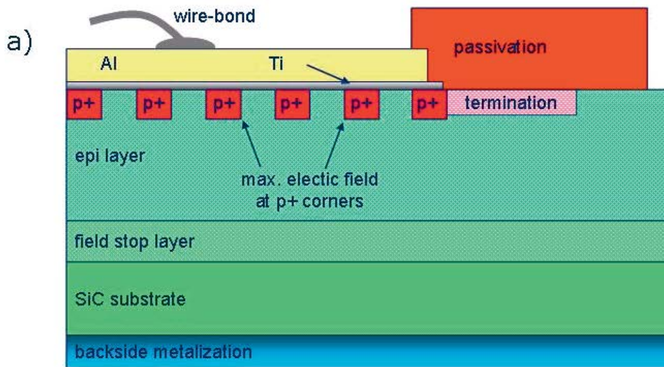
Majority carrier diode

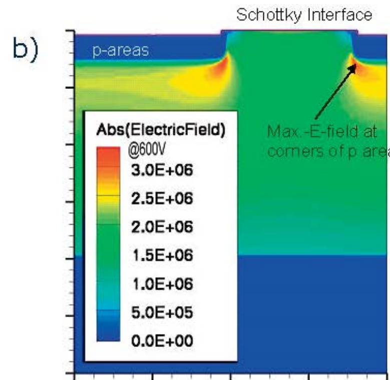
High leakage current

Nothing reported on reliability

Hull et al, *Mat. Res. Forum,* vols. 600-603, pp. 931-934, 2009 - Cree & NIST paper

Current Status of Best Commercial SiC MPS Rectifier





1.2 kV/20A diode

Breakdown voltage derated by 30%

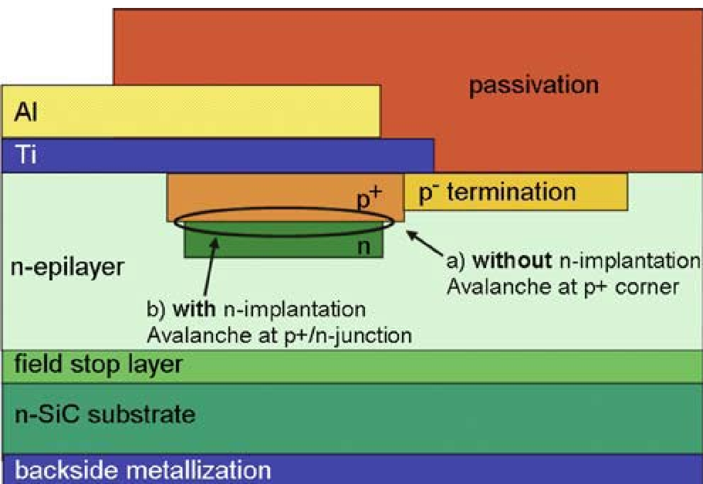
Breakdown at edge termination

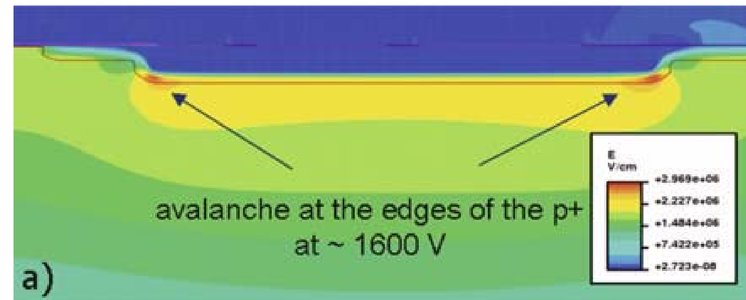
Majority carrier diode

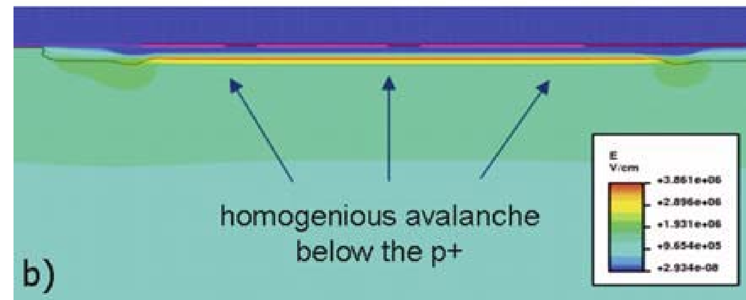
High leakage current

Poor *dv/dt* < 50V/ns

Nothing on switching reliability

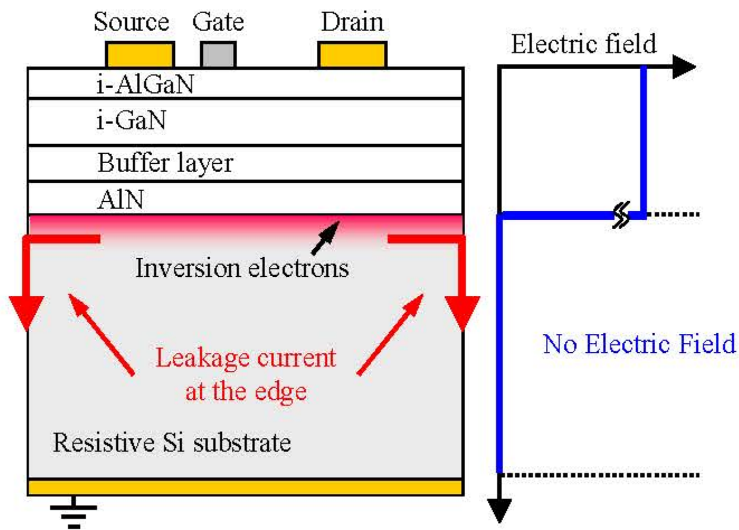




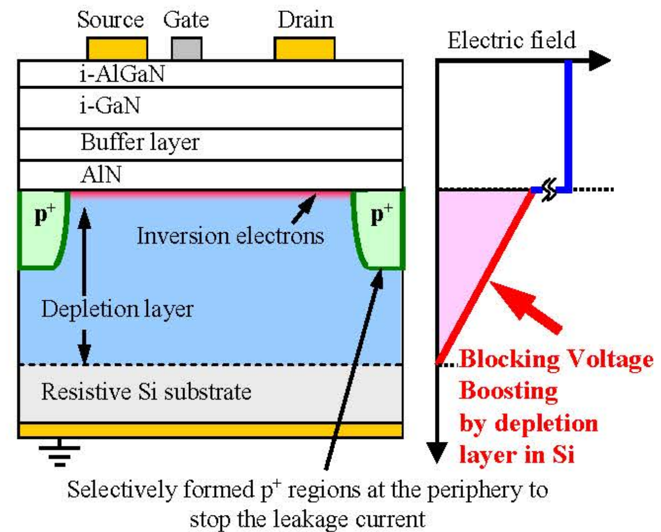


Holz et al, *Phys. Status Solidi A 206,* no. 10, 2295-2307, 2009 – Infineon paper

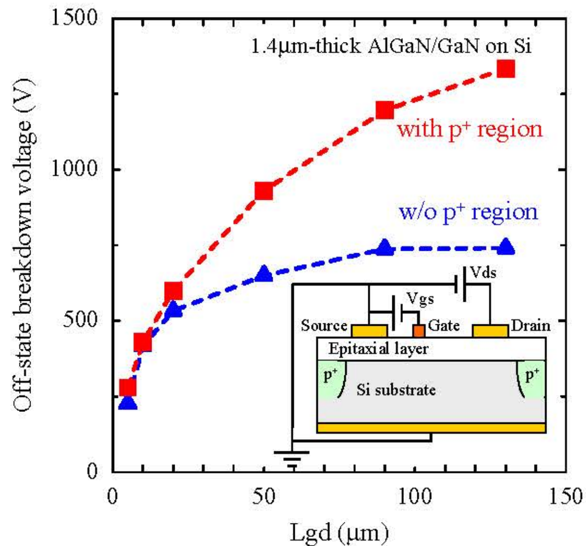
High-Voltage GaN HFETs

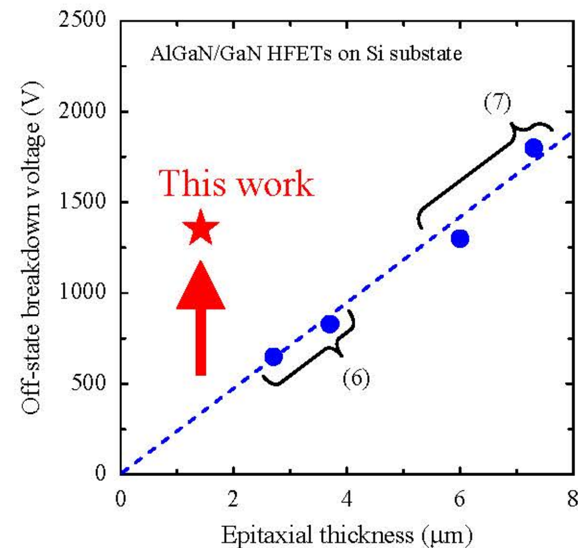


(a) Conventional HFET



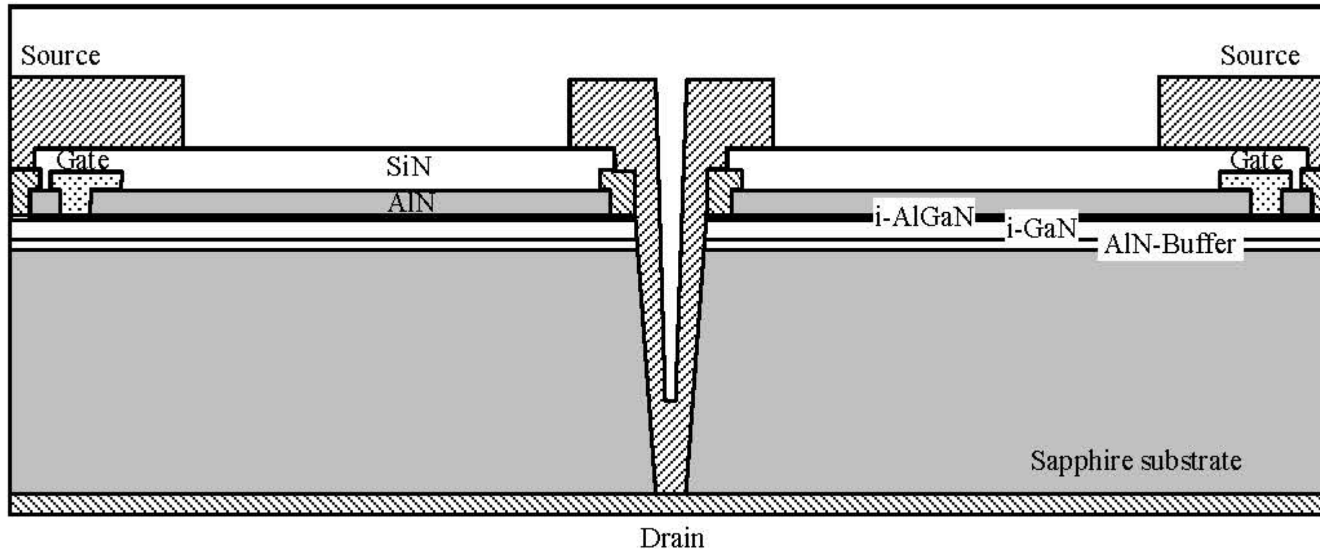
(b) Proposed HFET with channel stoppers



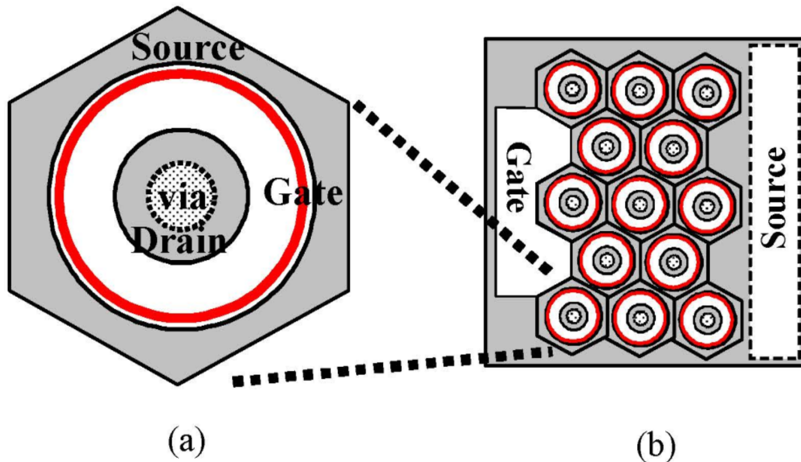


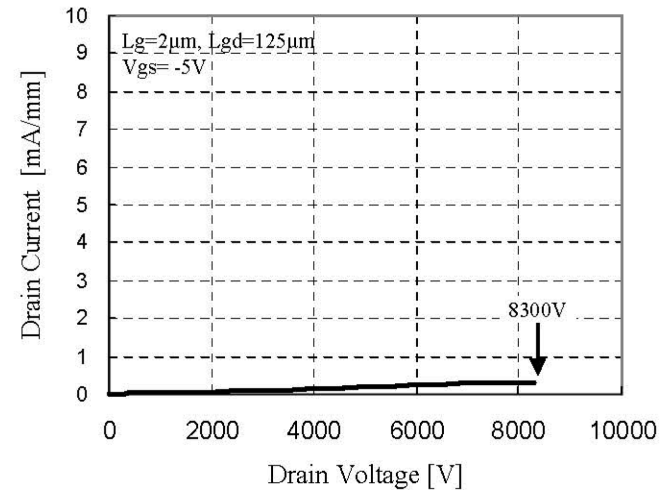
H. Umeda *et al*, in *Digest of IEEE IEDM*, pp. 480-483, 2010 – Panasonic paper

High-Voltage GaN HFETs



8300V, R_{sp} = 186 mΩ x cm^2





Y. Uemoto *et al*, in *Digest of IEEE IEDM*, pp. 861-864, 2007 – Panasonic paper

Current Status

Best Commercial SiC Devices:

1700V/25A Schottky Barrier Diode
1200V/33A MOSFET

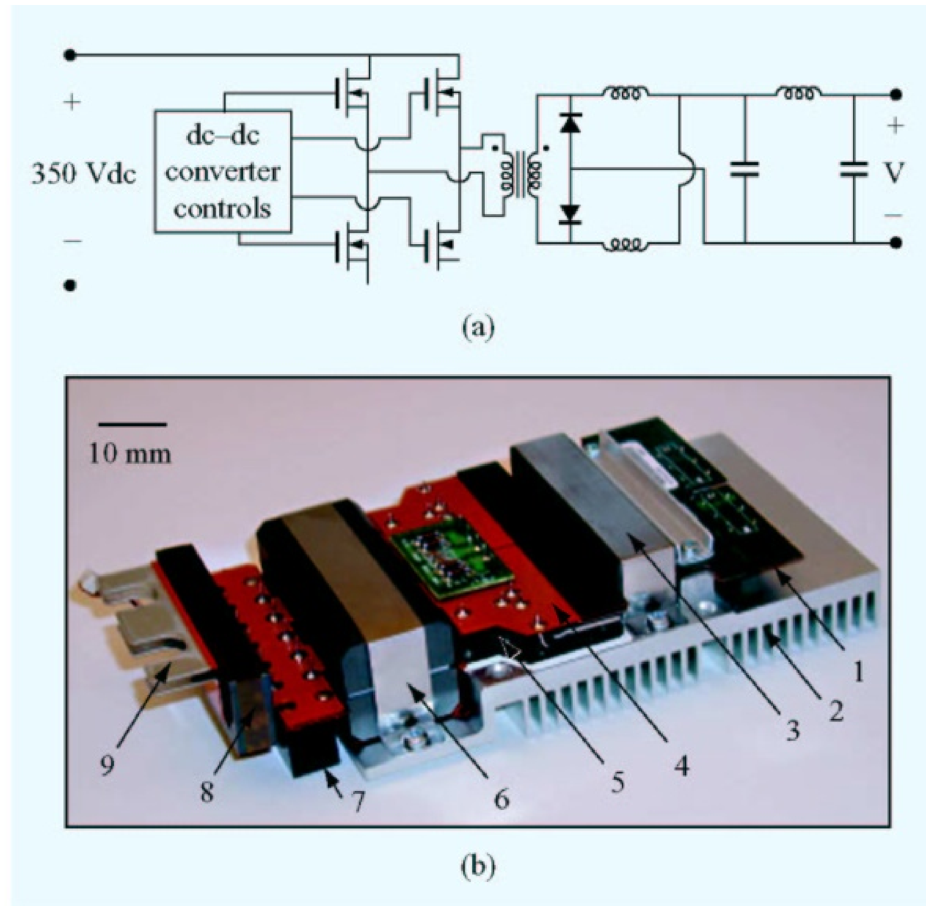
No Commercial GaN Power FETs

Too Expensive
Reliability Unknown

Power Semiconductor Switch Reliability

Lessons Learned from Silicon Power MOSFET Failures in High-Density Power Supply Field-Reliability Study

Power Supply Reliability Study



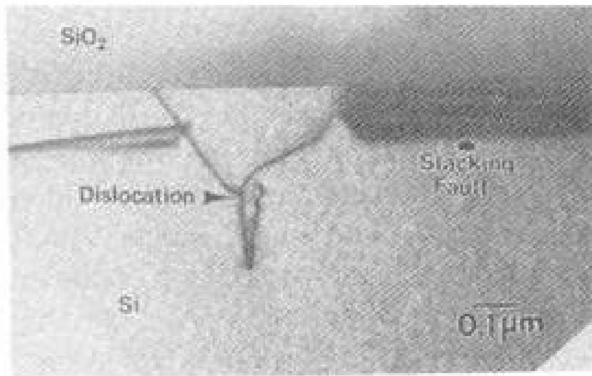
(a)

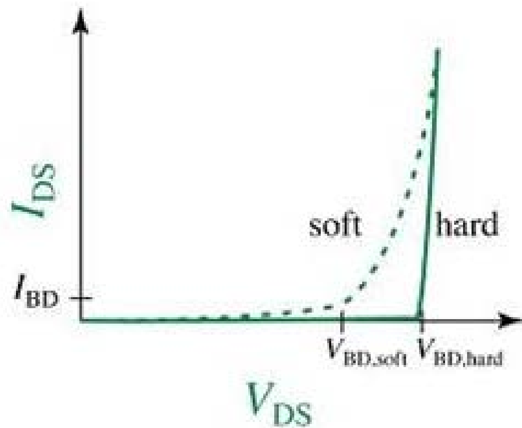
(b)

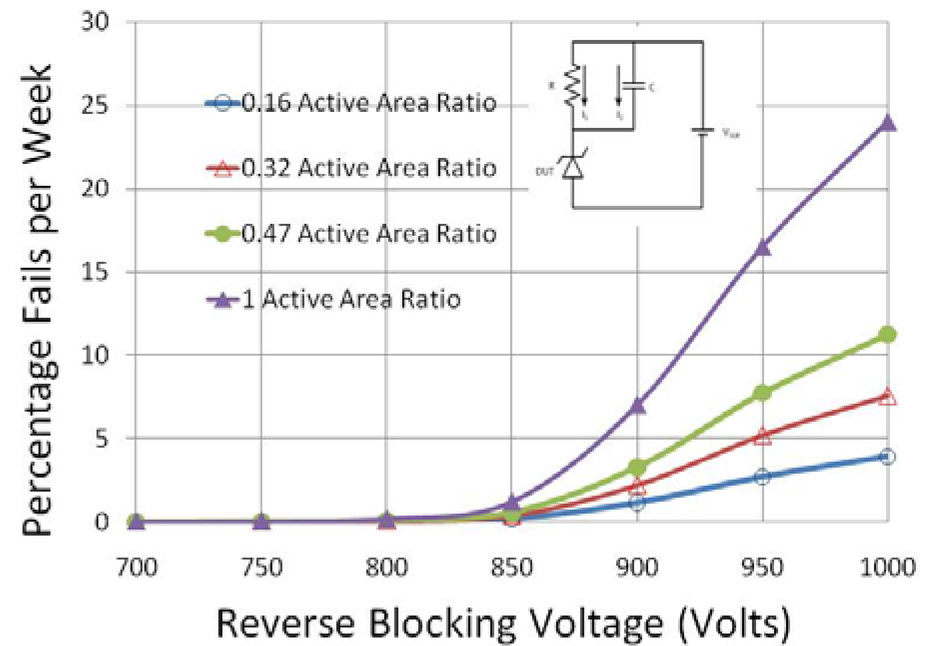
Field-reliability of computer/telecom power supplies was extensively evaluated to study the cause of power MOSFET failures.

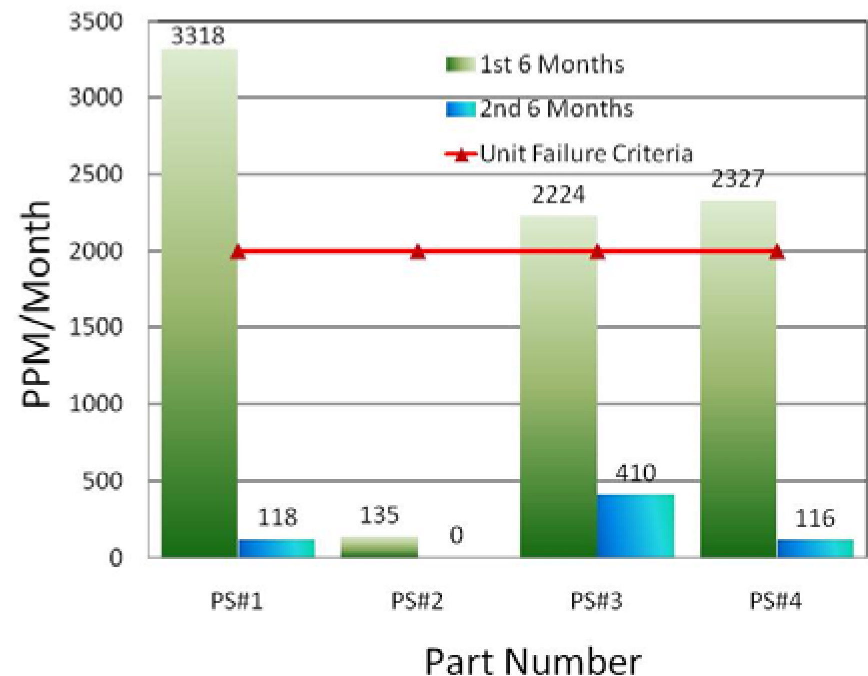
K. Shenai, *IEEE NAECON 2010*, Dayton, OH, July 2010

Material Defects Caused Field-Failures of Silicon Power MOSFETs



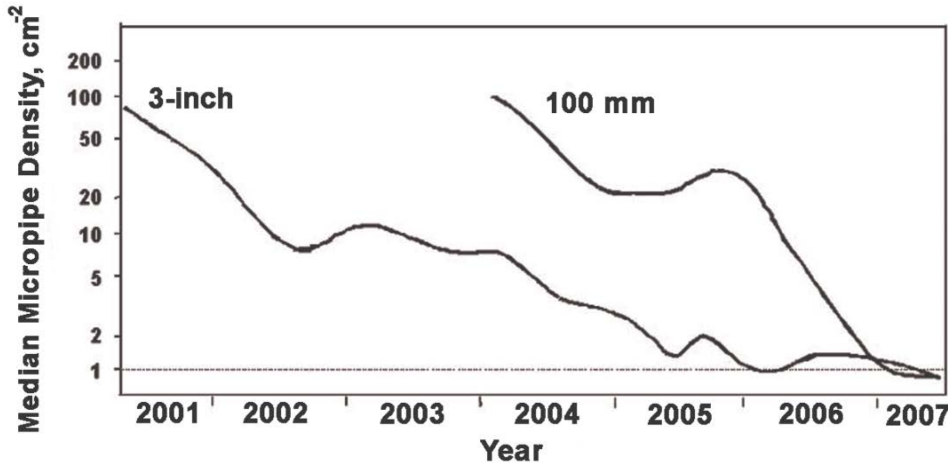




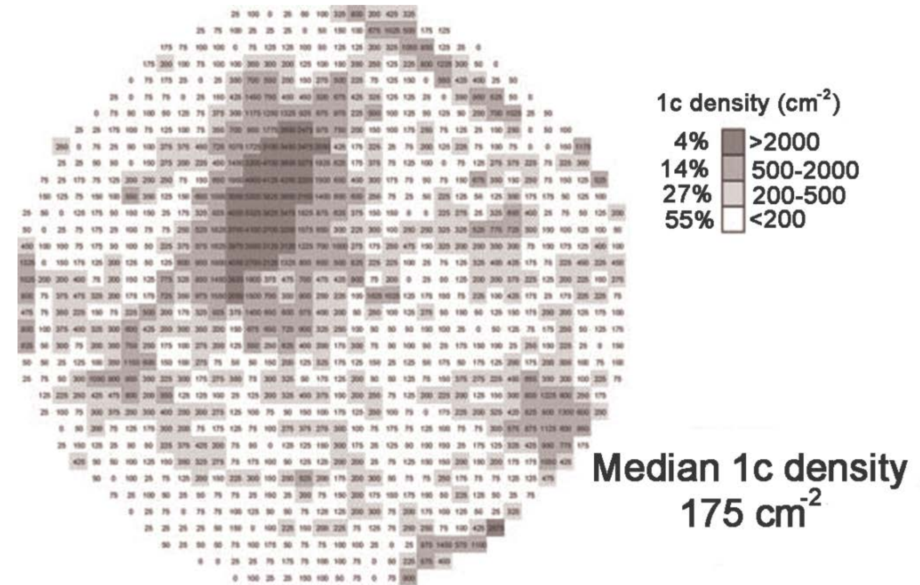


K. Shenai, *IEEE NAECON 2010*, Dayton, OH, July 2010

Current Status of Defect Density in Best R&D SiC Wafers



Nearly Zero (0.8 cm^{-2}) Micropipe Density in 4 inch Commercial SiC PVT Wafers - Expensive



Best Screw Dislocation Density in 3 inch R&D SiC PVT Wafers – Very Expensive

Leonard et al, *Mat. Res. Forum,* vols. 600-603, pp. 7-10, 2009 - Cree paper

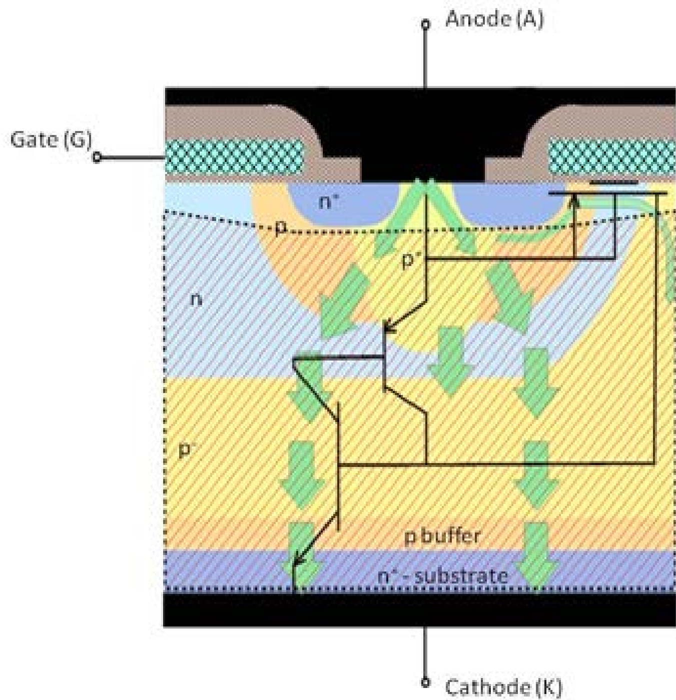
The best R&D SiC PVT wafers have a wide range of defect density from < 200 cm^{-2} to more than 2,000 cm^{-2}

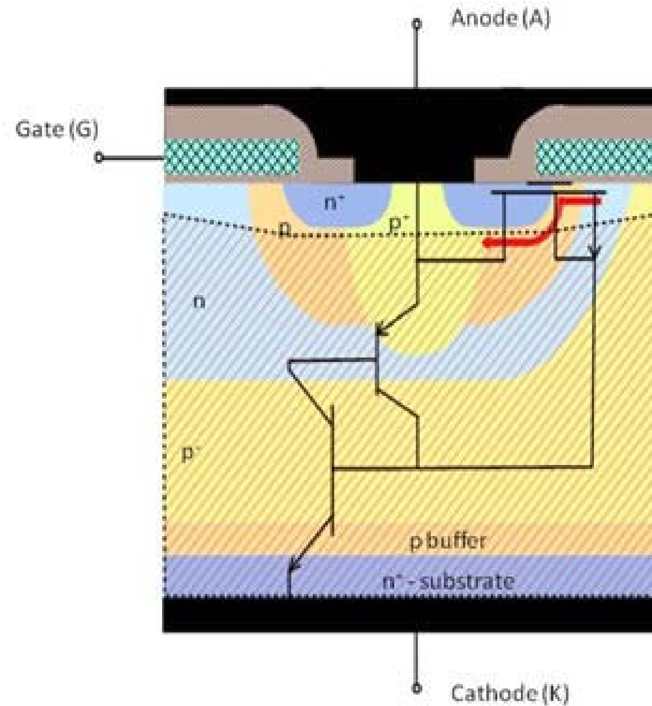
Carrier lifetime control is nearly impossible

The Key Question:

If silicon (with < 10 defects/cm^2) power MOSFET reliability is compromised by material defects, what is the reliability of power switching devices made on SiC (with > 10^3 defects/cm^2) or GaN (with ~ 10^7 defects/cm^2) ?

Turn-off Failures of Silicon MOS-Controlled Thyristors (MCTs)





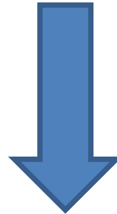
Plasma Constriction

Current Filamentation

Summary & Conclusion

To:

Reduce Cost & Develop Reliable Power Switch in SiC and GaN Semiconductors



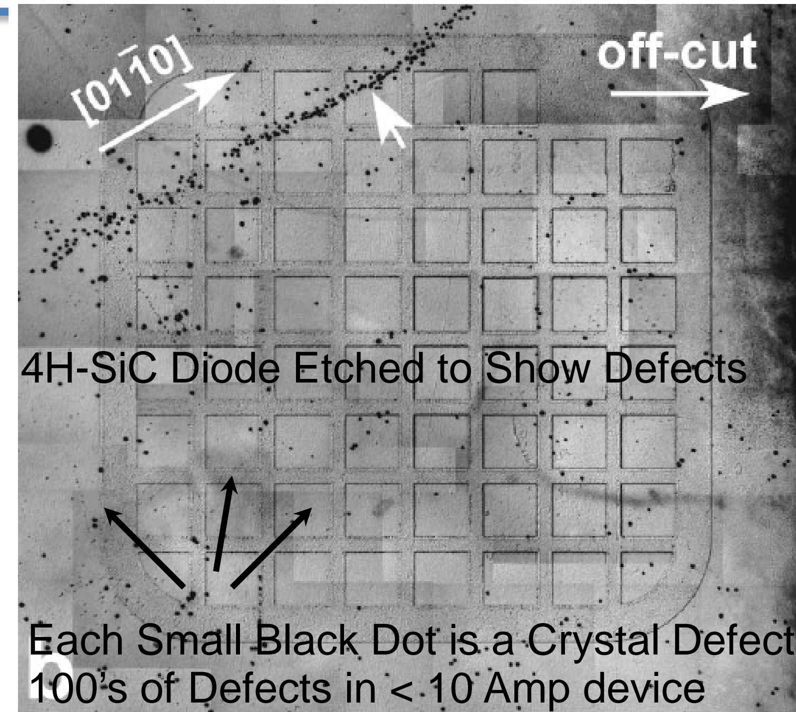
Material Defects & Structural Limitations Must be Eliminated

“Game Changing” Technology

Best 0.2 x 0.2 mm SD-free 3C mesa
(oxidized to map polytype and defects)

Defect-free SiC

Need Further R&D



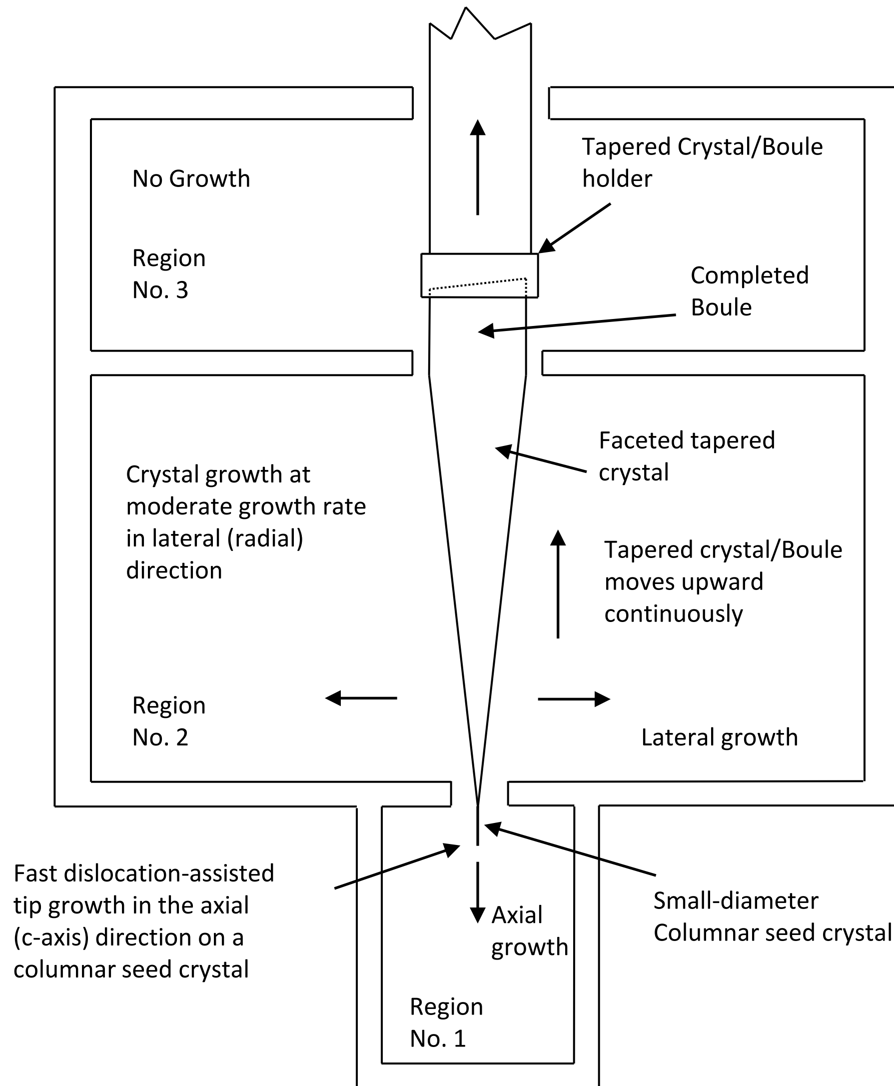
0.3 mm

- 4 in. dia. low-cost, low defect-density commercial wafers
- Robust high-performance devices
- Low-cost manufacturing
- 250C packaging and 300C sensors

LTC Game Changing Technology

Large Tapered Crystal (LTC) Growth Method for SiC (US Patent # 7,449,065B1)

Simplified Schematic Cross-Sectional Representation



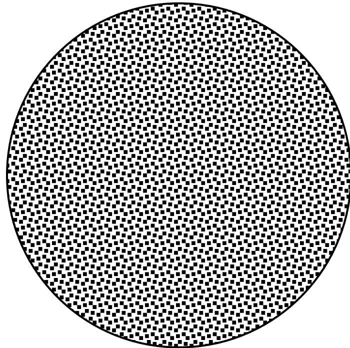
<u>Features (one embodiment):</u>

1. **3-Region growth apparatus for 3 different growth actions.**
2. **Region 1: Axial (c-axis) growth on a <u>very small diameter</u> columnar portion enables fast growth in the c-axis direction.**
3. **Region 2: Lateral (m-direction) growth at moderate growth rate on the tapered portion**
4. **Region 3: No growth after LTC boule reaches desired diameter.**
5. **Growth rate of boule in c-axis direction equals fast growth rate of columnar seed crystal.**
6. **Boule contains only one SD along its axis; the remainder of the boule is nominally defect-free.**

LTC Game Changing Technology

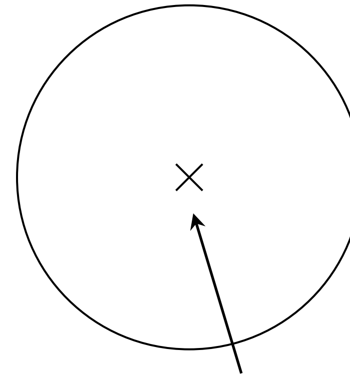
LTC Vision: **Dramatically improved SiC wafer quality realized at higher volumes and lower production cost.**

Present-Day SiC Wafer



~100-10,000 screw dislocations/cm^2
< 0.5 wafers per hour
Cost: > $2,000/4-inch wafer
Commercial Power Devices
Limited to < 50 A, ~1 kV

LTC SiC Wafer



< 1 screw dislocation/cm^2
> 1 wafer per hour
Cost: < $500 /6-inch wafer
Commercial Power Devices
100-1000 A, > 10kV

Drastic wafer improvement sufficient to unlock full SiC power device potential.
(Approach also applicable to 3C-SiC, GaN, Diamond, and other semiconductors)

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We can do it !

Any Questions ?