IS10.7 – Highly Thermally Conductive Epoxy Substrates as Ceramic Replacement with High Volume Manufacturing

Presenter: Prof. Doug Hopkins

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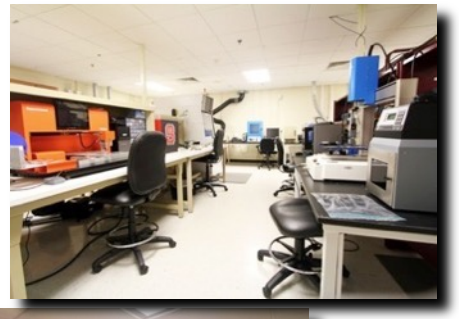

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* Planned summer 2022 graduation

Why Organic Substrates?

- Lower material costs
- Tapping high volume PCB manufacturers for panel-level processing
- New ultra thin ERCD dielectrics (120µm vs 635µm) provide higher thermal 'conductance' compared with Al_2O_3 (Alumina) ceramic
- Multilayering for direct Common Mode management
- Higher levels of integration with more components on "cheaper" real estate
- Design like designing PCBs
- Enables integrated baseplate with IMS (Insulated Metal Substrate)
  - Great IMS process description: https://www.ncabgroup.com/wp-content/uploads/2015/10/07-NCAB_Group_Seminars_IMS_2_0_150930.pdf

OUTLINE

- Organic Substrate Material Characteristics
- Example Application: 600V/25A PV Dual SiC BiDFET Inverter Module
- Example Application: 400V/6kW Fast Charger GaN Module
- Example Application: 6,500V/100 HV SiC Super Cascode Power Switch

The Power Electronic Substrate: Ceramic vs Organic

Technical Drivers

ENERGY FORMS

ELECTRICAL

- *(pF/mm²)•µm Inter-Conductor **Cap**acitance*
- kV/mm Breakdown Voltage
- µA/kV Partial Discharge*

THERMAL

- *(W/°C)/mm² Thermal 'Conductance', **λ***
- °C Max operating temp (T_g)

MECHANICAL

- *Modulus, **E*** (HDT)*
- Brittleness / Ductility
- ….,e.g R2R processing

**Reliability Drivers*

Partial Discharge → Graceful Aging

Modulus → Stress Failure

Cost Drivers

Material Cost → Supply Chain

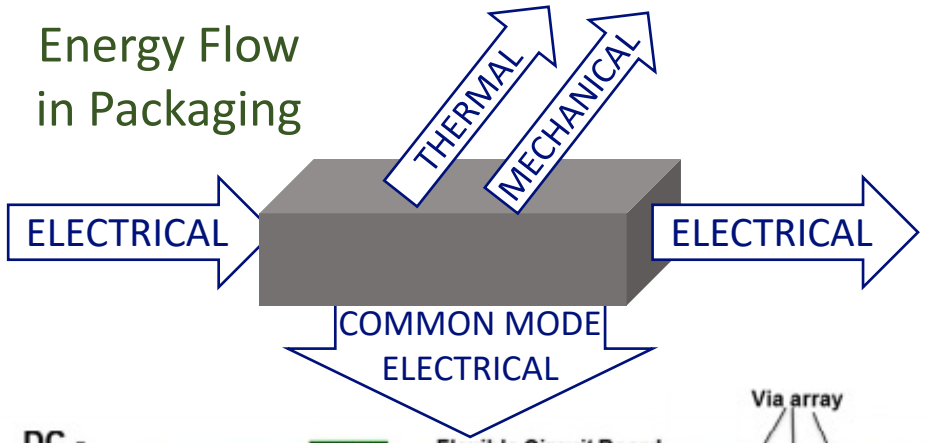
Processing Cost → Panel Size

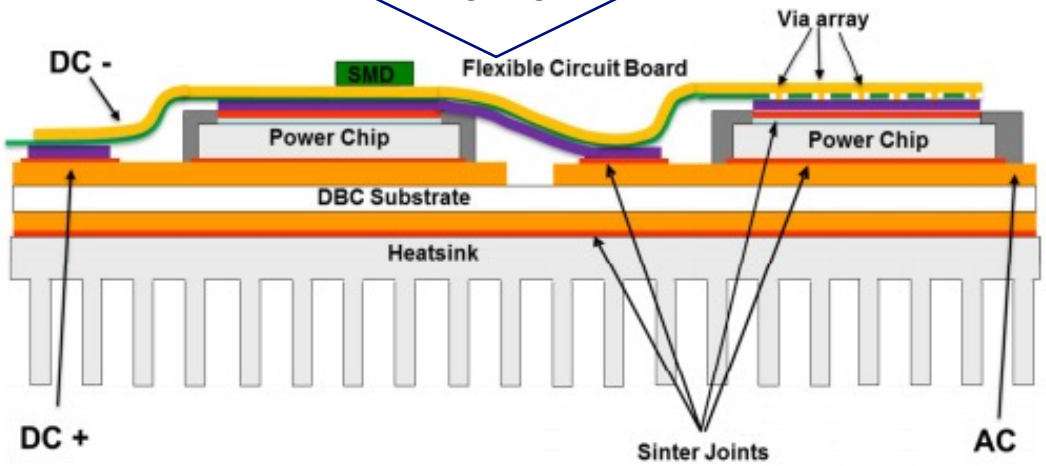
Substrate Impact on Design

	CERAMIC		POLYMER	
	Al_2O_3, Si_3N_4, AlN	Al_2O_3 Ribbon	POLYIMIDE	EPOXY
Cap	+++	-	-	-
BV	++	+++	-	+++
PD	++	?	+	++
λ	+	+++	-	+++
Max T°	+++	+++	--	++
E	-	+	+++	+++
$-Mat'l	--	?	+	++
$-Proc	---	?	+++	+++

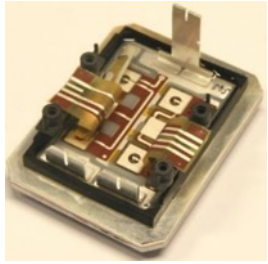
Electrical Opportunity for Organic Substrates

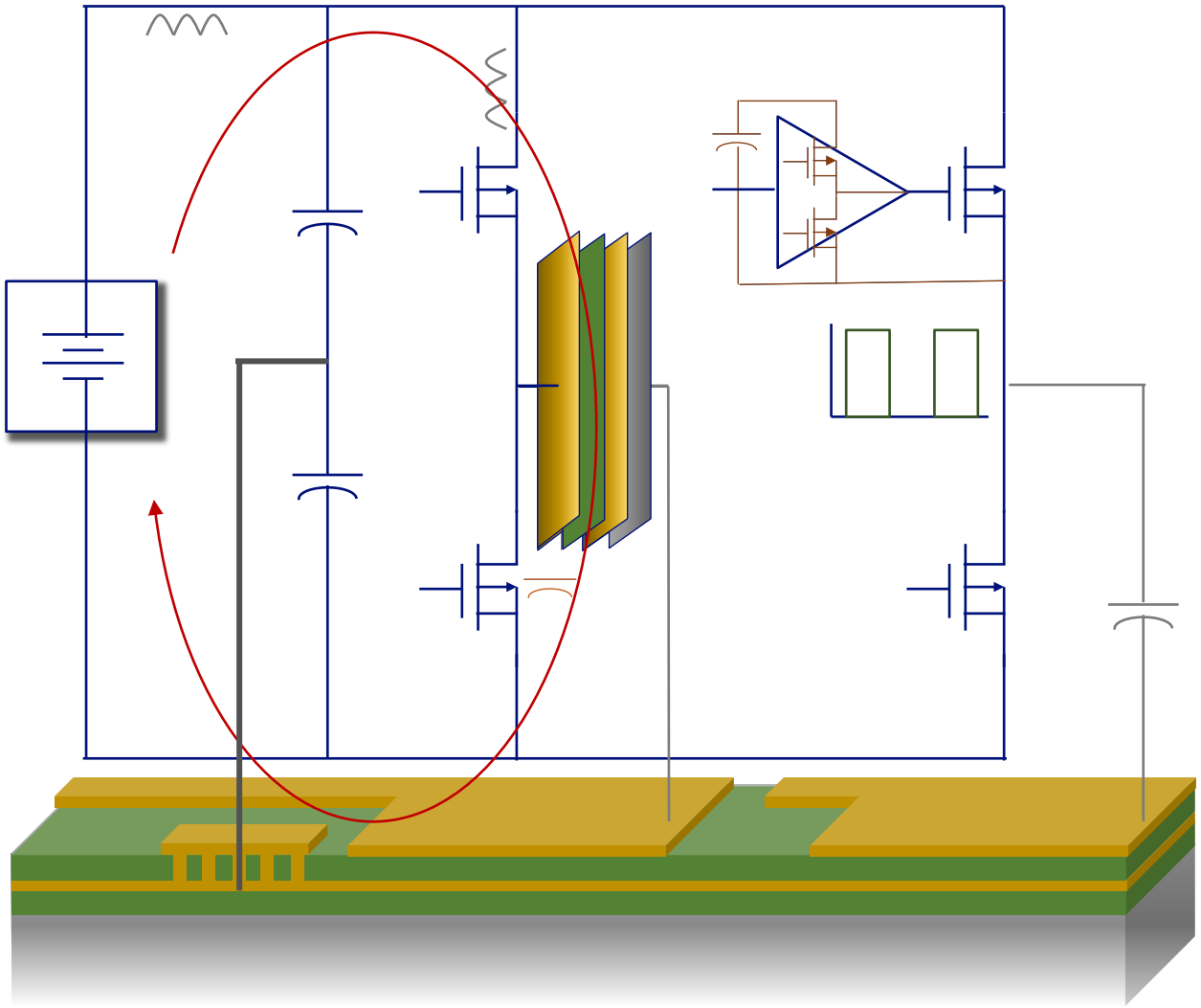
MODULES ARE A FIVE PORT NETWORK





Semikron SKiN module [1]





[1] S. Hauser. Direct Pressed Die Technology: Increased Power Density and Reliability in Standard Power Module Packages. APEC 2017, Tampa, FL.

Organic Substrate Material Characteristics

Epoxy Resin Composite Dielectric Substrate Mat'l Syst

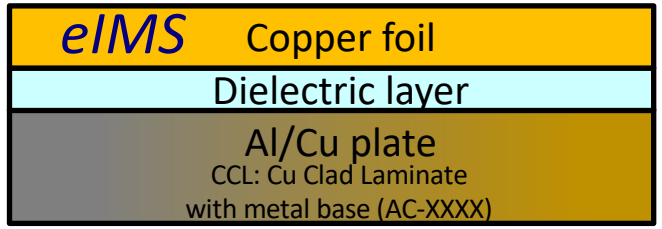
US Rep: Yoshi Fukawa, TechDream, Inc.<yoshi@tech-dream.com>

RISHO
Risho Kogyo Co., Ltd.

Glass Reinforced		Thermal Conductivity k	Non Glass Reinforced		
CCL [CS]	**Prepreg [ES]**		**Al/Cu Base CCL [AC / CC]**	**Bonding Sheet [AD]**	**RCC [CD]**
Copper Foil Woven Glass Cloth Reinforced Insulation Layer Copper Foil	Insulation *Layer* *B-Stage* *Woven Glass Cloth Reinforced*		Copper Foil Insulation Layer Copper PLATE Aluminum	Release Film Bonding Layer B-Stage Release Film	Copper Foil Bonding Layer B-Stage Release Film
$R_{th} = 1/k * l/A$					
		10 W/mK	80um – 120um AC/CC-7210N	80um – 120um AD-7210N	80um – 120um CD-7210
		8 W/mK	80um – 120um AC/CC-7208		80um – 120um CD-7208
		5 W/mK	80um – 120um AC/CC-7200TY	80um – 120um AD-7200TY	80um – 120um CD-7200TY
60um – 1600um CS-3295	60um – 100um ES-3245	3 W/mK	80um – 120um AC/CC-7303	80um – 120um AD-7303	80um – 120um CD-7303
		2 W/mK	100um AC/CC-7302		100um CD-7302
60um – 1600um CS-3945 (1.3W/mK)		1 W/mK	60um – 100um AC-7900		

CCL: Cu Clad Laminate
AC/CC: Al / Cu Clad
AD: Bonding Sheet
RCC: Cu Clad Release Film

ERCD: (10W/mK) Properties & Price Comparison

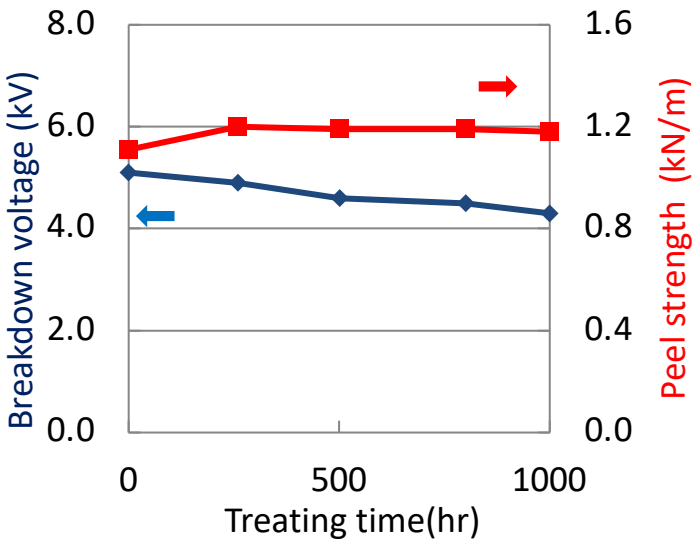


PROPERTIES RISHO

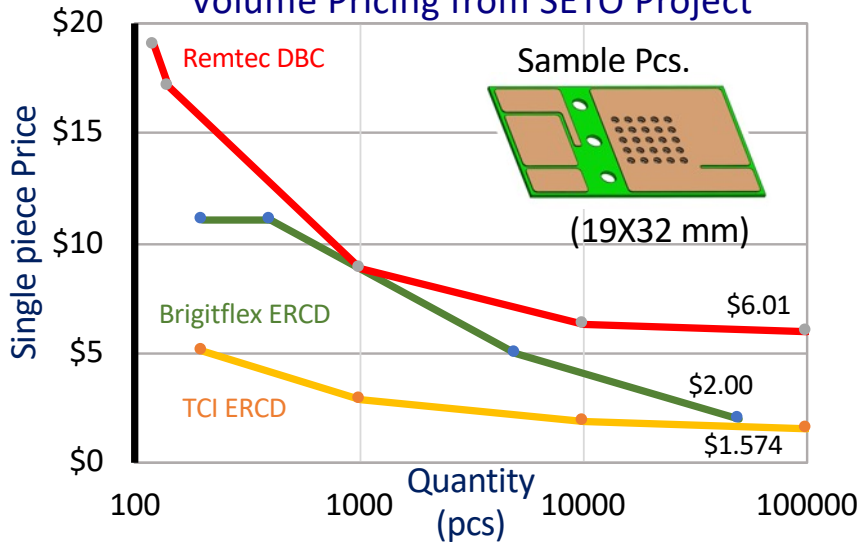
Product number	RISHO: AC-7210	
Dielectric layer thickness	120µm	
Thermal conductivity（W/mK）	**10**	Laser flush method
Tg（℃）	**270**	DMA method
Peel strength（kN/m）	1.2	1 oz copper
Solder limit（sec）	60＜	260℃
CTE（ppm/℃）α1	14/14/14	X/Y/Z
Breakdown V（kV_{ac}）(50/60Hz)	**> 5**	JIS C2110 (ASTM-D149)

http://www.risho.co.jp/english/product/products0/index.html

High temp long term reliability(175℃)



*Volume Pricing from SETO Project



PCB MFGR'	ADDRESS	PANEL SIZE
TCI (Taihong Circuit Ind. Co., Ltd.)	No.81, Guangfu Rd., Hukou Township, Hsinchu County 303, Taiwan (R.O.C.)	20"x24" (510x610 mm)
Aurora	2250 White Oak Circle, Aurora, IL 60502	
Amitron	2001 Landmeier Road | Elk Grove Village, IL 60007	18"x24"
Brigitflex	1725 Fleetwood Drive, Elgin IL 60123	21"x41"
Electronic Interconnect	2375 Estes Avenue, Elk Grove Village, IL 60007	

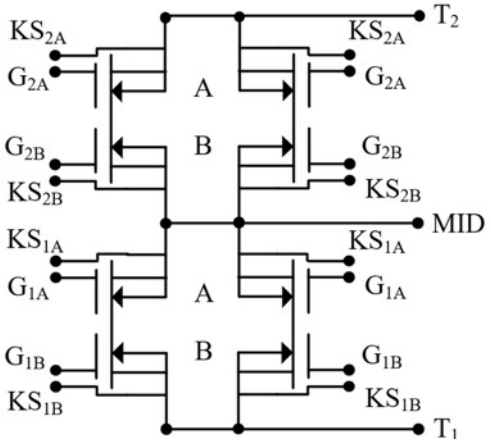
Example Application:
600V/25A PV Dual-‘SiC BiDFET’ Inverter Module

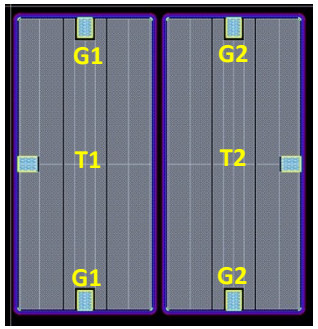
This research is funded by the Solar Energy Technologies Office (SETO) within the Office of Energy Efficiency & Renewable Energy (EERE) at the Department of Energy (DoE) of the U.S. Government under the Grant DE- EE0008345.

PV Inverter Systems w/ Monolithically Integrated SiC Bi-Directional FET (BiDFET)

Demonstrate a Cyclo-Converter based 1-phase grid connected PV inverter using 1200V/25A BiDFETs and advanced packaging of dual-switch modules.

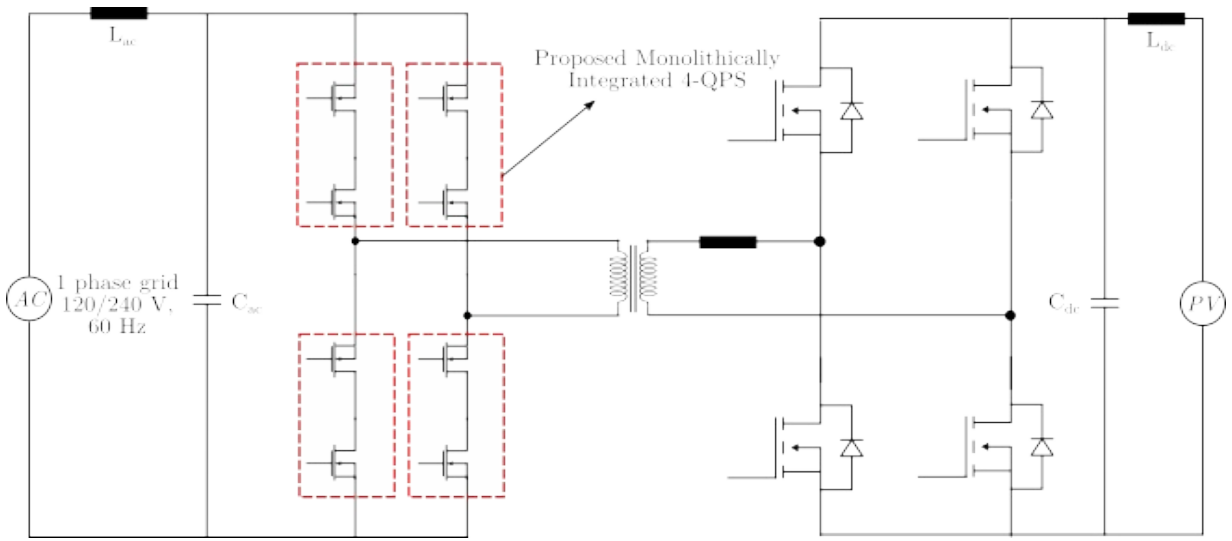
(Sponsor: Solar Energy Technologies Office – US Dept of Energy)

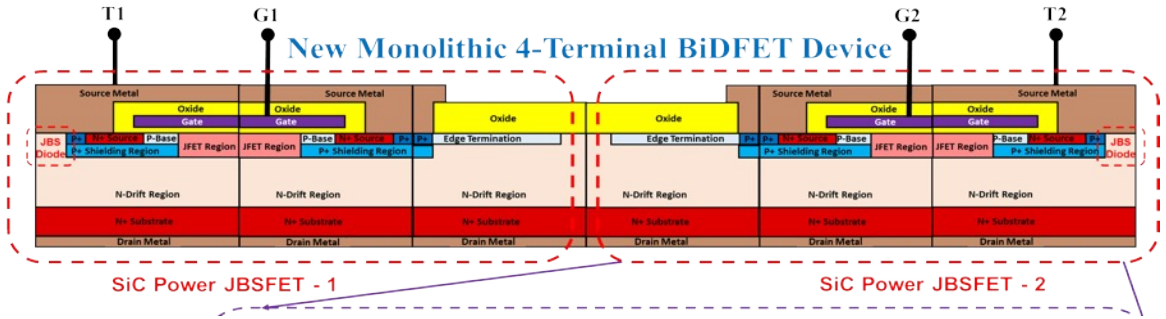




BiDFET Switch

Two BiDFETs per Switch, ½-Bridge Module





SiC Power JBSFET Structure: Power MOSFET with Integrated Schottky (JBS) Anti-Parallel Diode

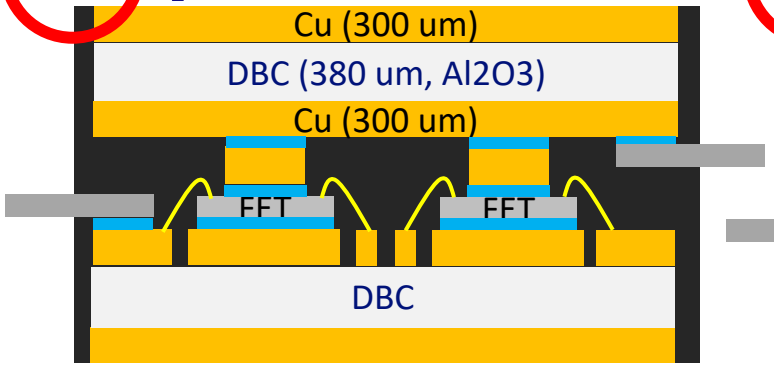
Principal Investigators: Subhashish Bhattacharya; Jayant Baliga, Douglas Hopkins

Other Contributors (PhD students): Ajit Kanale, Tzu-Hsuan Cheng, Isaac Wong, Ramandeep Narwal; (Post-Doc scholars): Aditi Agarwal

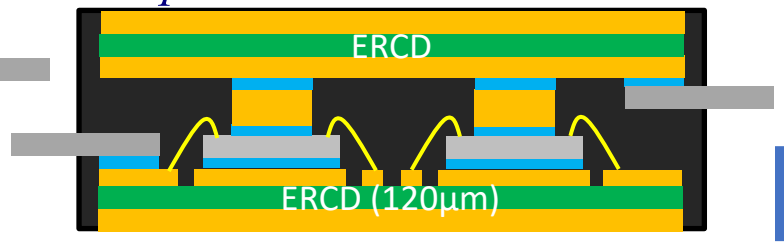
Comparison DBC vs ERCD –

Mechanical and Thermal Performance

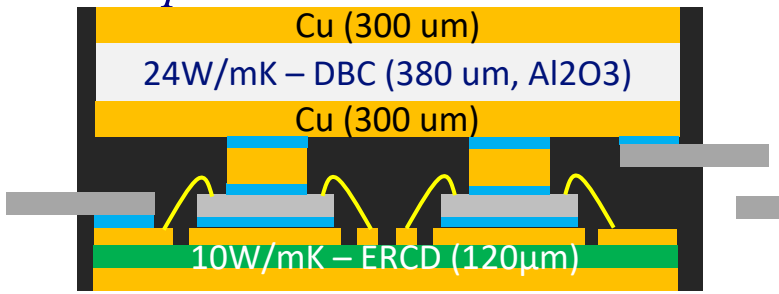
D/D *Top: DBC / Bottom: DBC*



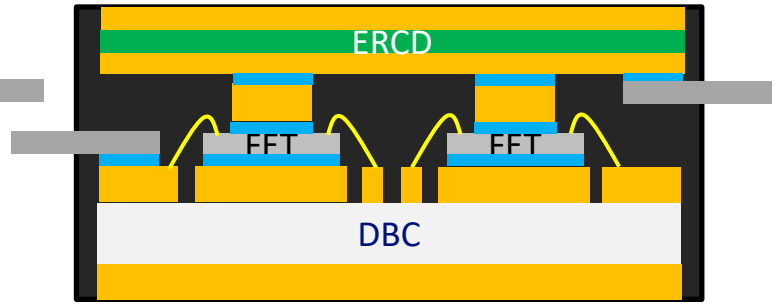
E/E *Top: ERCD / Bottom: ERCD*

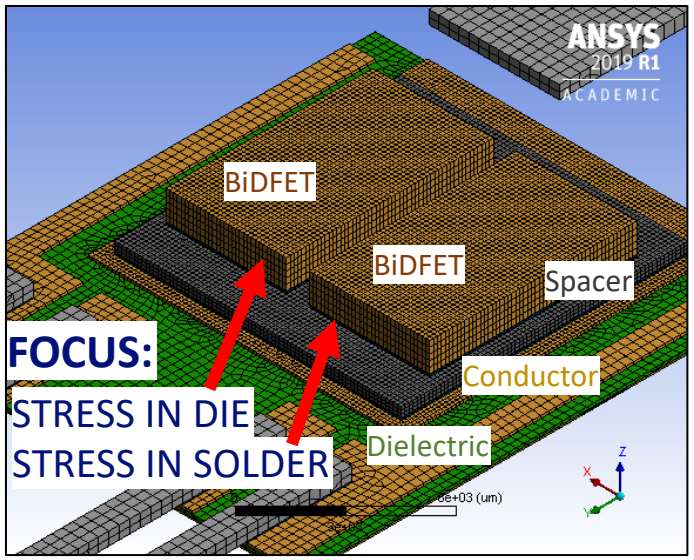


D/E *Top: DBC / Bottom: ERCD*



E/D *Top: ERCD / Bottom: DBC*

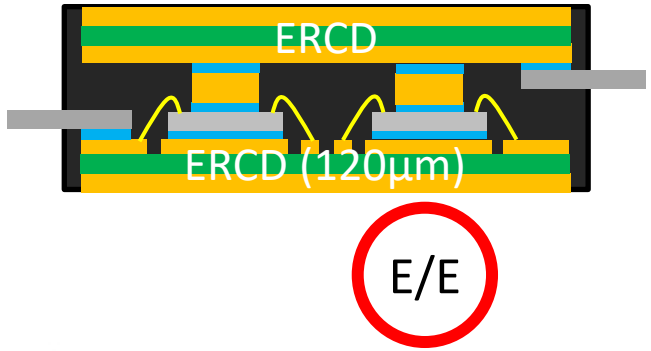


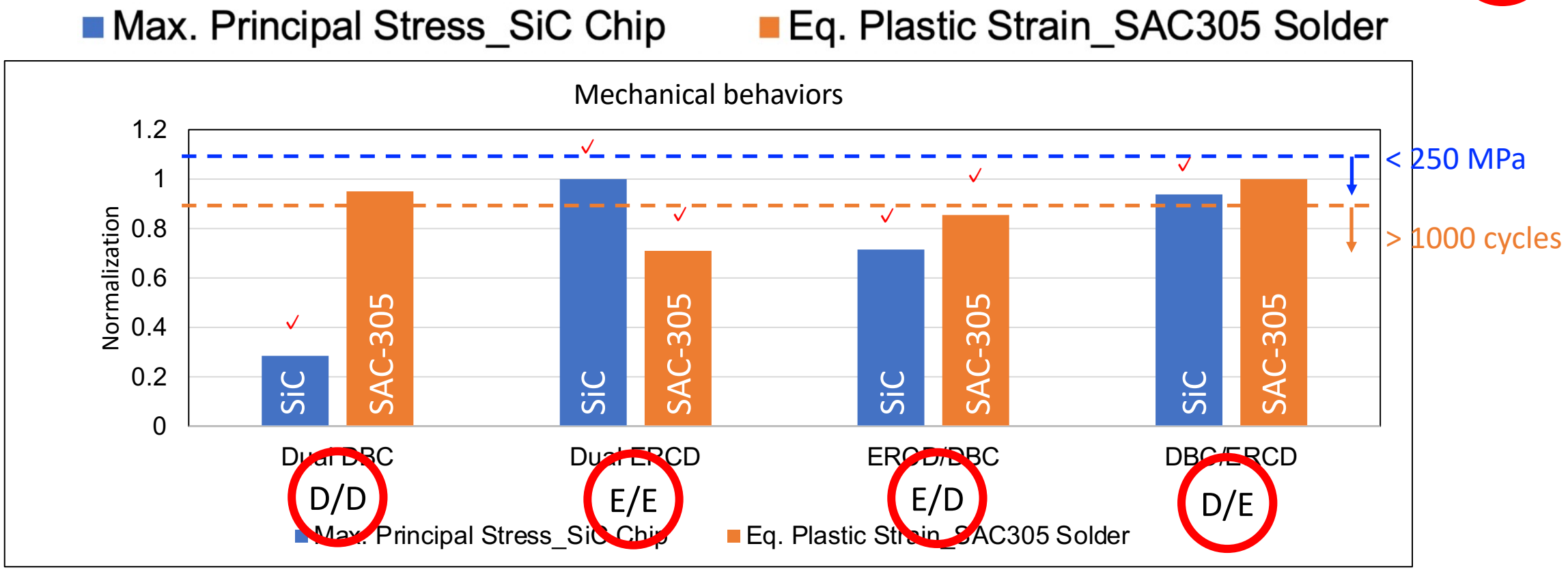


Device	Material	Thickness (mm)	Modulus (GPa)	CTE (ppm/°C)	Thermal (W/mK)
BiDFET	4H-SiC	0.36	347	4.5	380
Spacer	Cu	1	110	17.6	398
Conductor		ERCD: 0.07 DBC: 0.3			
Solder	Sn5/Pb92.5/Ag2.5	0.1	13.8	28.9	36
	Sn95/Sb5	0.1	50	22.8	46
	Sn96.5/Ag3/Cu0.5	0.1	38.7	21	60
Dielectric	ERCD	0.12	30	14	10
	Al2O3	0.38	310	6	24
Molding	2-Pack type (Epoxy + Hardener)	Duals: ERCD 2.2; DBC 3.4	15	16	3

ThermoMechanical Reliability: Solder & Die Stresses

- ERCD/ERCD & ERCD/DBC pass failure criteria for solder and SiC.
  - *Although "dual DBC" offers best reliability of SiC device due to low CTE mismatch between Al_2O_3 and SiC, the high modulus of Al_2O_3 (310 GPa) can cause high stress/strain on SAC305 solder layer.*

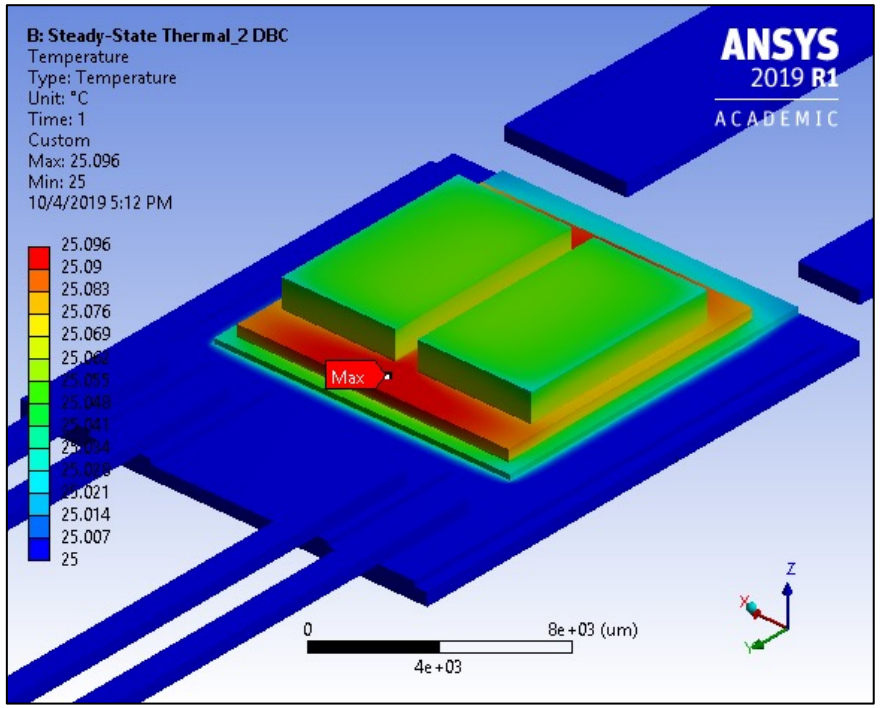




Thermal Analysis (Steady-State)

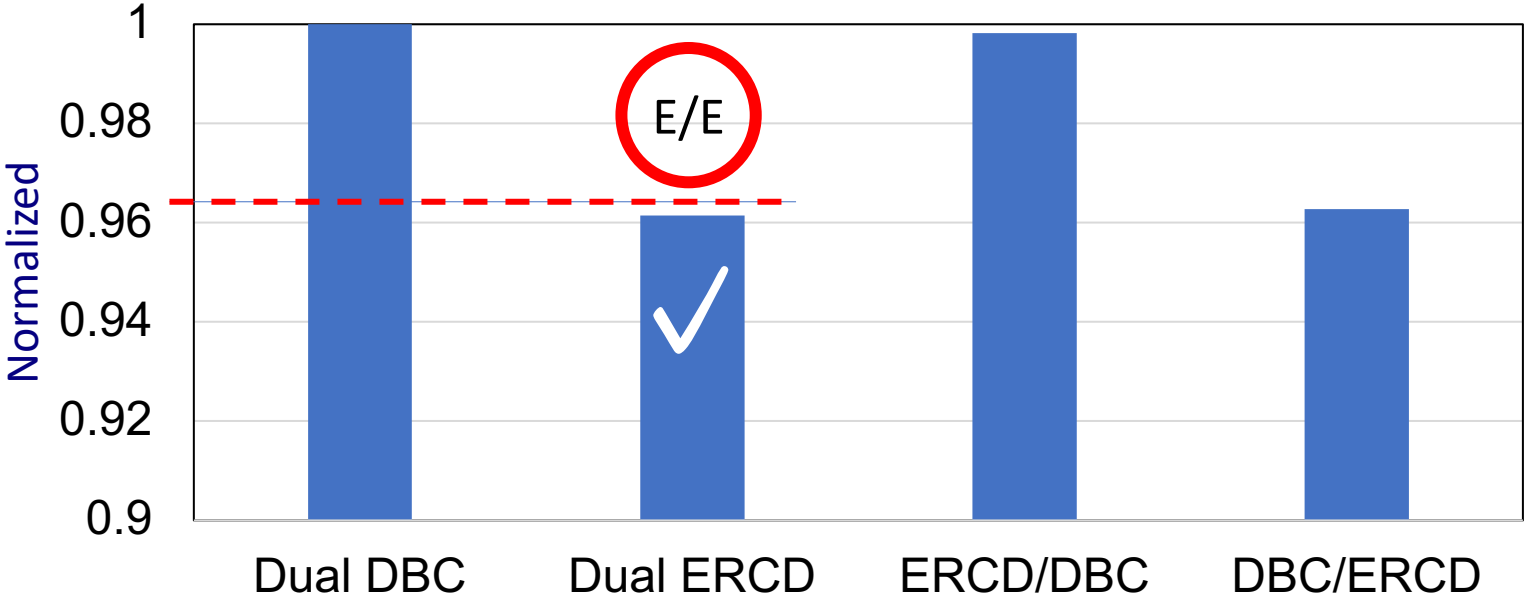
- Boundary conditions:
  - ✓ Infinite heat transfer on top and bottom exposed Cu pads
  - ✓ Heat sources on die top surface
- Thermal resistance:

$$R_{jc} = \frac{T_{j,max} - T_c}{P}$$



FROM SIMULATION

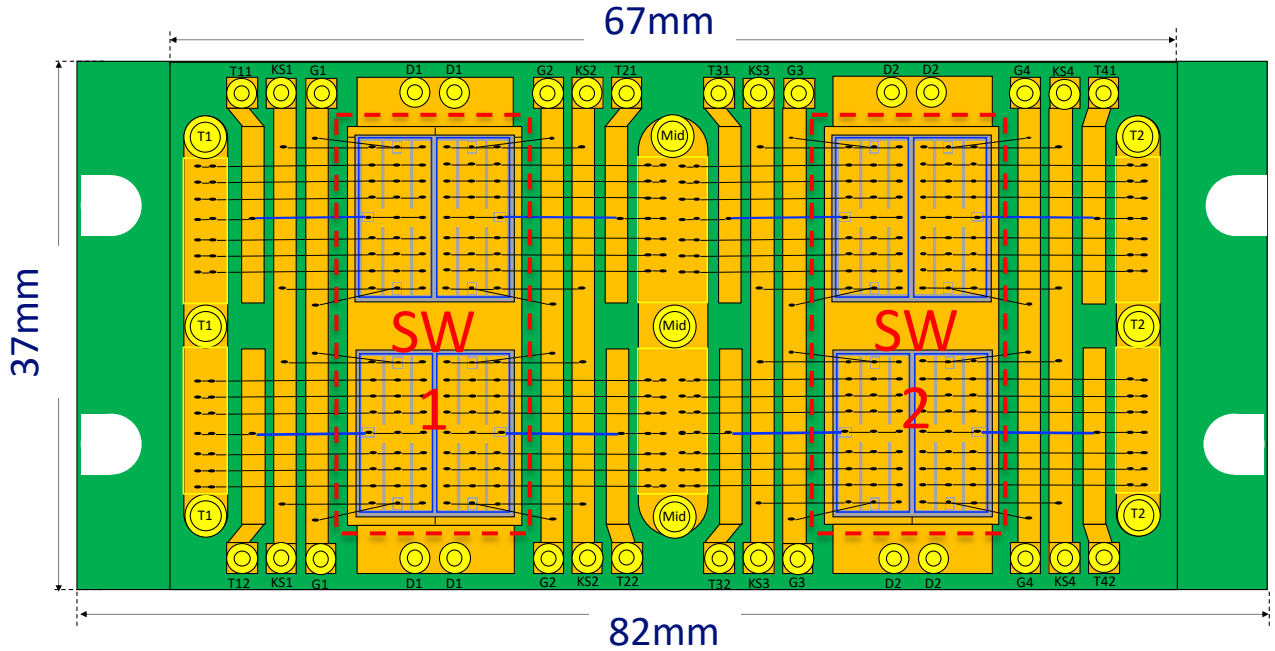
Thermal resistance junction-to-case (Rjc)

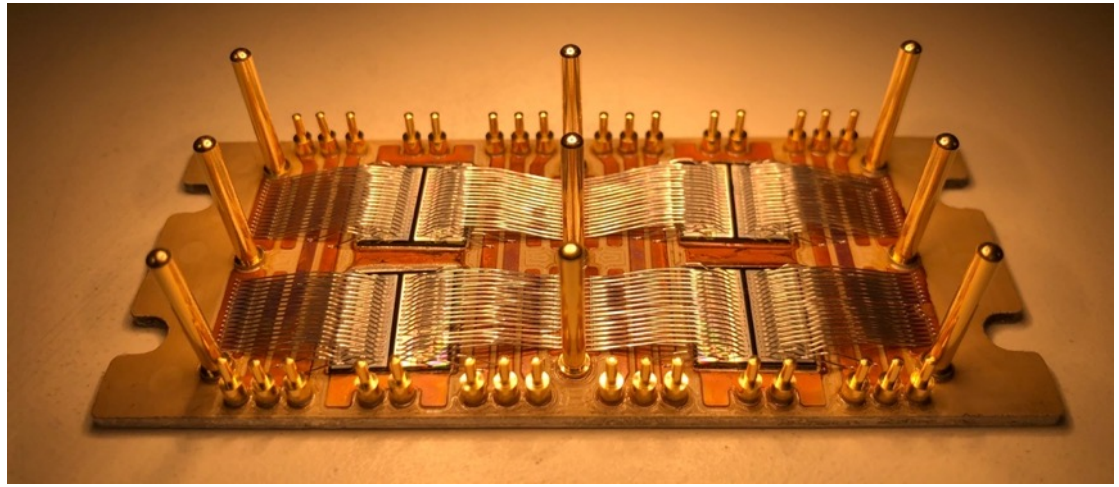


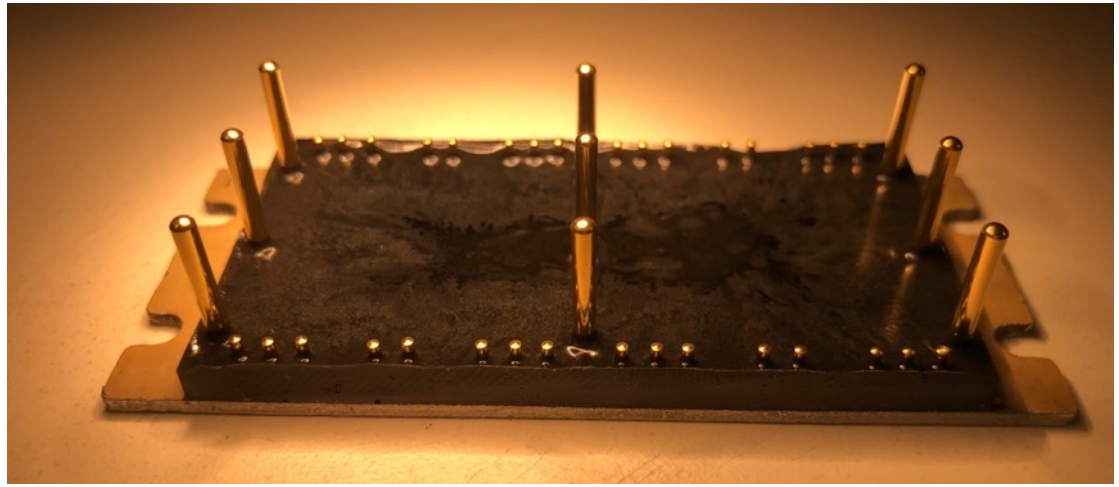
The advantage of ERCD material not only provides a competitive thermal and mechanical performance, but also a cost-effective solution for the advanced power module.

Single-Side Cooled Parallel BiDFET Half-Bridge Module

- 1200V/25A module: ERCD–IMS with 2mm baseplate, 120µm ERCD and 2oz Cu
- Two BiDFETs are connected in parallel and two switches connected in a half-bridge.
- To minimize parasitic resistance and inductance in the power loop, 20-mil stitched Al wires are bonded on each JBSFET.
- The SMD signal pins and THD power pins assist alignment for mounting the module on PCB.

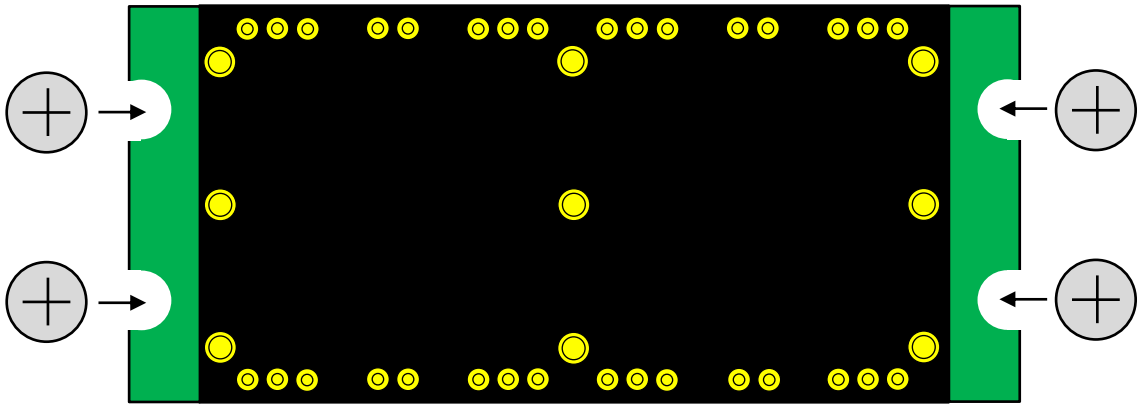


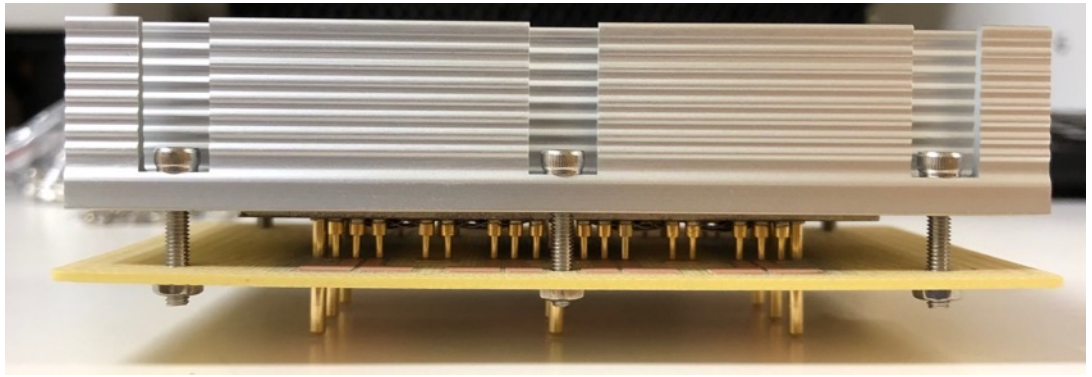


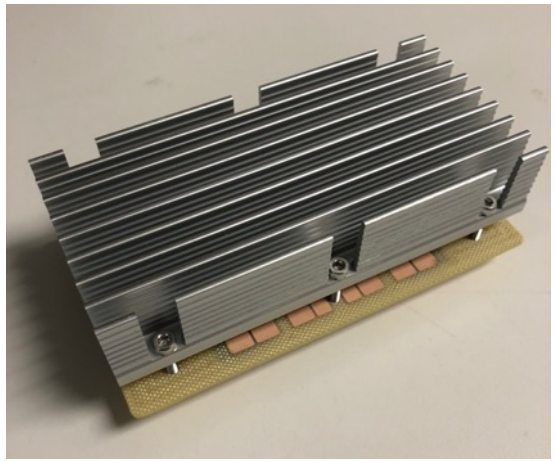


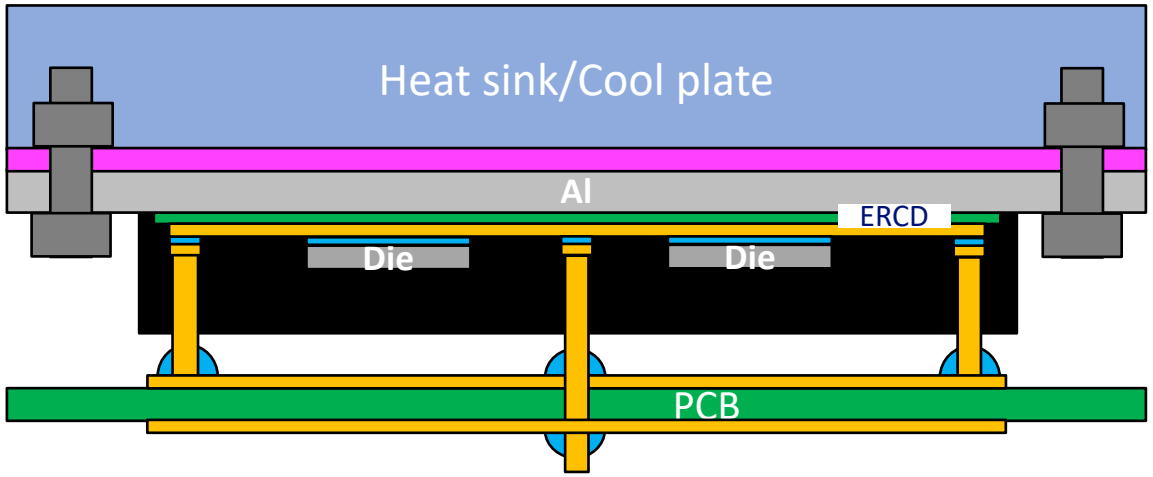
Single-Side Cooled Parallel BiDFET Half-Bridge Module

The *eIMS* provides the heat-sink & mounting plate, and provides a convenient platform for paralleling multiple modules, e.g. for a three-phase inverter.



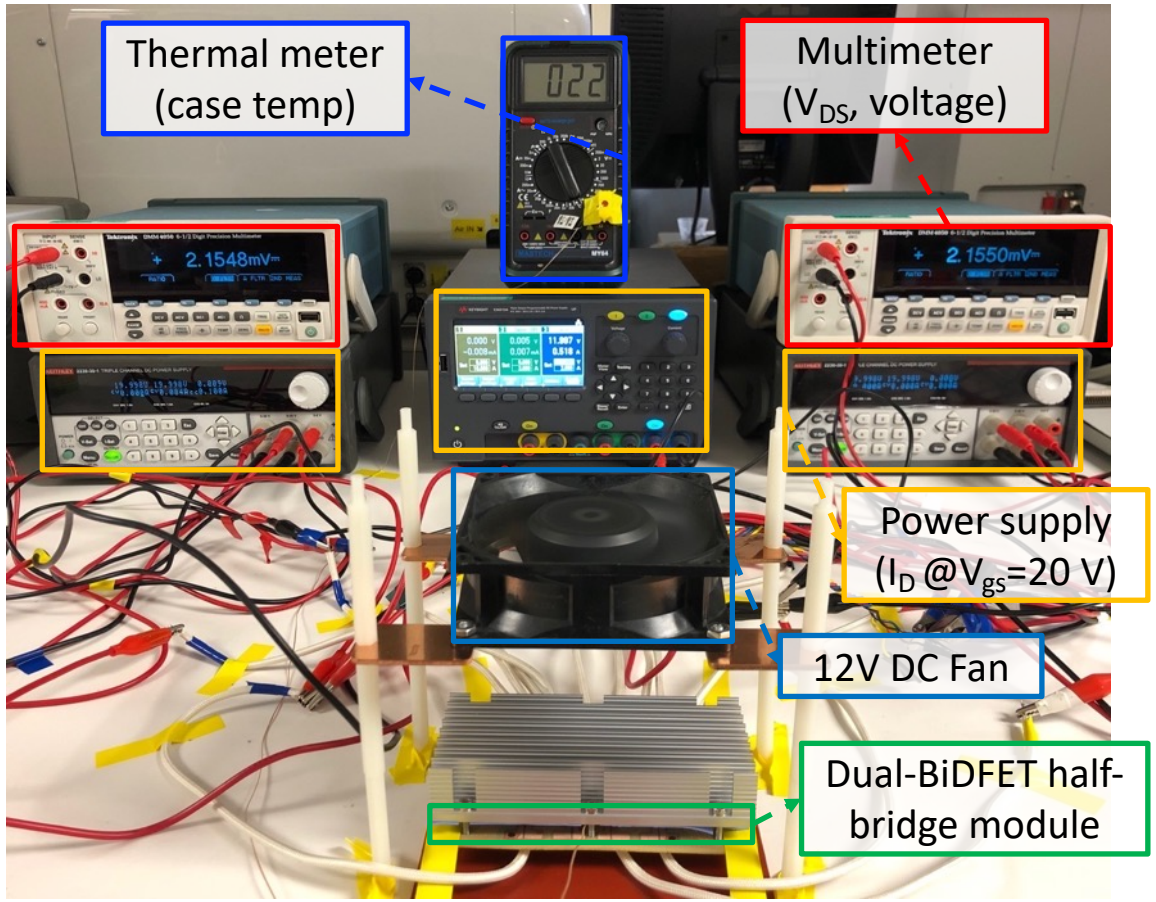




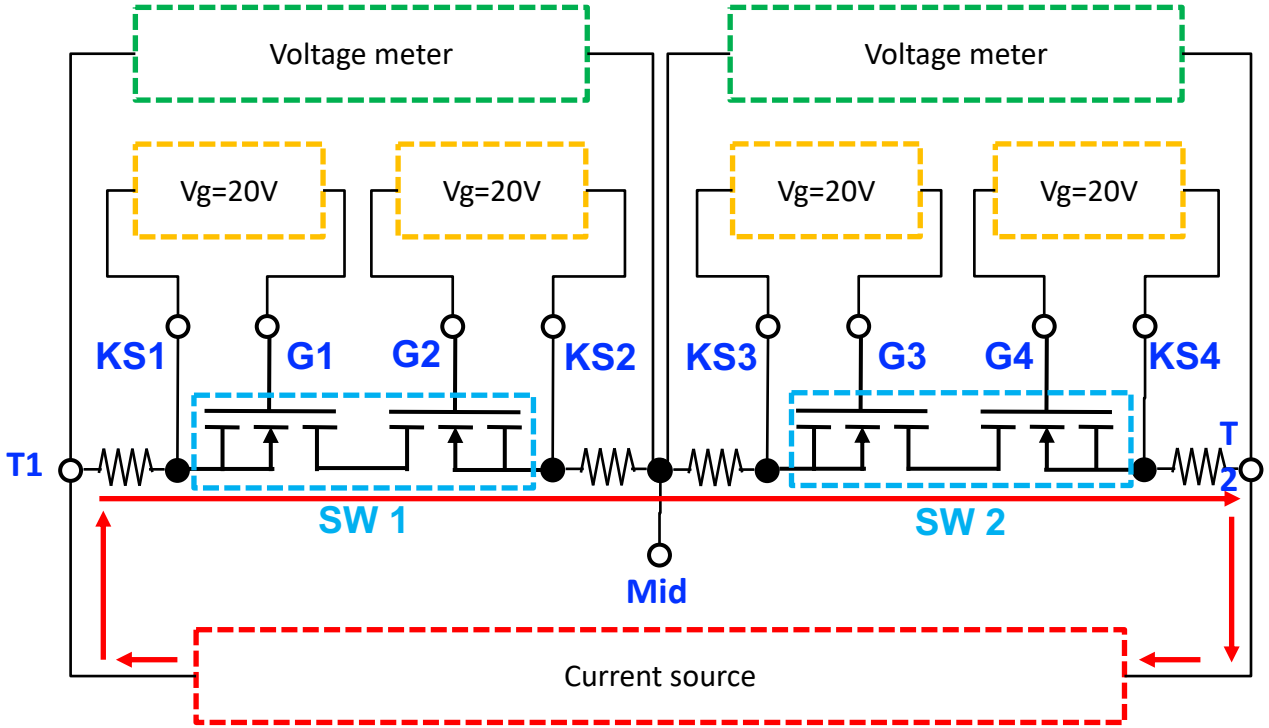


Experimental Thermal Characterization

The case temperature was captured by thermocouple located at the center of the case (bottom surface of the eIMs) for not blocking heat transfer under the die. A 6 W/mK thermal pad with a thickness of 0.5 mm was placed between the module and the heat sink. A 12V DC fan was mounted on the top to ensure a uniform cooling for four BiDFET devices. The figure below demonstrates the test setup and all equipment.



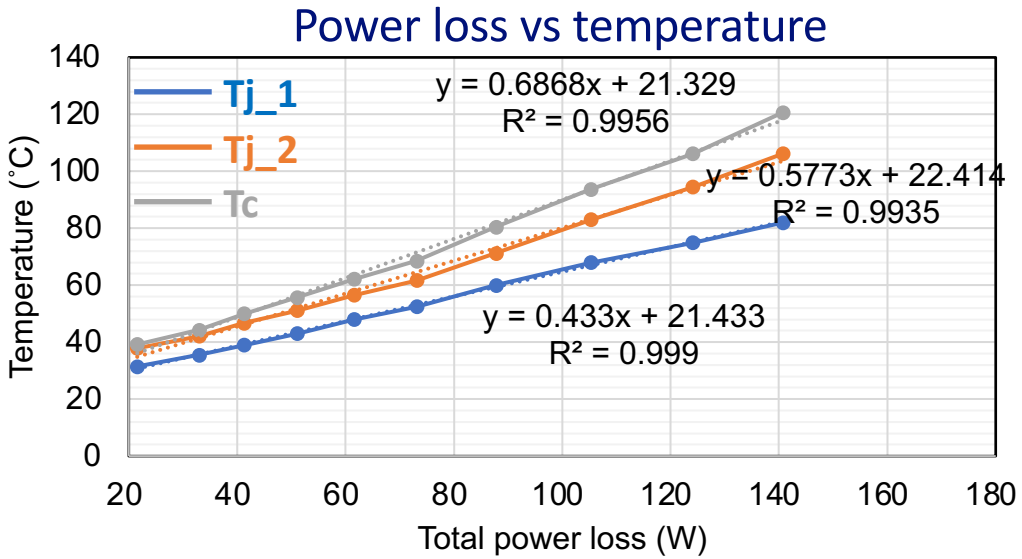
To characterize the max. current (current capability) and max. power of the module, a thermal experiment was carried out. The module was self-heating by inputting known DC current through T1 to T2 terminal. The voltage drops across T1 to Mid (SW1) and Mid to T2 (SW2) were measured by Kelvin connection method.

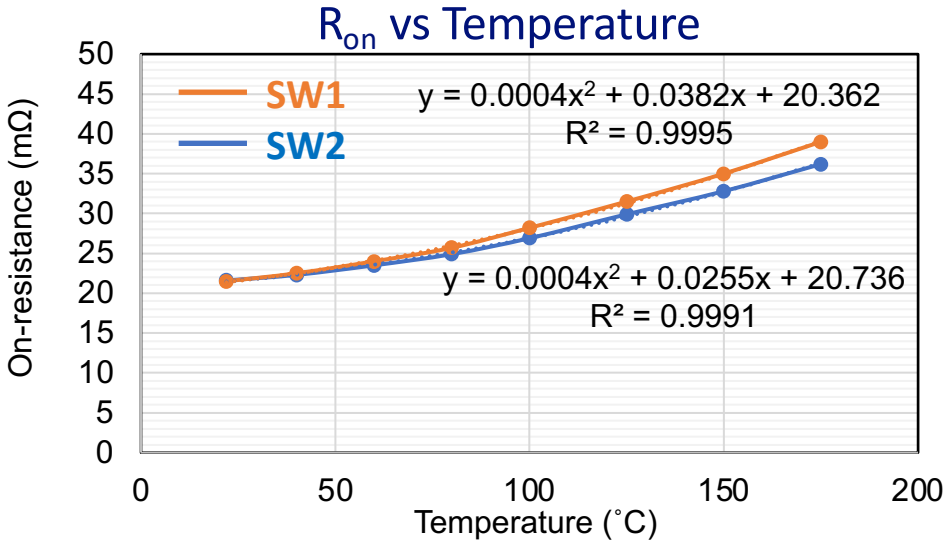


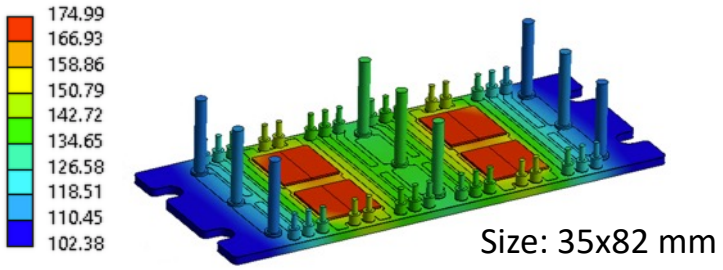
Experimental Thermal Characterization – Power & $T_{j,max}$

- Voltage drops across T1 to Mid and Mid to T2 are captured by Kelvin connection. The Tj and power loss on each switch is given in the Table and figures.
- *50A & 141W* loss give $T_{j,max}$=*121 ℃* with T_{case}=*82 ℃*

I (A)	V1 (V)	V2 (V)	Ron_1 (mΩ)	Ron_2 (mΩ)	P1 (W)	P2 (W)	P_total (W)	Tc (˚C)	Tj_1 (˚C)	Tj_2 (˚C)
22	0.49	0.49	22.2	22.3	10.8	10.8	21.6	31.5	37.9	39.2
30	0.69	0.69	22.8	23.1	20.6	20.8	41.3	39	46.7	50.0
36	0.85	0.86	23.5	23.9	30.5	31.0	61.5	48	56.5	62.2
42	1.03	1.06	24.6	25.3	43.2	44.5	87.7	60	71.3	80.4
48	1.27	1.32	26.5	27.6	60.8	63.2	124	75	94.5	106.2
50	1.38	1.45	27.6	29.0	68.6	72.1	141	82	106	121





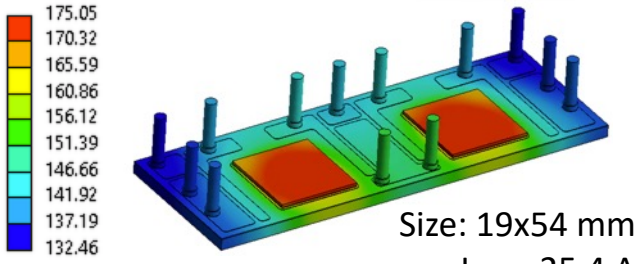


Unit: ˚C

Size: 35x82 mm

I_{max}= 54.9 A

P_{max}= 226.8 W



Unit: ˚C

Size: 19x54 mm

I_{max}= 25.4 A

P_{max}= 97.4 W

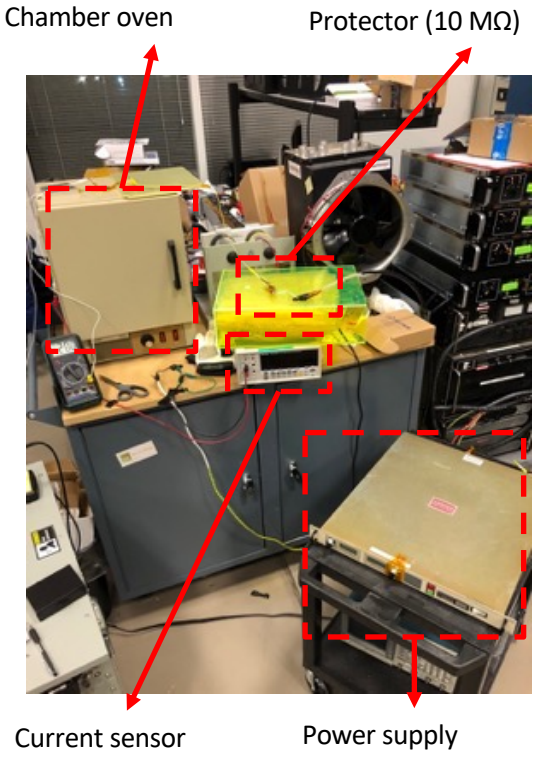
Insulation Characterization for eIMS

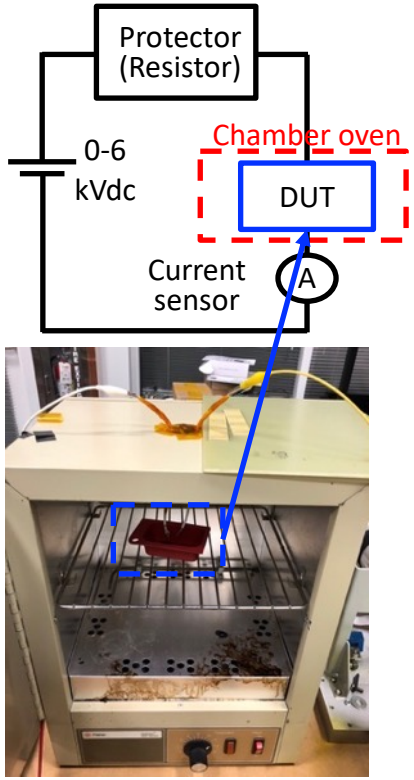
Relationship between geometry and leakage current of epoxy-resin based insulated metal substrate (*eIMS*)

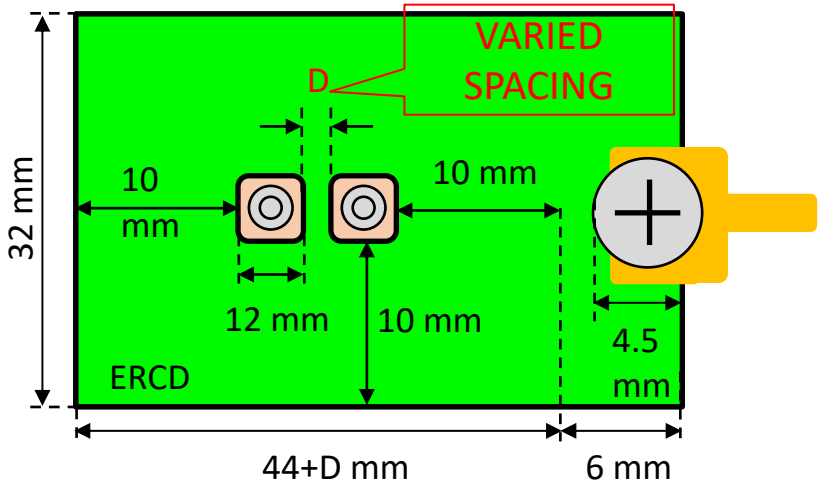
- 120um-thick dielectric together with epoxy encapsulant.
- A 10-Mohm resistor for limiting current ≤1mA if DUT fails.
- Current sensor provides in-situ leakage current monitoring.

This characterizes vertical and horizontal insulation.

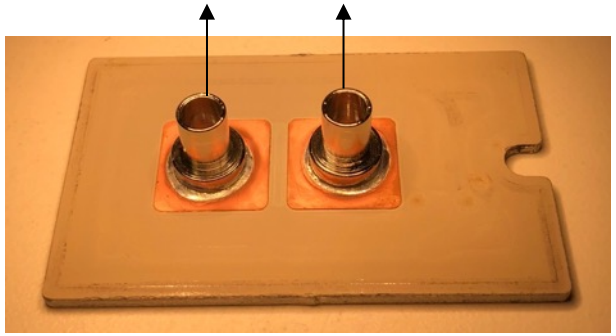
- To accurately measure leakage current, the Cu pads with banana connectors are surrounded by a 10mm-wide Cu-free area.
- The space between Cu pads and temperature are considered as variables.



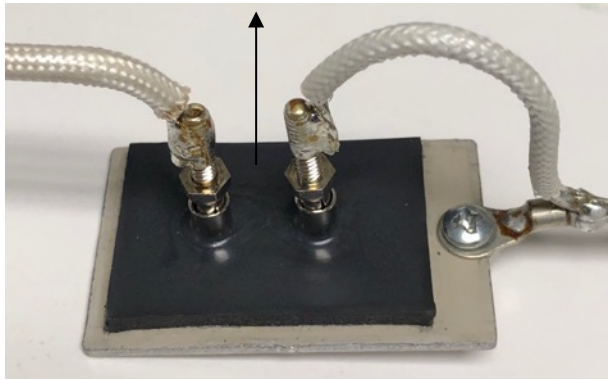


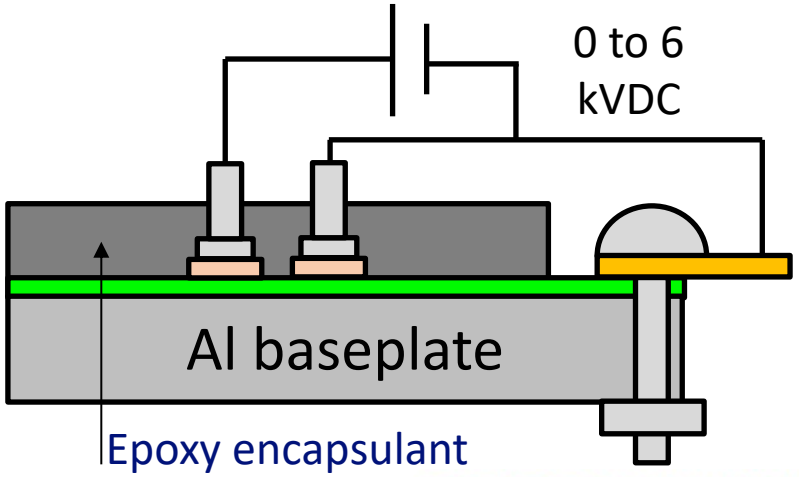


Banana connector



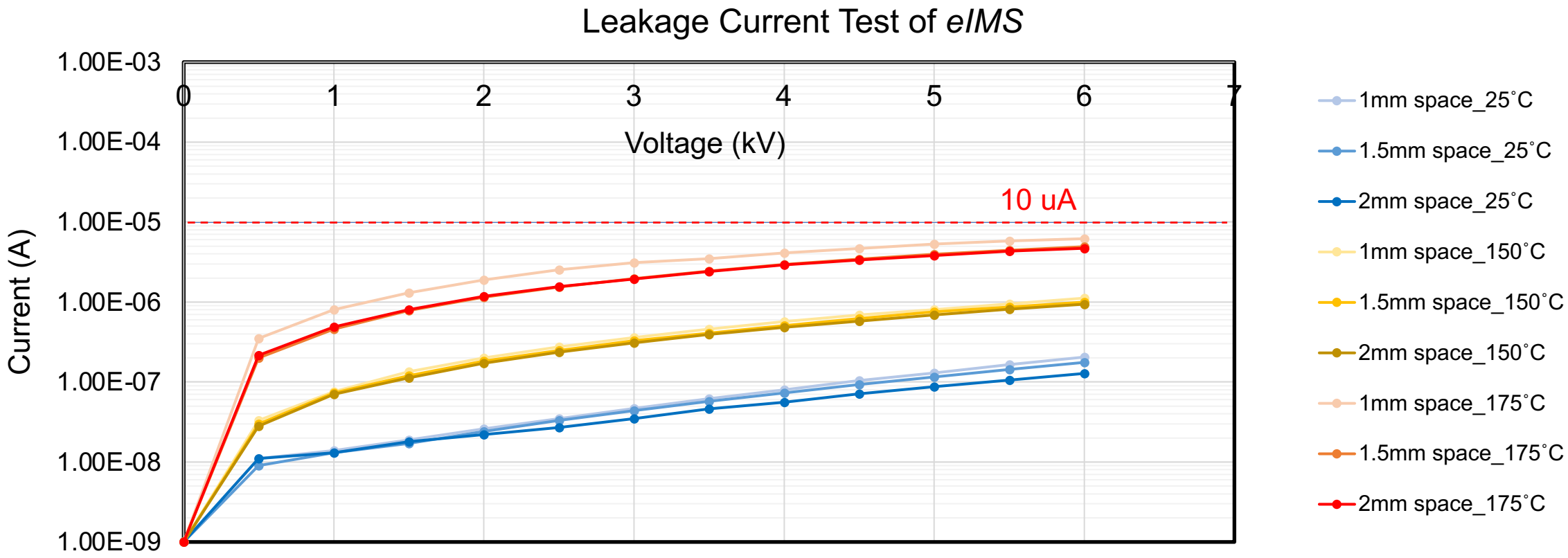
w/ Epoxy encapsulant



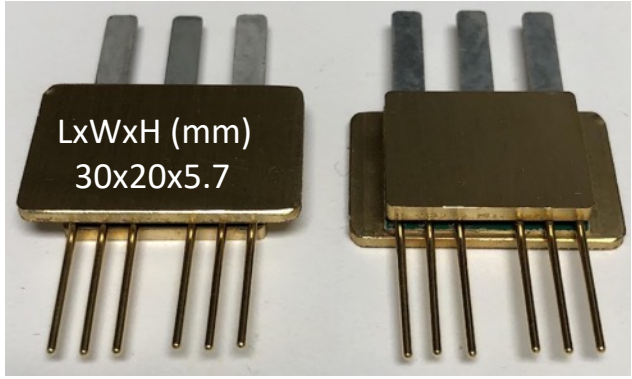


Insulation Characterization For eIMS (Con'd.)

The 120um-thick ERCD on Cu (*eIMS*) can block 6kVDC and yield <10uA leakage current at 175˚C. The leakage paths include:
(1) through the baseplate vertically,
(2) through the dielectric layer (ERCD) horizontally,
(3) through the epoxy encapsulant horizontally,
(4) through the interface of ERCD and epoxy encapsulant horizontally.



Demonstration of Advanced Power Packaging Technology for Near Term Commercialization



PowerAmerica Member Initiated Projects

Prof. Douglas C Hopkins, Prof. Wensong Yu, Tzu-Hsuan Cheng, Sourish Sinha, Utkarsh Mehrotra
NC State University

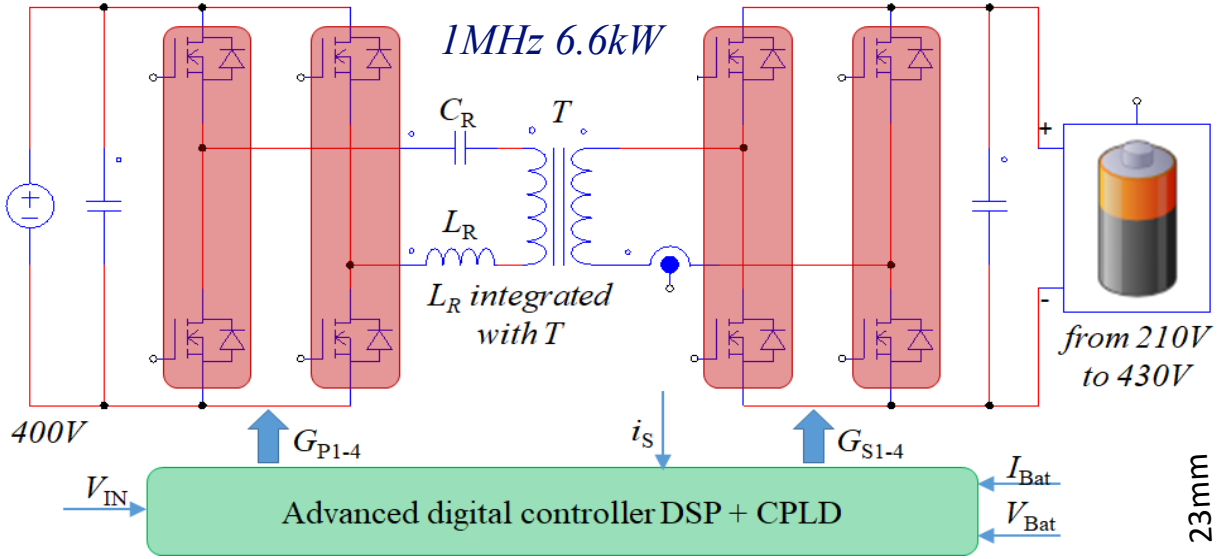
Dr Carl Neufeld, Transphorm, Inc.
Dr. Peter Losee, United SiC

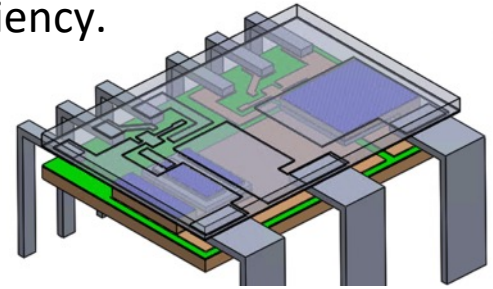
This project is funded by the PowerAmerica Institute, North Carolina State University

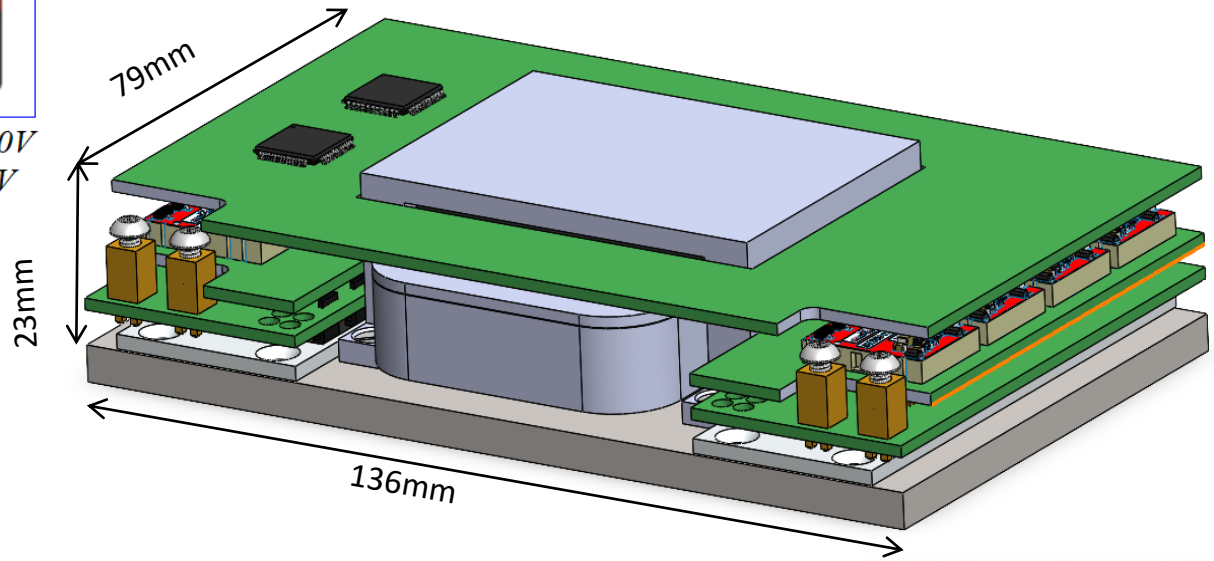
Objective

PROVIDE LOW COST, HIGHLY RELIABLE, NEAR-TERM POWER PACKAGING SOLUTION THE POWER ELECTRONICS INDUSTRY CAN GROW WITH.

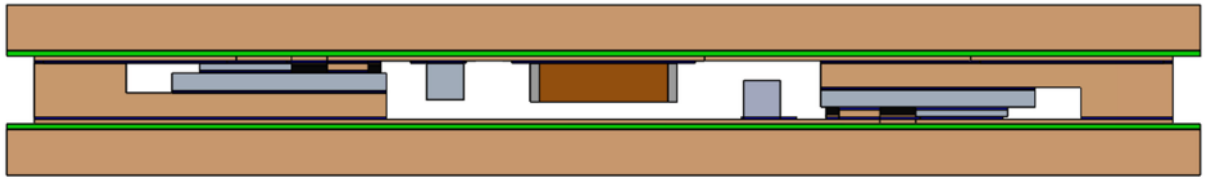
- Intro new epoxy insulated metal substrate (*eIMS*) processed by PCB/OSAT houses.
  - The *eIMS* uses a new 'high temperature, highly thermally conductive organic dielectric having characteristics of *40kV/mm* breakdown, *10W/mK* and operates at *Tg≥300 ℃* with a low modulus.
- Demo ½-Bridge GaN modules in a *400V/6.6kW, 1MHz* charger at *≥98%* efficiency.

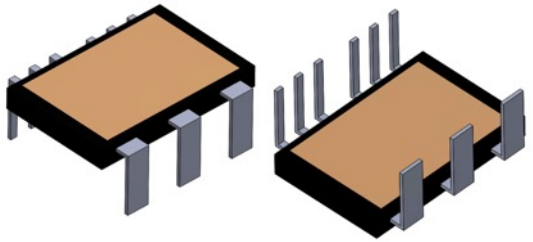




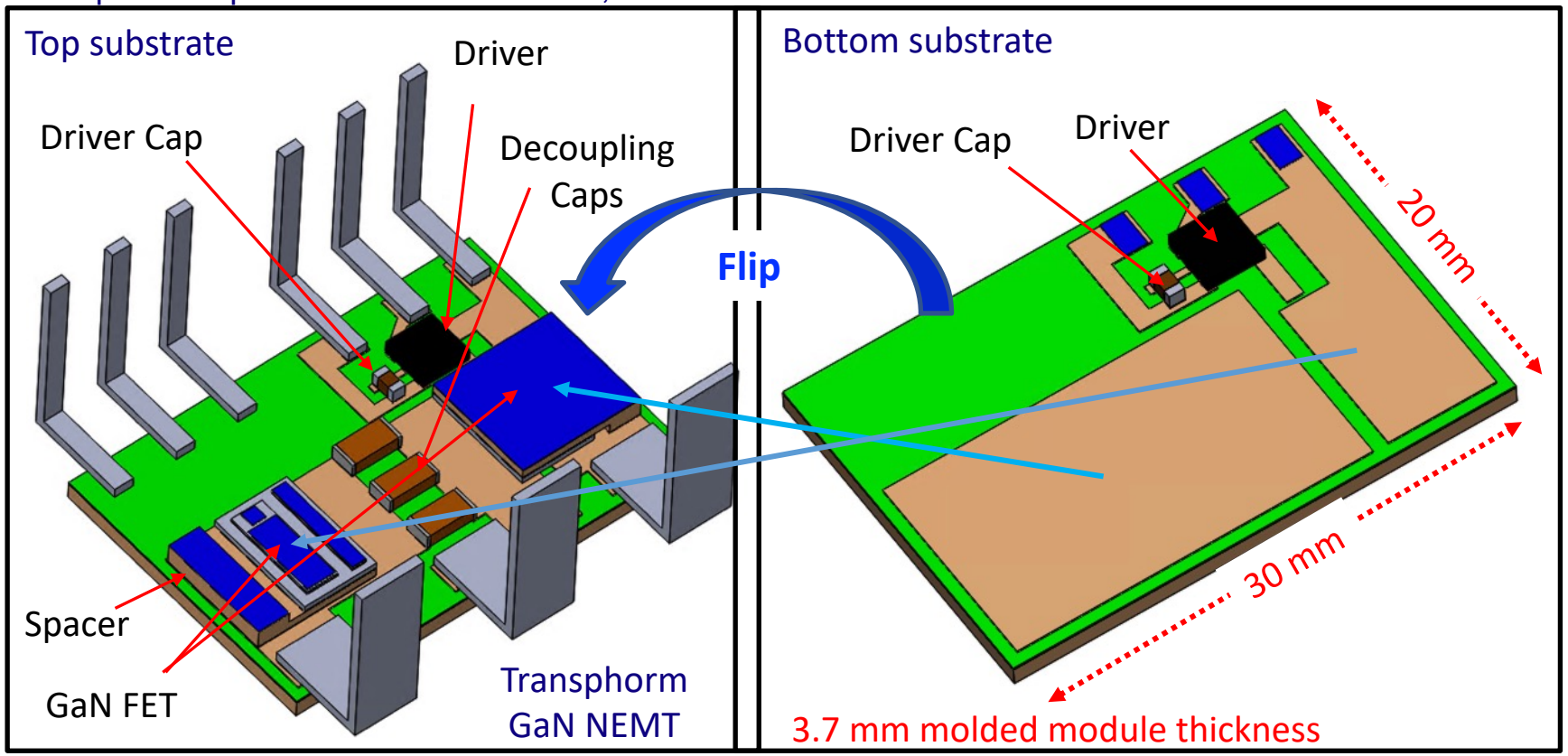


Single-Die HB-IPM Layout *(Transphorm)*



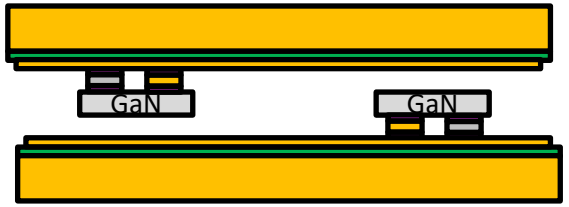


Transphorm eq.:TP65H015G5WS 650V, 15 mΩ

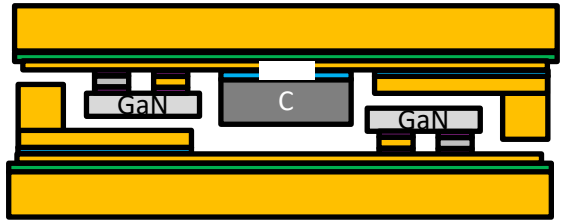


Fabrication flowchart

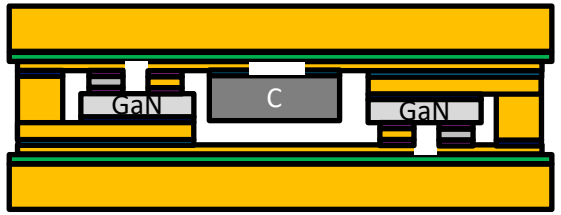
1. Die bonding by Semi-sintering (20min ramp from 25˚C to 130˚C, hold for 120 minutes;15 minutes ramp to 200˚C, hold for 60 minutes)



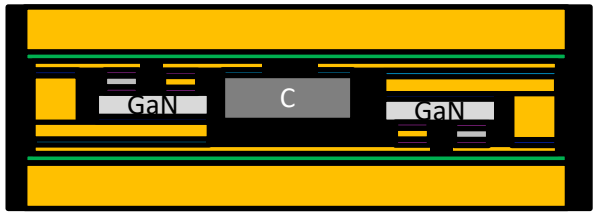
2. Spacer, capacitor, driver, pin bonding by Sn90/Sb10 solder (MP: 250 – 257˚C)



3. Top and bottom substrate assembly by SAC305 (MP: 217 – 219˚C)

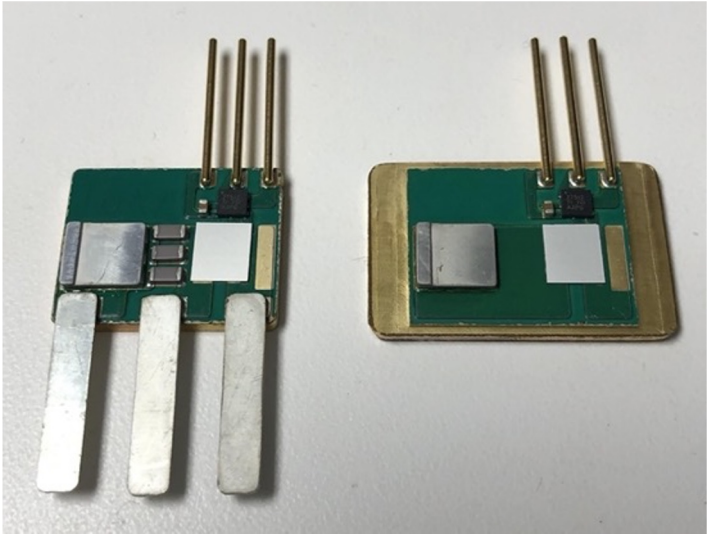


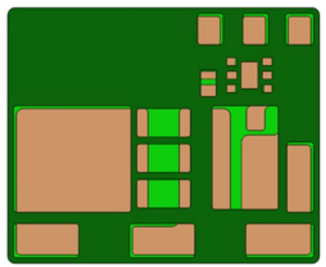
4. Encapsulation by epoxy molding compound



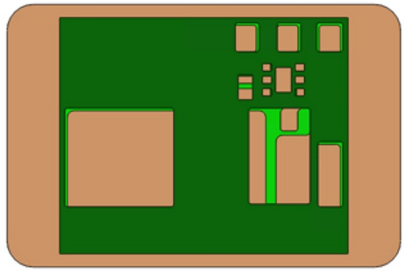
Dry run of module fabrication flowchart (eIMS version)

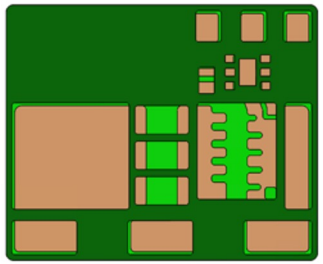
1. Mount dies, spacers, drivers, capacitors, and terminals on top and bottom substrates



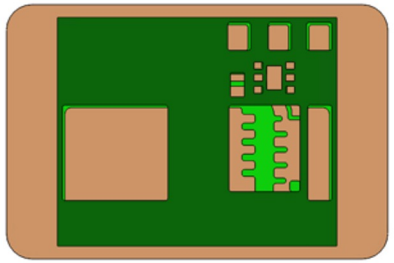


Transphorm Design

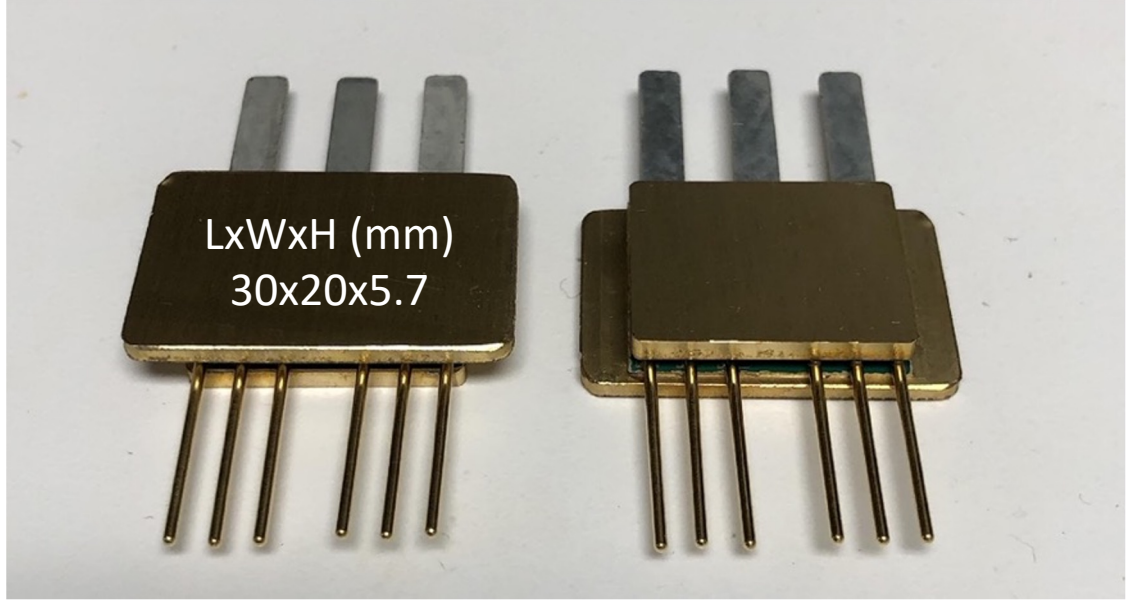




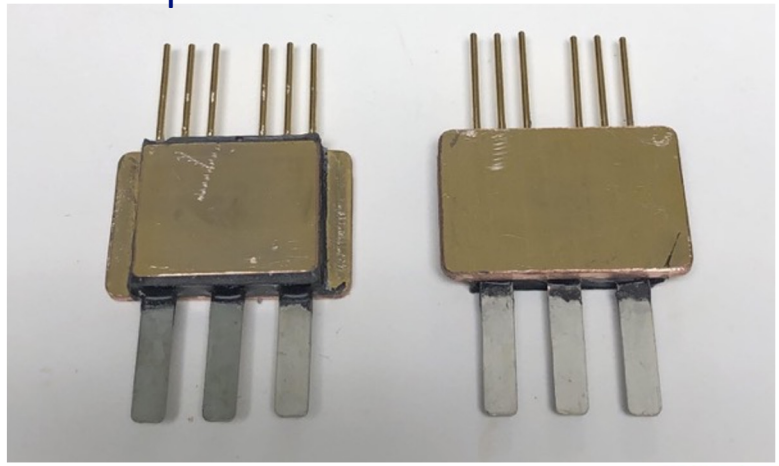
GaN Systems Design



2. Assemble top and bottom substrate assembly



3. Encapsulation



Status of eIMS Substrate Manufacturing

1. Brigitflex requested 18x24” ERCD bonding sheets from RISHO.
2. Brigitflex trimmed to 9x12” and 12x18” for processing T1/T3 (Top eIMS) and T2/T4 (Bottom eIMS),for Transphorm/GaN Syst, respectively.
3. Brigitflex finished lamination and patterning/etching process as shown above.
4. Brigitflex completed solder mask, surface finish, and routing/slicing Oct. 11 - Oct. 17

Sept.27,2021

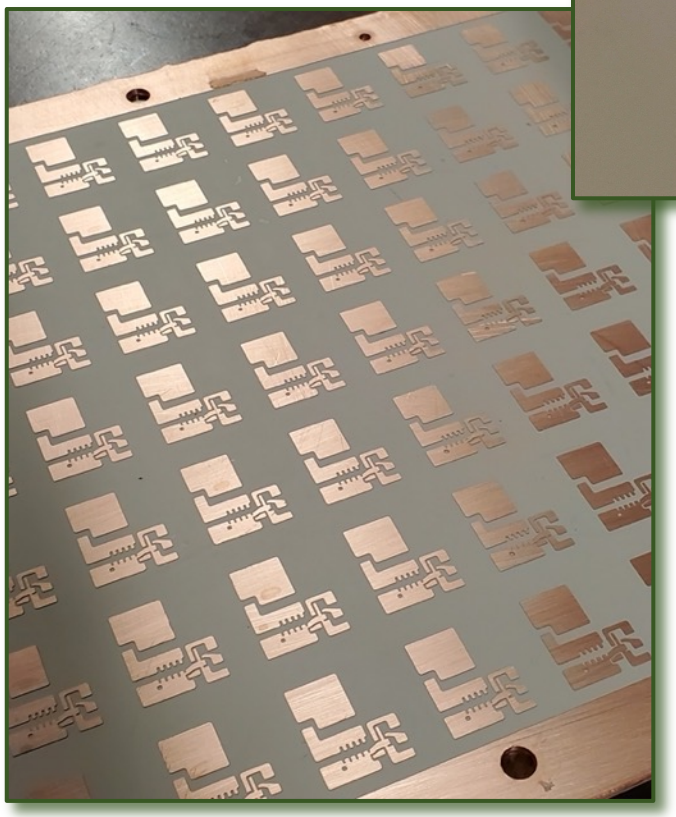
M/S. Brigitflex

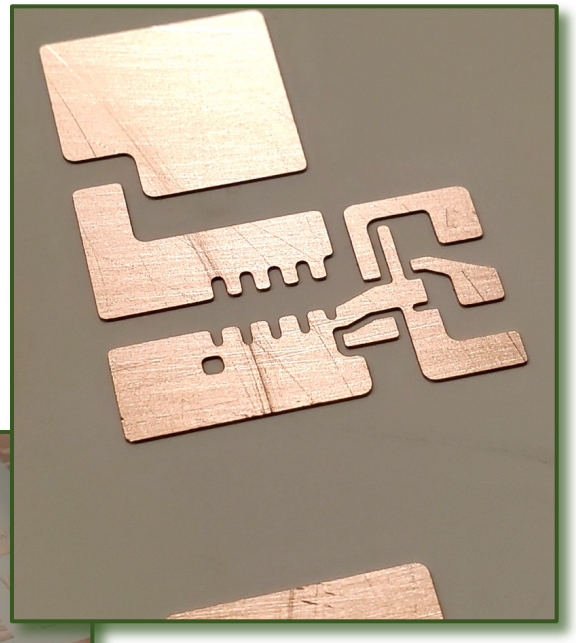
利昌工業株式会社
RISHO KOGYO CO, LTD.

RISHO KOGYO CO.,LTD
TOKYO OFFICE

LIST of TEST Samples

Product No.	AD-7210N
Material	High Thermal Bonding Sheet (10W/mk)
Production Lot No.	AK6-X419-4
Quantity(sheets)	15
Dielectric nominal thickness(mm)/(mil)	0.12/(5mil)
Panel size(mm) /(inch)	458×610/(18×24)
Releasing film	PET film double sided
Appearance	No problem
HS Code	3919.90.5060
Gross Weight (Kg)	3



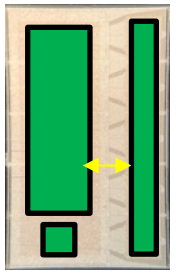


GaN Syst Patterns

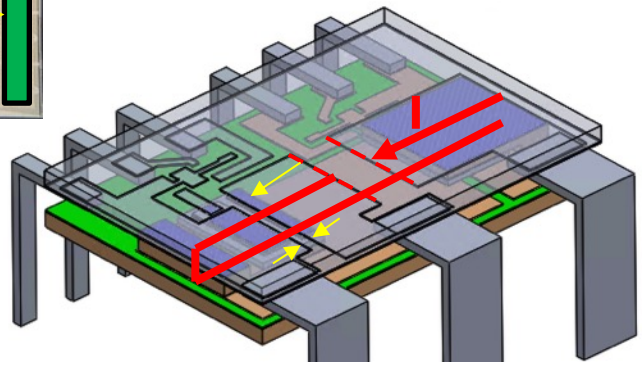
Q3D & Thermal Comparison

Transphorm & GaN Syst. Designs

T_a = 50˚C, $T_{c,max}$ = 90˚C P_1/P_2=12.5W (>98% eff)	Transphorm version		GaN Systems version	
IMS type	Cu baseplate	Al baseplate	Cu baseplate	Al baseplate
h coefficient (W/m^{2}K)	1450	1585	1450	1570
Tj,1 (˚C)	97.2	96.6	97.2	96.8
Tj,2 (˚C)	99.1	98.5	101.3	101.3
Rjc,eq (˚C/W)	0.36	0.34	0.45	0.45
Rja,eq (˚C/W)	1.96	1.94	2.1	2.1
Pd,max (W)	51.0	51.5	48.7	48.7



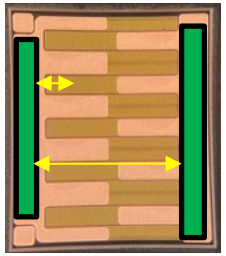
Transphorm
4.7x7.1 mm

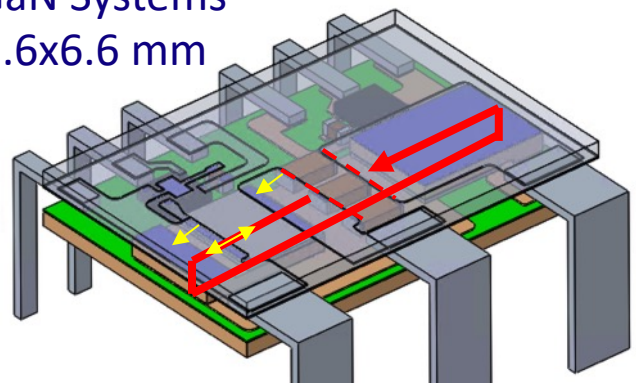


Commutation Loop Inductance	Value (nH)			
	DC	1 MHz	10 MHz	100 MHz
Transphorm version	2.99	1.51	1.50	1.50
GaN Systems version	2.51	1.18	1.18	1.18

Size: 20 x 30 x 4.24 mm (excludes terminals)

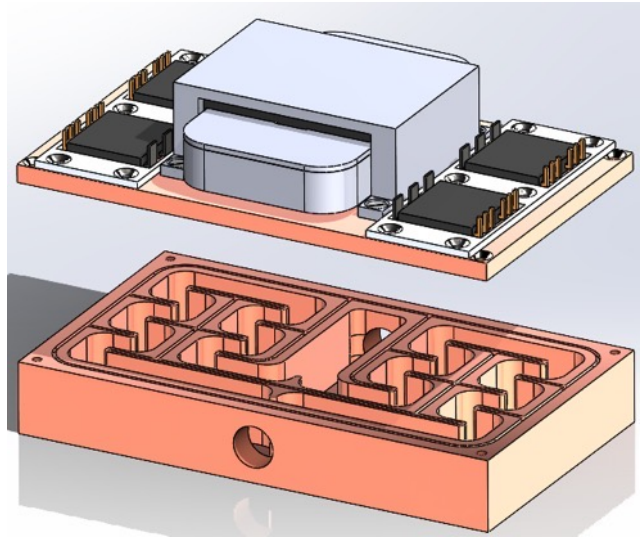
GaN Systems
5.6x6.6 mm

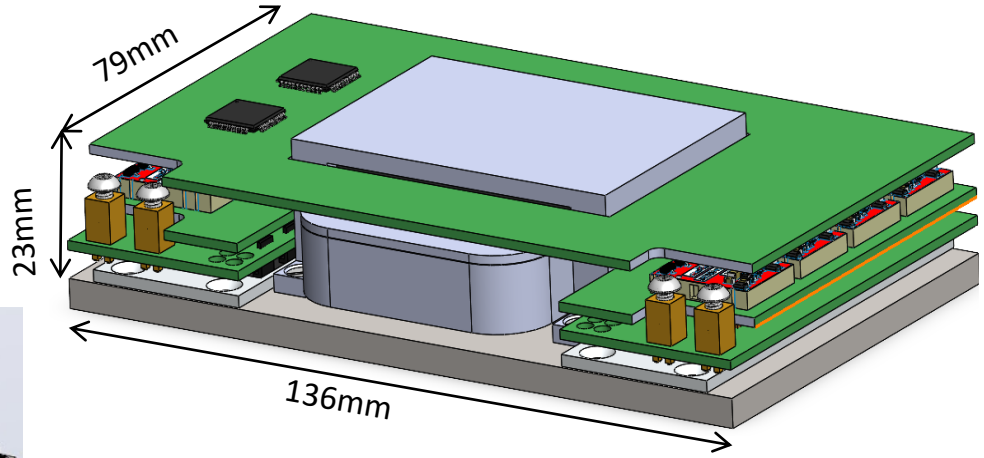


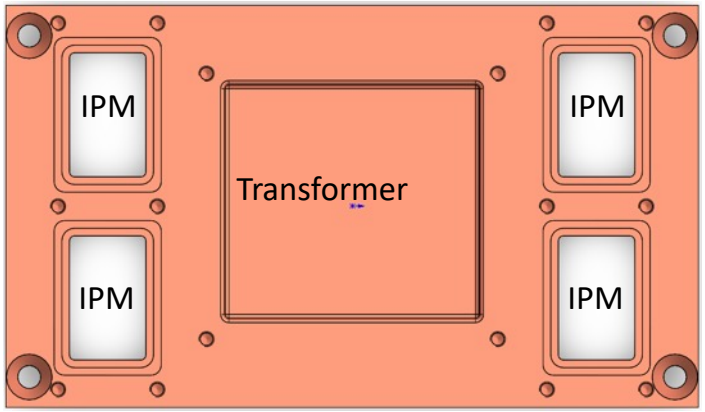


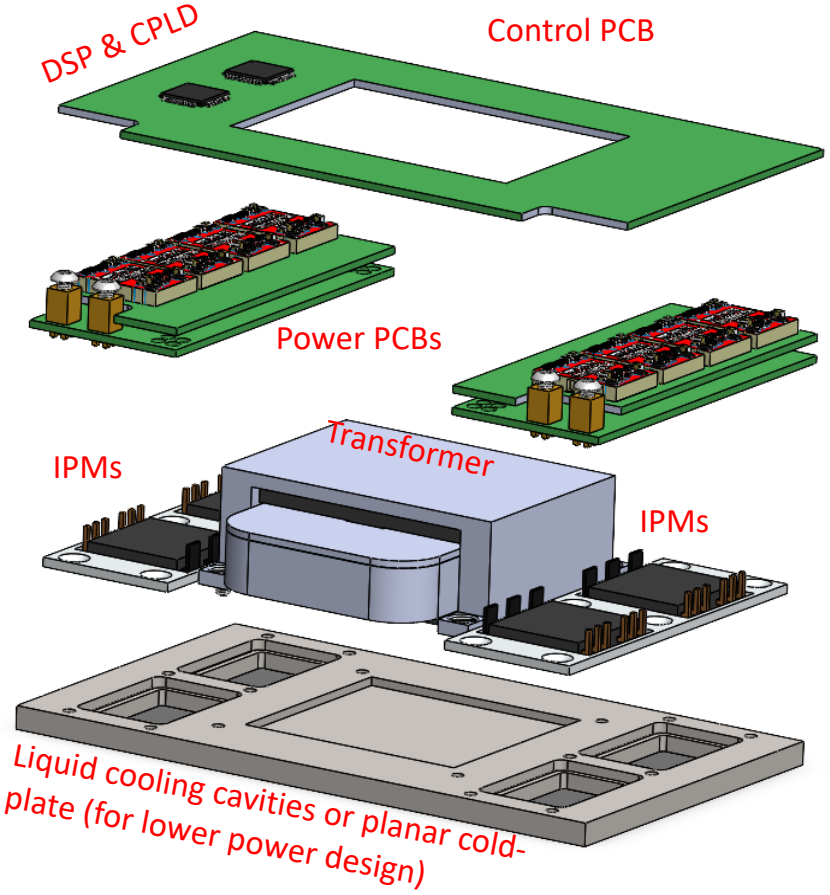
Compact 400V/6.6kW, 1MHz Fast-Charger Demo

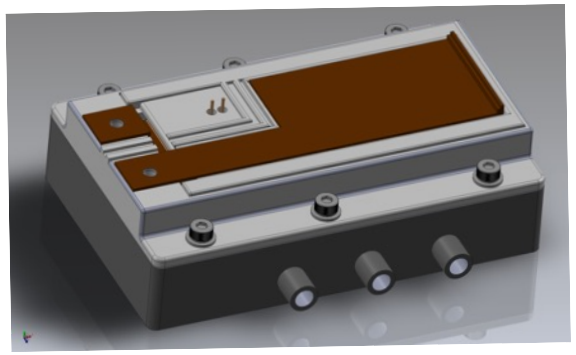
- Power Density of 12.7kW/L (209 W/in^3)
- Efficient liquid cooling design for both IPMs and transformer
- Vertical integration of IPMs, transformer, power PCB, and control PCB

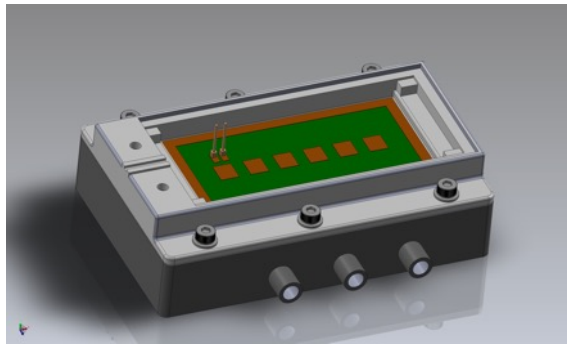










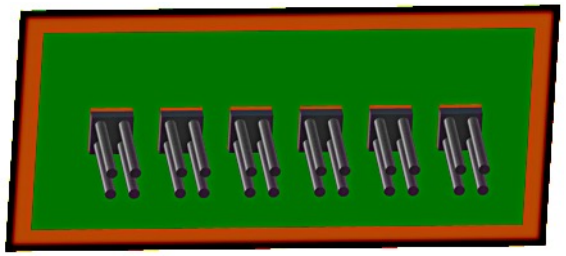


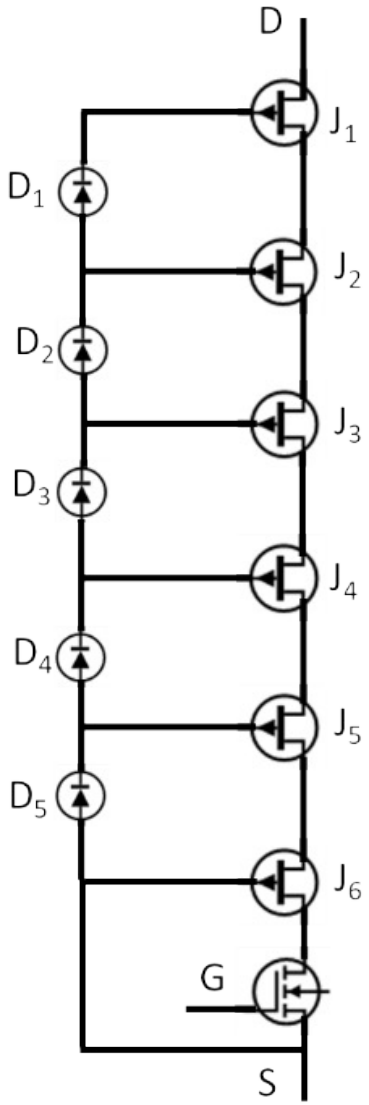
Highly Robust Integrated Power Electronics Packaging Technology

Prof. Douglas C Hopkins, Utkarsh Mehrotra
NC State University

Focus is on: Power switch module topologies scalable to MV/HV/VHV

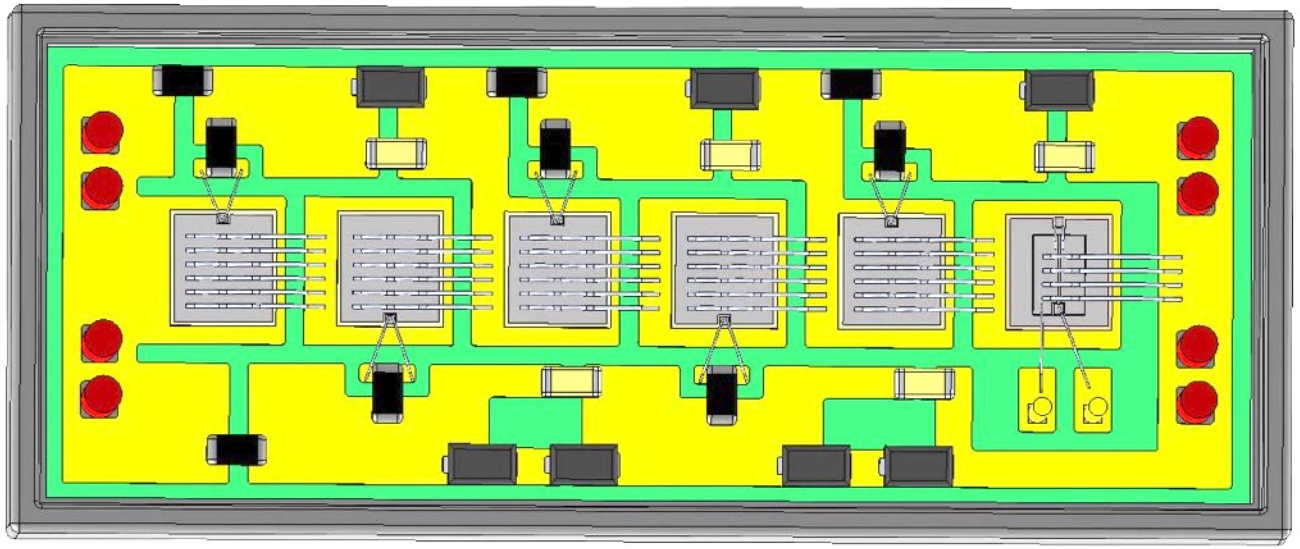
- Packaging for 6.5 kV substrates cascaded to 24kV, and scalable to >100kV)
- “Segmented Baseplate” power modules for reduced ground coupling currents
- High temperature (≥250˚C)
- High power density with dielectric cooling

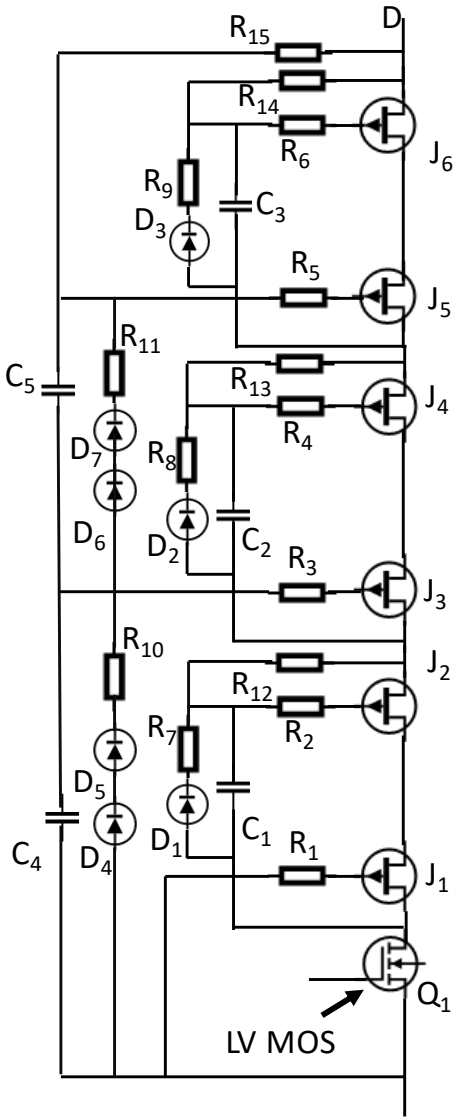




Based on Cascaded SuperCascode Networks

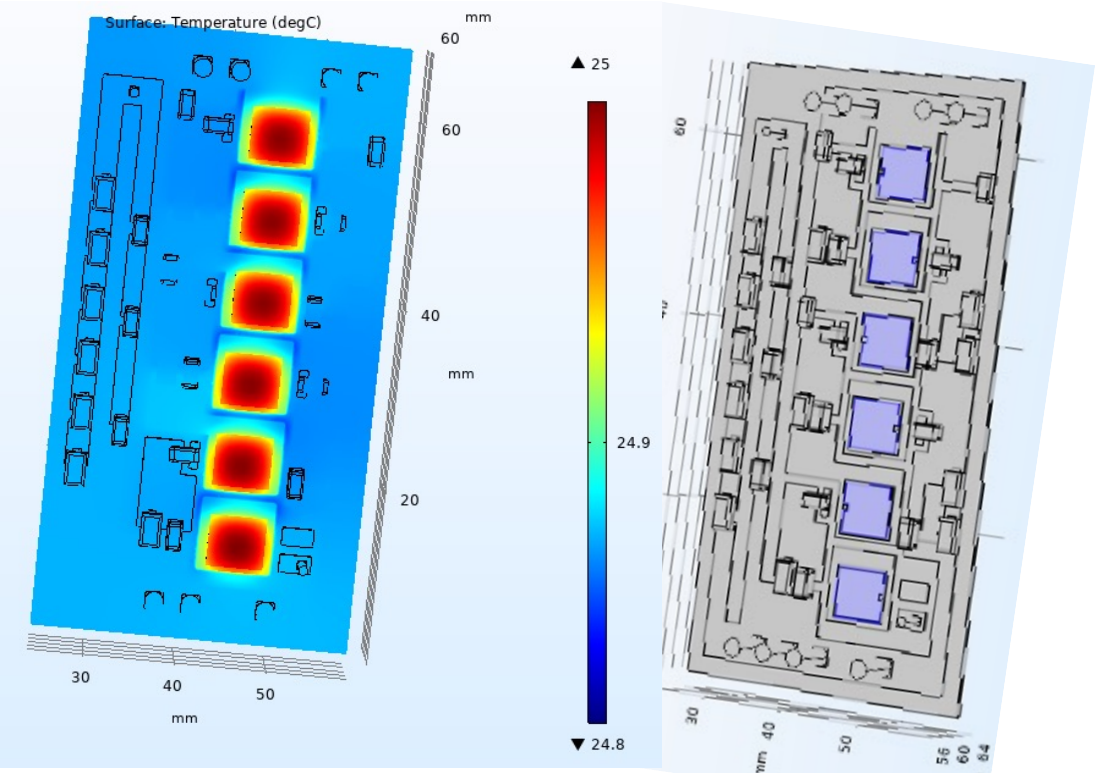
Creating a Medium Voltage (MV) scalable circuit with a new packaging approach

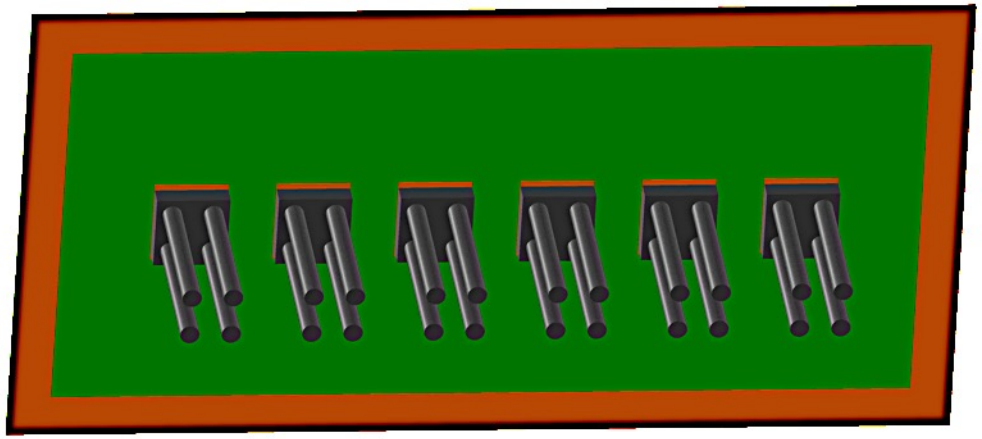


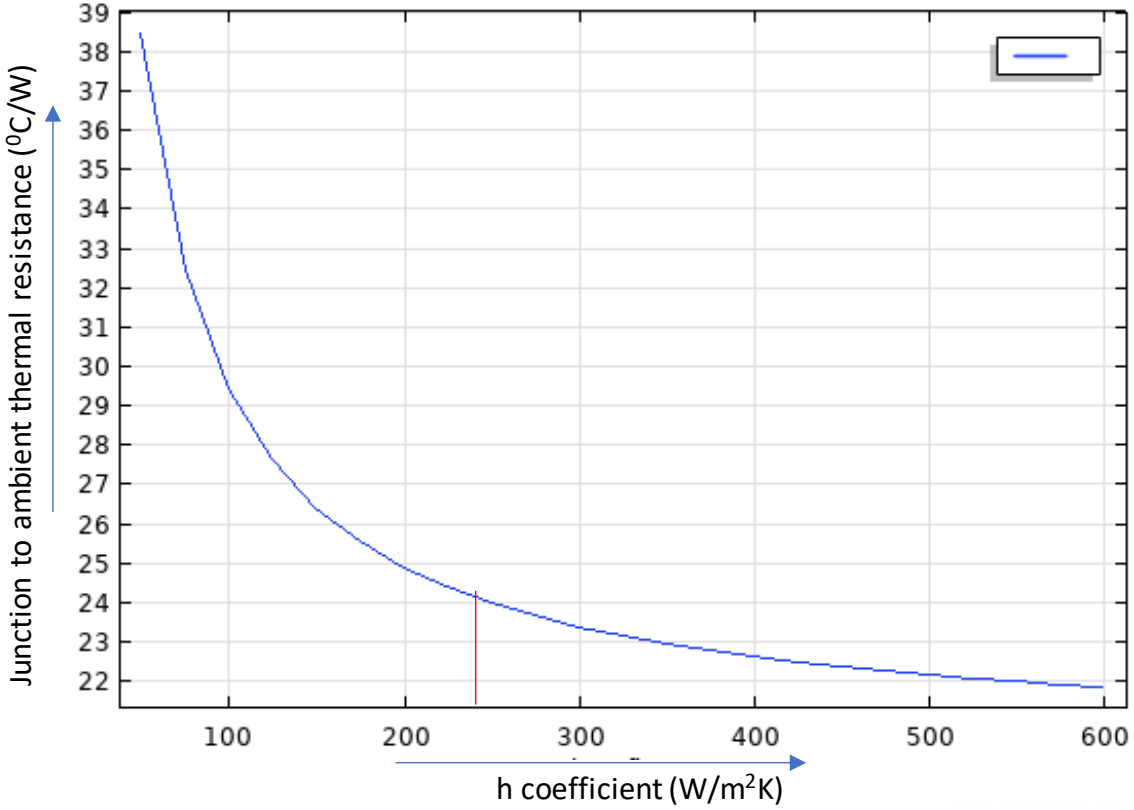


Thermal Performance

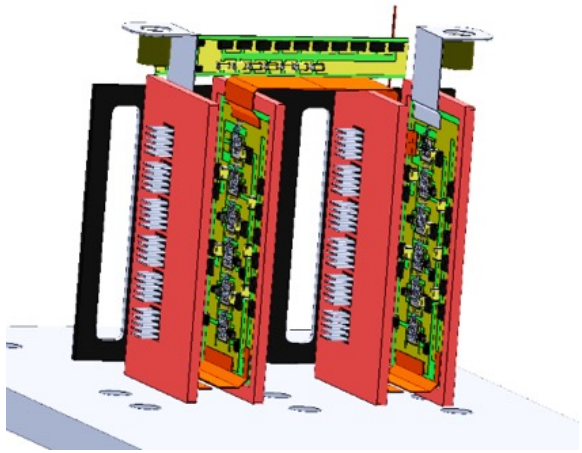
Dielectric fluid cooling provides high power density and performance



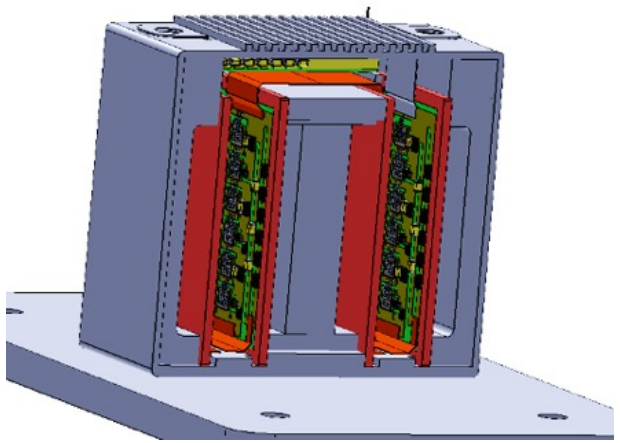




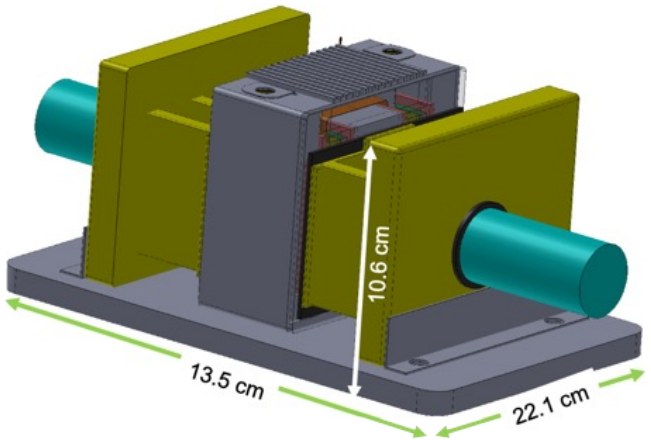
Fluid Cooled 24kV/105A Power Module Assembly



- Four serial 6kV/105A Cascaded SuperCascode Power Modules (CSCPM) (PLX01-CS65E2S10E2UM1)



- HV-CSCPM without fluid chambers. Projected dimensions: 10x9.6x4.7cm, performance: 1.43 MW/kg (liq) (1.16 MW/kg air), 2.66 MW/L and 99.5% eff



- Dielectric liquid cooled 24kV/105A High Voltage Cascaded SuperCascode Power Module (HV-CSCPM). [~20A at 50˚C air cooled] (PLX01-CS24E3S10E2UM3)

Thin Organic Substrates Are Key to Heterogeneous Integration

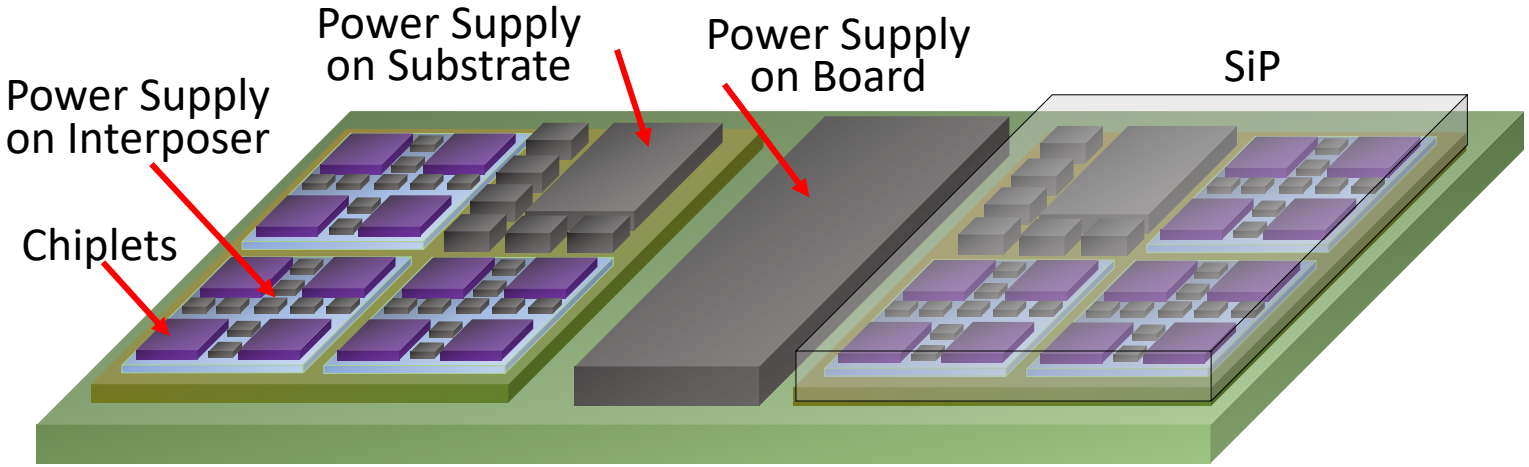
Next slide introduces the recent “Integrated Power Electronics” Chapter 10 of the Heterogeneous Integration Roadmap

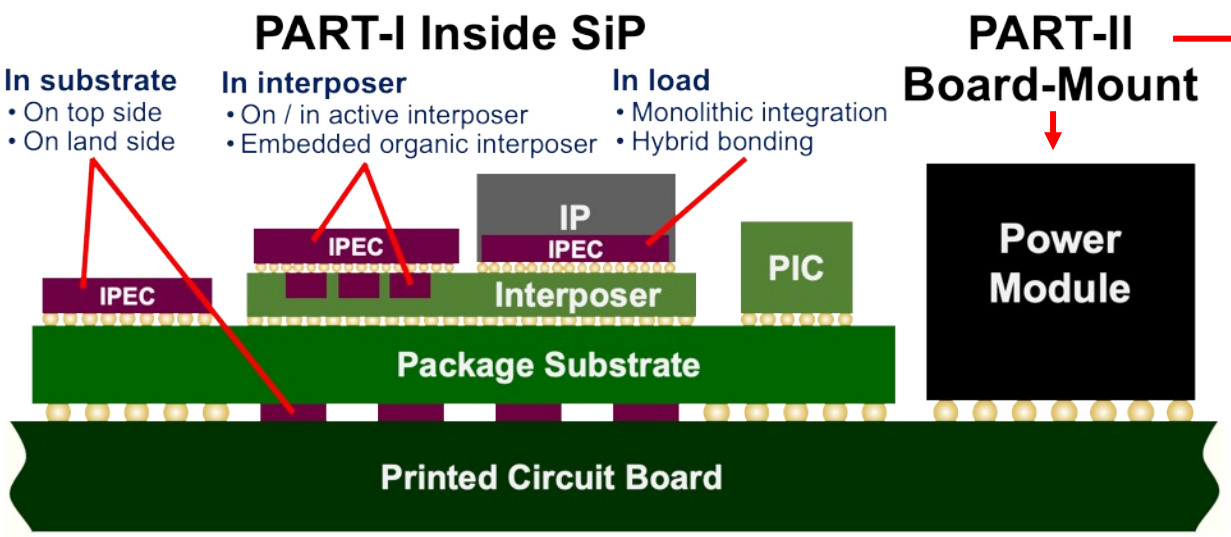
Not only for higher power modules….

Basis for Heterogeneous Integration

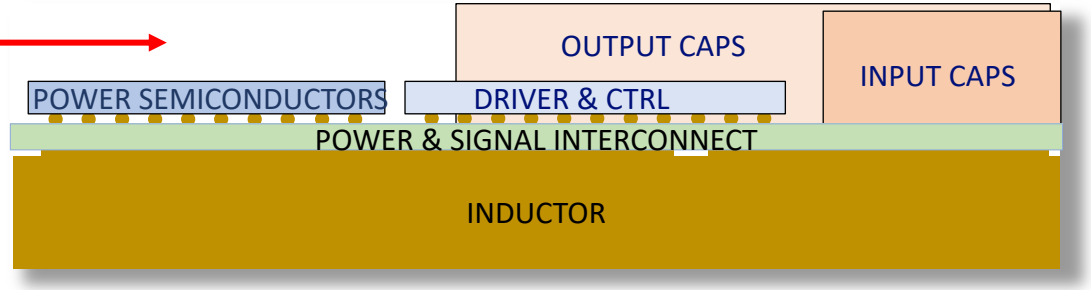
Heterogeneous Integration Roadmap 2021 Edition
https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

IPEC (Integrated Power Electronic Component)





PART-II Board-Mount



PART-III Standalone

PART-IV Energy Harvesting

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