Advanced Dual-Sided Half-bridge Packaging with Epoxy Insulated Metal Substrates (eIMS)

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What?

Extending IMS to eIMS with new high temperature, highly thermally conductive organic composite dielectric

IMS: Insulated Metal Substrate → eIMS: Epoxy IMS

Why?

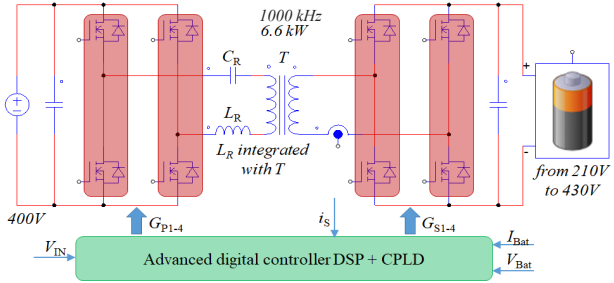
- *Lower Cost through materials and manufacturing*
- *Low Modulus Organic Dielectric for greater reliability*
- *High Thermal Conductance Through Thin Laminates*

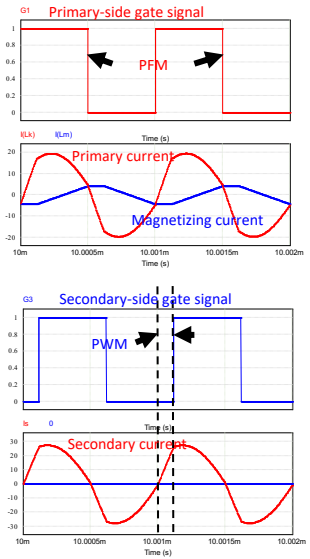
What else?

- *Planarizing GaN Cascode with Semi-Silver Sintering*
  Low/no flow-out for stable placement, Low Modulus for greater reliability
- *Identifying the PCB/OSAT Manufacturers*
  Large panels at very high volume by many manufacturers
  THINK: Designing & producing heterogeneously integrated power modules through virtual fabs

DEMONSTRATION* IN A

400V : 210-430V Fast Charger w/ 6.6kW/ 1MHz / >97%





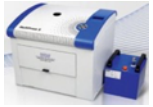
- *Advanced PFM & PWM optimizes controllability of with adaptability to load and voltage variations;*
- *1MHz ZVS reduces weight and volume of passives;*
- *Transformer integrated resonant inductor simplifies power circuit, and reduces system cost;*
- *0.2ns time step control with variable frequency modulation, and resonance trajectory detection and prediction, expands soft switching range and minimizes circulating power;*
- *Cost-effective DSP and CPLD avoids complicated FPGA hardware and time-consuming software.*

Lead by Prof Wensong Yu

GO ONLINE
To see what we develop
https://go.ncsu.edu/prees_open_source

LPKF ProMask Pro Legend, UV Lamp Table

1. Panel size: 22.9 x 30.5 cm (9" x 12")
2. Up to eight layers
3. Custom process profiles



LPKF MultiPress S Auto Lamination Press

PREES' Recent Equipment Investment

1. Max. size: 25.0 x 33.0 x 2.6 cm (9.8" x 13" x 1")
2. Min. space/width: 0.1mm
3. Mech. resolution: 0.5µm

LPKF ProtoMat S104 Circuit Board Plotter

1. Panel size: 23.0 x 33.0 cm (9" x 13")
2. Thru-hole electroplating
3. Electroless tin plating
4. Max. via aspect ratio 1:10

LPKF Contac-S4 Etching&Thru-Hole Plating

(*not presented in this conference)

complex programmable logic device (CPLD)

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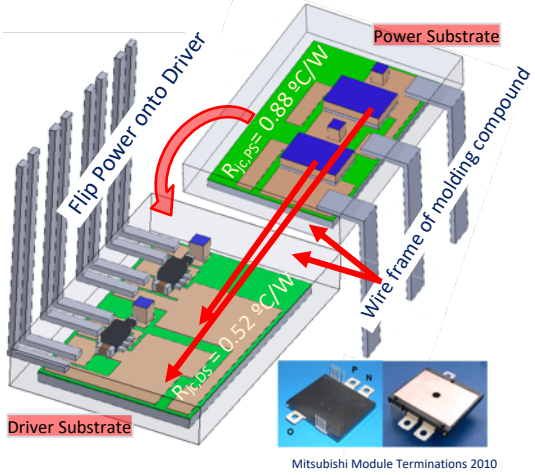
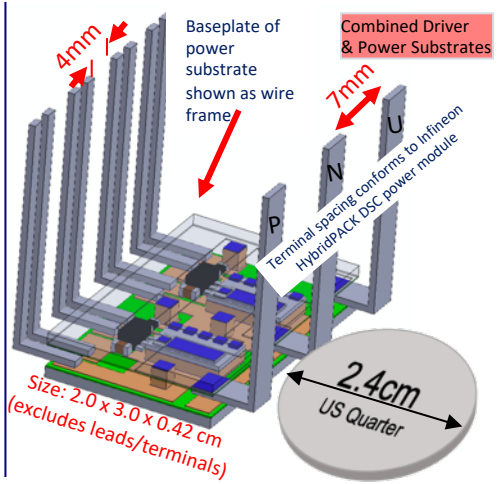
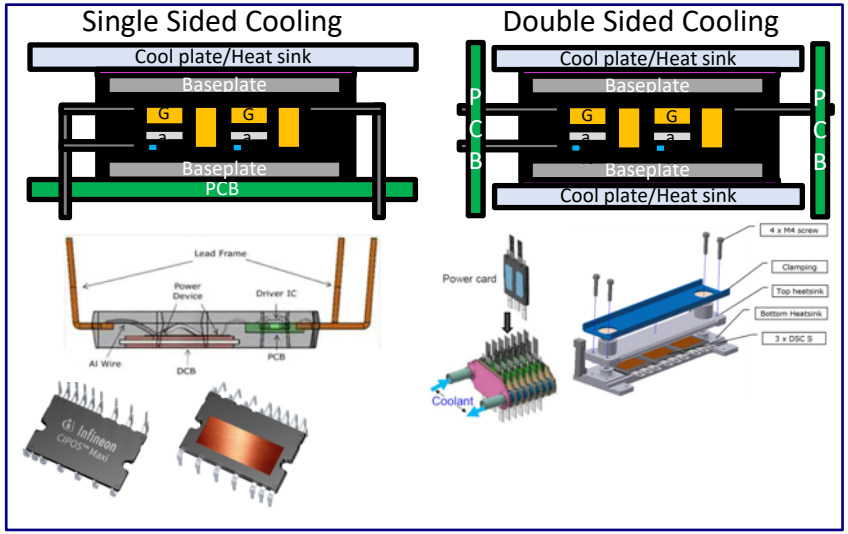
PREES GaN MODULE VER-1

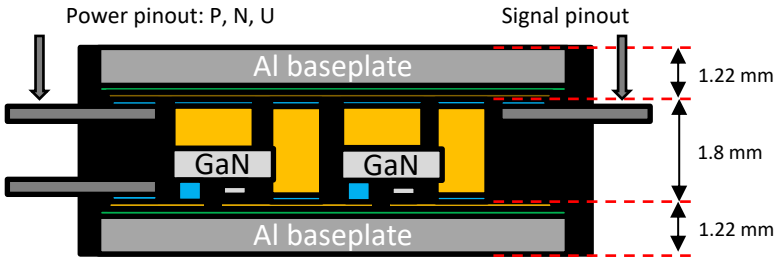
(PLX01-MD-6E2-H-20E1-S2IMS)

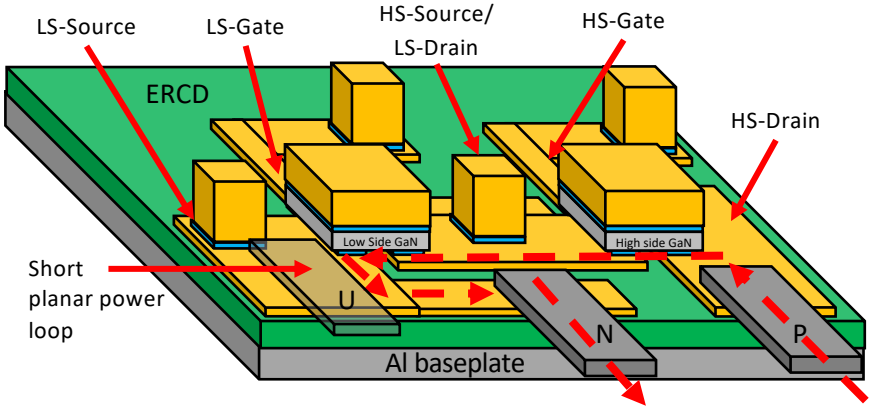






1. GaN HEMT half-bridge module using Transform TP65H015G5WS 650V/18mΩ die
2. UCC27531 SOT-23 35V/5A FET driver w/ Vishay 0603 1Ω TF resistor and 0603 0.22uF cap SMDs
3. RISHO CC-7210N eIMS (Cu/ERCD/Cu at 100µm/120µm/ 1mm)
4. Commutating capacitors and organic interposer <u>explored</u> in possible Ver-2





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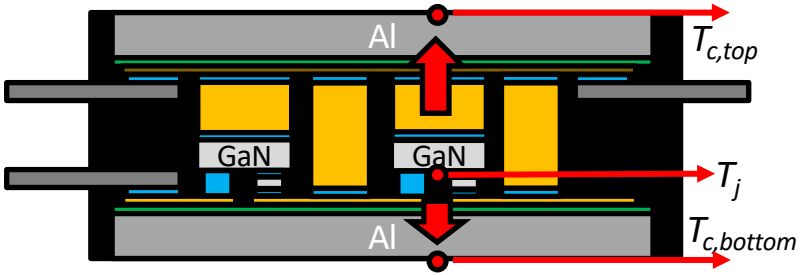
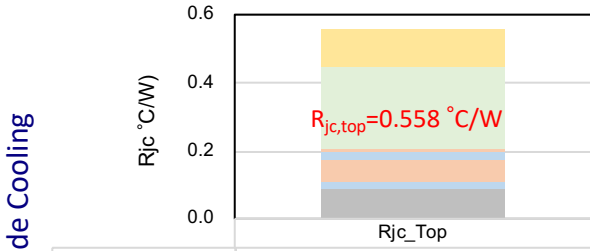
ANSYS Thermal Characterization

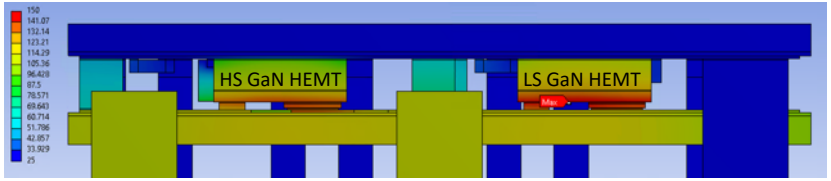


$$R_{jc,eq} = R_{jc,top} \,//\, R_{jc,bottom}$$
$$= 0.444\ ^\circ C/W$$

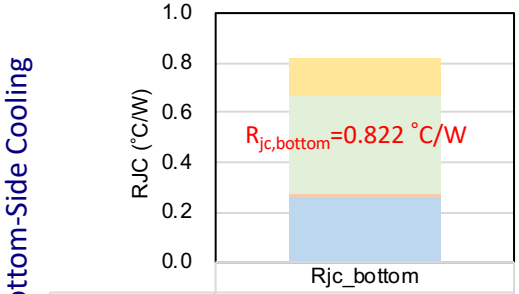


Top Al baseplate	1.15E-01
Top ERCD	2.42E-01
Top Cu	5.27E-03
Top Spacer Solder	2.47E-02
Top Spacer	6.43E-02
Die Attach	2.31E-02
GaN	8.38E-02

Top-Side Cooling

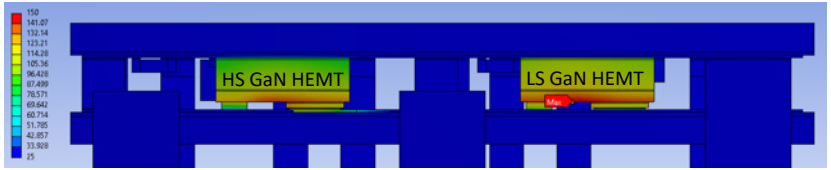


- Tc,top = 25˚C
- Tj,max = 150˚C
- Assume each GaN takes 50% of $P_{d,total}$
- Max. $P_{d,total}$ = 426.74 W (for two GaN devices)



Bottom Al baseplate	1.55E-01
Bottom ERCD	3.97E-01
Bottom Cu	1.06E-02
GaN Solder/Si FET	2.60E-01

Double-Side Cooling



- Tc,top = Tc,bottom = 25˚C
- Tj,max = 150˚C
- Assume each GaN takes 50% of $P_{d,total}$
- Max. $P_{d,total}$ = 562.76 W (for two GaN devices)

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Epoxy Resin Composite Dielectric (ERCD) Material Systems

Glass Reinforced

CCL [CS]

Copper Foil
Woven Glass Cloth Reinforced Insulation Layer
Copper Foil

Prepreg [ES]

Insulation *Layer*
B-Stage
Woven Glass Cloth Reinforced

$$R_{th} = 1/k * l/A$$

60um – 1600um
CS-3295

60um – 100um
ES-3245

60um – 1600um
CS-3945 (1.3W/mK)

CCL: Cu Clad Laminate
AC/CC: Al / Cu Clad
AD: Bonding Sheet
RCC: Cu Clad Release Film

Thermal Conductivity k

10 W/mK
8 W/mK
5 W/mK
3 W/mK
2 W/mK
1 W/mK

Non Glass Reinforced

Al/Cu Base CCL [AC / CC]

Copper Foil
Insulation Layer
Copper
PLATE
Aluminum

80um – 120um
AC/CC-7210N

80um – 120um
AC/CC-7208

80um – 120um
AC/CC-7200TY

80um – 120um
AC/CC-7303

100um
AC/CC-7302

60um – 100um
AC-7900

Bonding Sheet [AD]

Release Film
Bonding Layer
B-Stage
Release Film

80um – 120um
AD-7210N

80um – 120um
AD-7200TY

80um – 120um
AD-7303

RCC [CD]

Copper Foil
Bonding Layer
B-Stage
Release Film

80um – 120um
CD-7210

80um – 120um
CD-7208

80um – 120um
CD-7200TY

80um – 120um
CD-7303

100um
CD-7302

RISHO

Yoshi Fukawa, TechDream, Inc.
<yoshi@tech-dream.com>

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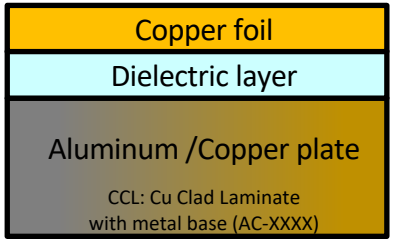
ERCD: (10W/mK) Properties & Price Comparison

PROPERTIES RISHO

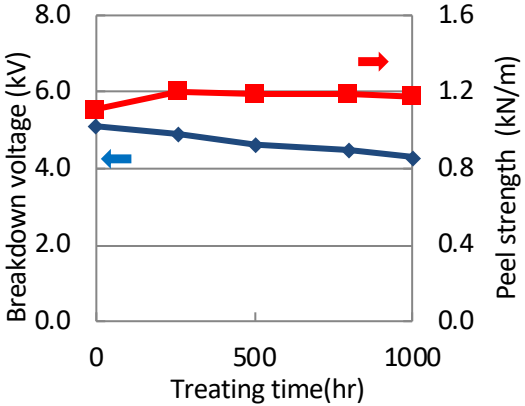
Product number	AC-7210	
Dielectric layer thickness	120µm	
Thermal conductivity (W/mK)	**10**	Laser flush method
Tg (℃)	**270**	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit (sec)	60＜	260℃
CTE (ppm/℃) α1	14/14/14	X/Y/Z
Breakdown Vdc (kV)	**>5**	JIS C2110

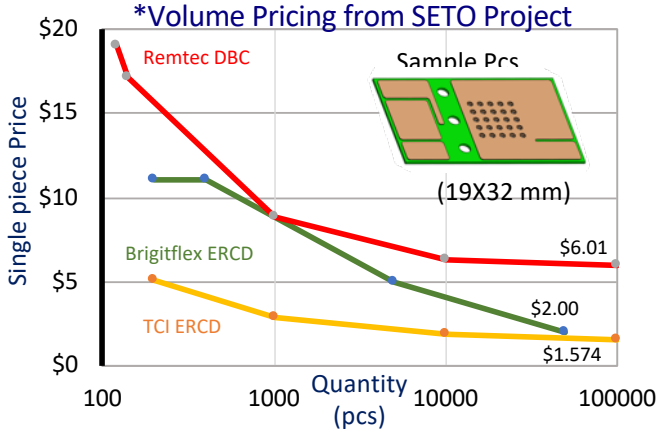
http://www.risho.co.jp/english/product/products0/index.html

eIMS



High temp long term reliability(175℃)





PCB MFGR	ADDRESS	WEBSITE	PANEL SIZE
TCI (TAIHONG CIRCUIT IND. Co., Ltd.)	No.81, Guangfu Rd., Hukou Township, Hsinchu County 303, Taiwan (R.O.C.)	http://www.tci.com.tw/	20"x24" (510x610 mm)
Aurora	2250 White Oak Circle, Aurora, IL 60502	https://auroracircuits.com/	
Amitron	2001 Landmeier Road | Elk Grove Village, IL 60007	https://www.amitroncorp.com/	18"x24"
Brigitflex	1725 Fleetwood Drive, Elgin IL 60123	http://www.brigitflex.com/	21"x41"

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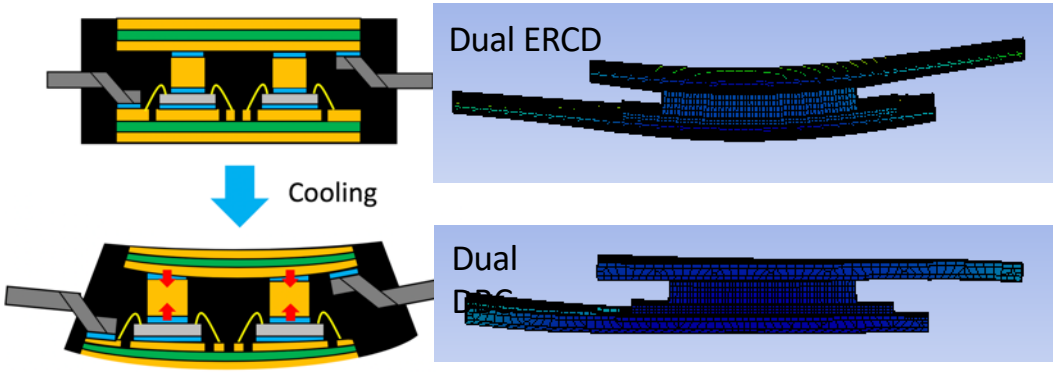
DBC Vs ERCD – Comparison of Mechanical and Thermal Performance

- Thermal cycling test:
  - ✓ Temperature range: -40 – 150˚C
  - ✓ Ramp rate of temperature: 19˚C/min
  - ✓ Dwell time : 10 mins

Thermal-mechanical reliability assessment: Two common failure criteria are assumed in this study:

1. The solder layer (SAC305) between spacer and die – would experience cyclic tensile and compressive stress due to the CTE mismatch and it can induce fatigue failure. According to the Coffin-Manson empirical equation, the fatigue life can be estimated by the equivalent plastic strain (ε_{eq}^{pl}). Fatigue life of SAC305 solder > 1000 cycles
2. Die crack is also a common failure mode in Thermal Cycling Test. Based on the tensile strength of the SiC material, the maximum principal stress cannot exceed 250 MPa.

(Interconnect and baseplate stress in not considered due to the low modulus of the intervening ERCD.)



- Fatigue life prediction: Coffin-Manson fatigue life relationship

$$N_f = C(\Delta\varepsilon_{eq}^{pl})^{-\eta}$$

where

$$\Delta\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{(\Delta\varepsilon_x^{pl} - \Delta\varepsilon_y^{pl})^2 + (\Delta\varepsilon_y^{pl} - \Delta\varepsilon_z^{pl})^2 + (\Delta\varepsilon_z^{pl} - \Delta\varepsilon_x^{pl})^2 + \frac{3}{2}(\Delta\gamma^{pl})}$$

$$\Delta\gamma^{pl} = \Delta\gamma_{xy}^{pl^2} + \Delta\gamma_{yz}^{pl^2} + \Delta\gamma_{zx}^{pl^2}$$

- Anand Viscoplastic Constitutive Model: Considered rate-dependent plastic behavior and creep behavior
  - Flow Equation
  - Evolution Equations

$$\dot{\varepsilon}_p = A\exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m}$$

$$\dot{s} = \{h_0(|B|)^a \frac{B}{|B|}\}\dot{\varepsilon}_p;(a>1) \quad s^* = \hat{s}\left(\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right)^n \quad B = 1 - \frac{S}{S^*}$$

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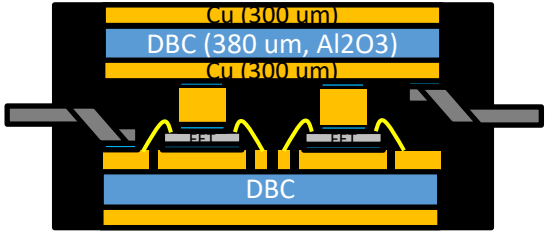
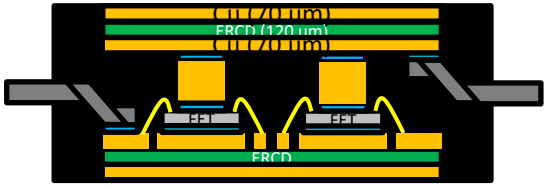
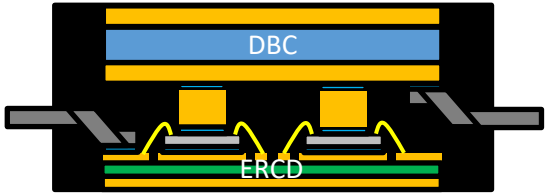
DBC Vs ERCD – Analysis Results of Mechanical and Thermal Performance



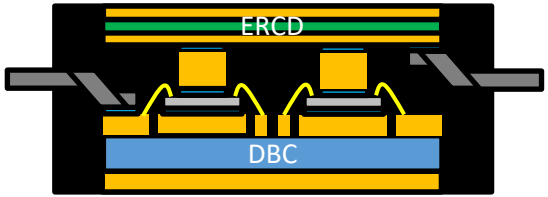
Dual DBC



Dual ERCD

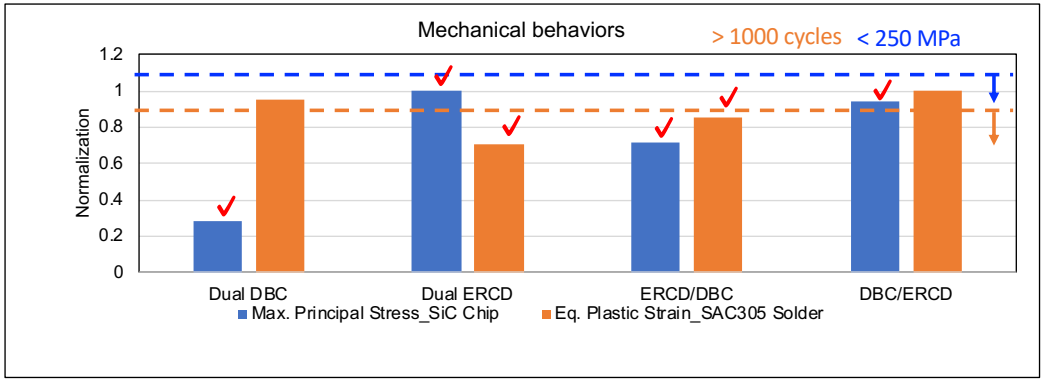


Top/Bottom substrate: DBC/ERCD



Top/Bottom substrate: ERCD/DBC

Components	Materials	Thickness (mm)	Modulus (GPa)	CTE (ppm/˚C)	Thermal k (W/mK)
BiDFET	4H-SiC	0.36	347	4.5	380
Spacer	Cu	1	110	17.6	398
Conductor layer on dielectric		ERCD: 0.07 DBC: 0.3			
Solder	Sn5/Pb92.5/ Ag2.5	0.1	13.8	28.9	36
	Sn95/Sb5	0.1	50	22.8	46
	Sn96.5/Ag3/ Cu0.5	0.1	38.7	21	60
Dielectric	ERCD	0.12	30	14	10
	Al_2O_3	0.38	310	6	24
Molding	2-Pack type (Epoxy + Hardener)	Dual ERCD:2.18 Dual DBC: 3.36	15	16	3



Thermal-mechanical reliability comparison and discussion:

- ✓ Only "dual ERCD" and "ERCD/DBC" can pass the failure criteria for SAC305 and SiC device.
- ✓ Although "dual DBC" offers best reliability of SiC device due to low CTE mismatch between Al2O3 and SiC, the high modulus of Al2O3 (310 GPa) can cause high stress/strain on SAC305 layer.
- ✓ The optimal thickness of all the components (substrate, solder, spacer) and the optimal materials (spacer and molding) will be evaluated in future work

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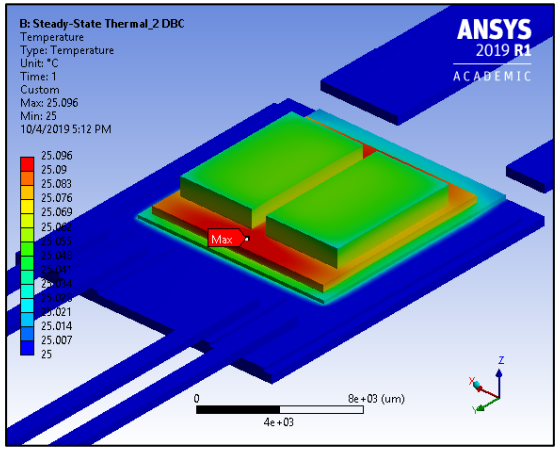
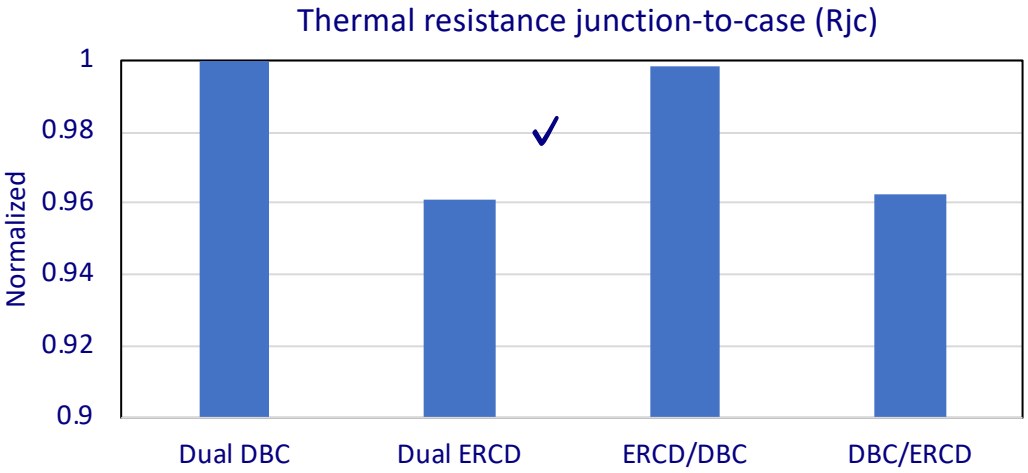
DBC Vs ERCD – Analysis Results of Thermal Performance

- Boundary conditions:
  - ✓ Infinite heat transfer on top and bottom exposed Cu pads
  - ✓ Heat source top surface of die (source)
- Thermal resistance: $R_{jc} = \frac{T_{j,max} - T_c}{P}$





The advantage of ERCD material not only provides a competitive thermal and mechanical performance, but also a cost-effective solution for the advanced power module.

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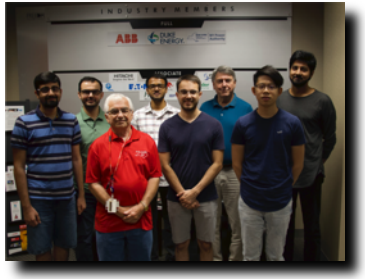

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QUESTIONS

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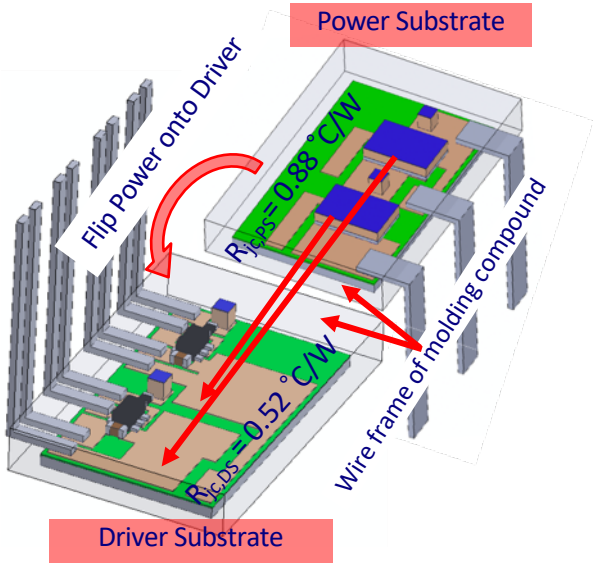

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