Gate driver solution for GaN-based low-power motor control applications

Eric Persson, Infineon Technologies

PSMA

Presentation Outline

- Introduction

- Goals

- The challenge: how to control dv/dt?

- Linearizing Cgd

- Multi-phase current-source gate drive

- Hardware results

- Thermal Performance

- Conclusions

- Acknowledgements

VSI is dominant appliance motor drive topology today

- VSI = Voltage Source Inverter

- **Transistor requirements** for VSI:

  - Block voltage in forward direction

  - Conduct current in either direction
    (Can be diode in reverse direction)

  - Short-circuit handling capability

  - Slew-rate can be controlled/limited

  - **LOW COST**

- Additional performance goals:

  - Low conduction loss (in both directions)

  - Low switching loss (dependent only on dv/dt limit – no additional Qrr loss)
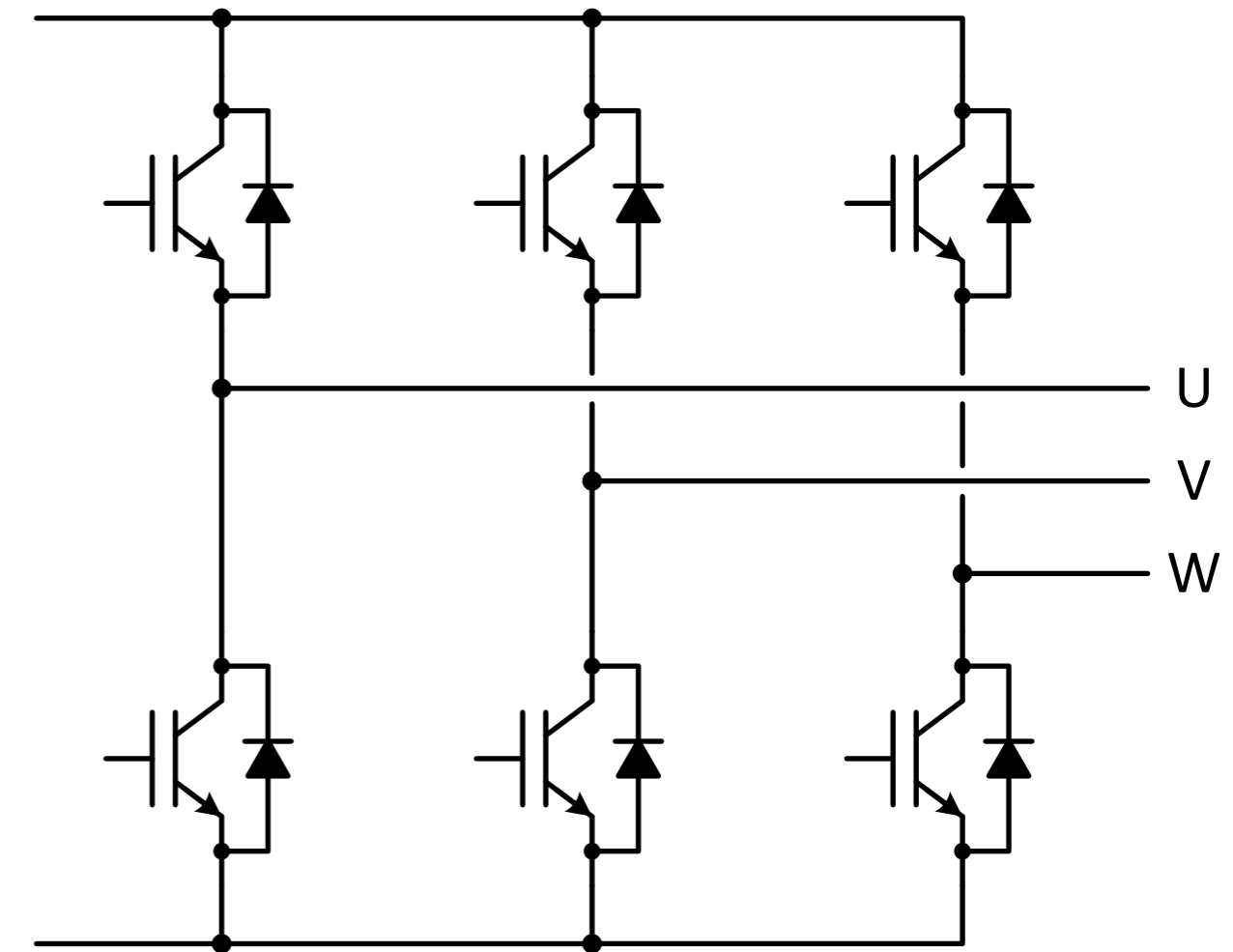
Typical 3Φ VSI using IGBTs

Why is slew-rate control necessary for motor drives?

- Typical low-cost motor windings are inserted in overlapping layers

- This results in large voltage gradients between adjacent coils

- Fast dv/dt waveforms can cause insulation breakdown

  - Due to corona and partial-discharge

- Motor bearings can also be damaged due to dv/dt induced capacitive currents

- **Typical limit is 5 V/ns**

- More expensive motors with concentrated windings may tolerate somewhat faster dv/dt

Motor winding insulation failure due to fast dv/dt
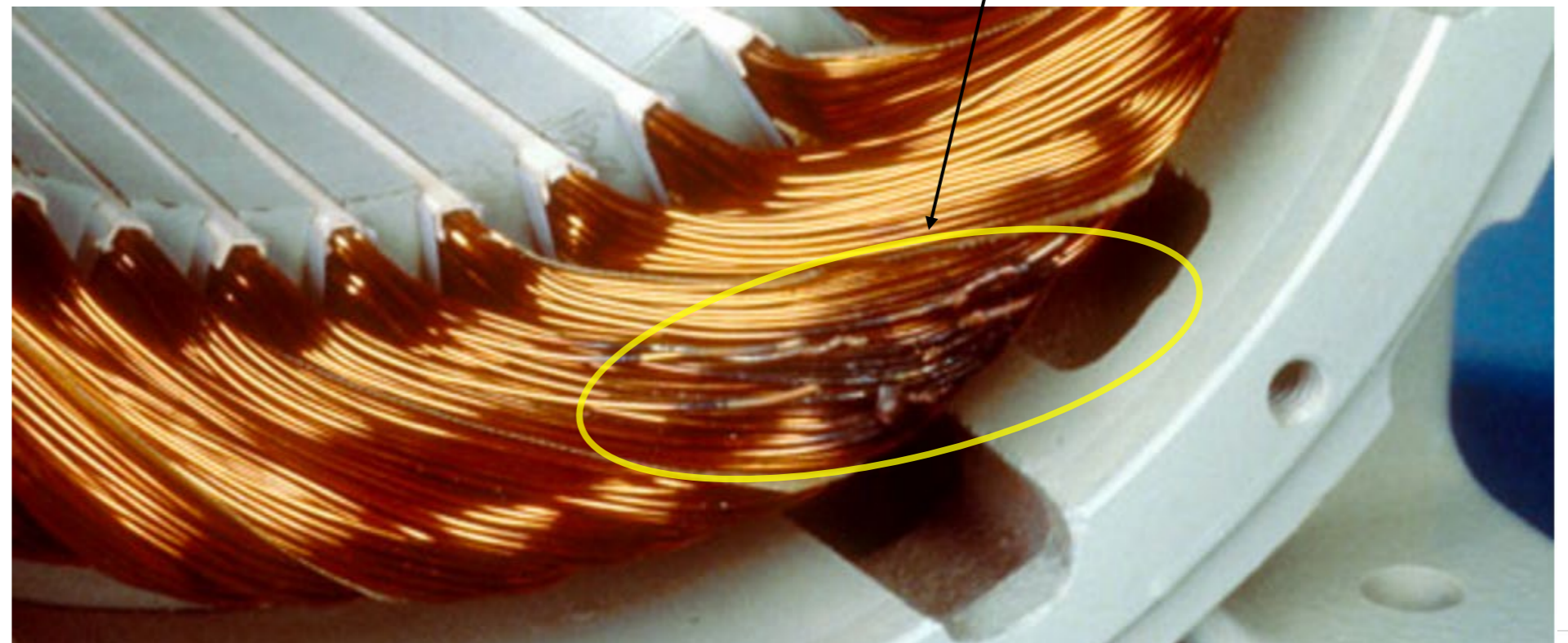
So – why use GaN for motor drives?

- GaN is often considered a very **fast**, high-performance (but **expensive**) switch

- Why does it make sense to **slow its switching speed**
  and use it at **low-frequency** in a low-cost motor drive VSI?

  - Package power dissipation limits output power in today's IPMs

  - **In the same package, GaN can deliver >2X output power**
    because lower conduction and switching loss than Silicon

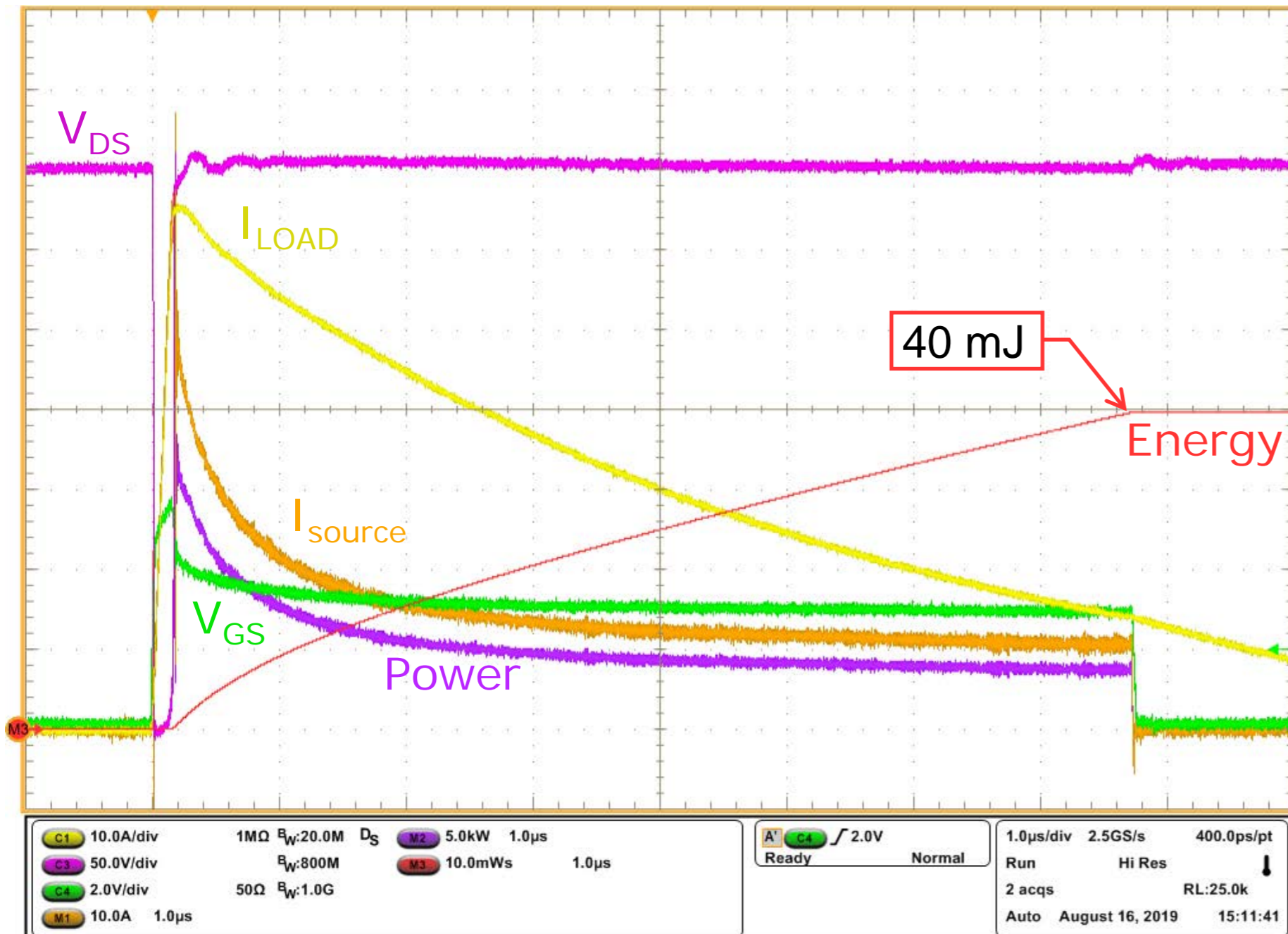 - The value proposition is **2X power density for <2X cost**
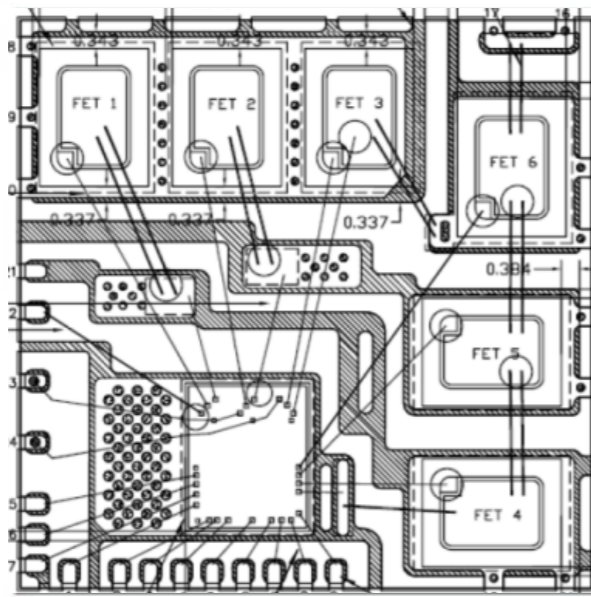
Nano IPM w/ 1.7Ω FREDFETs
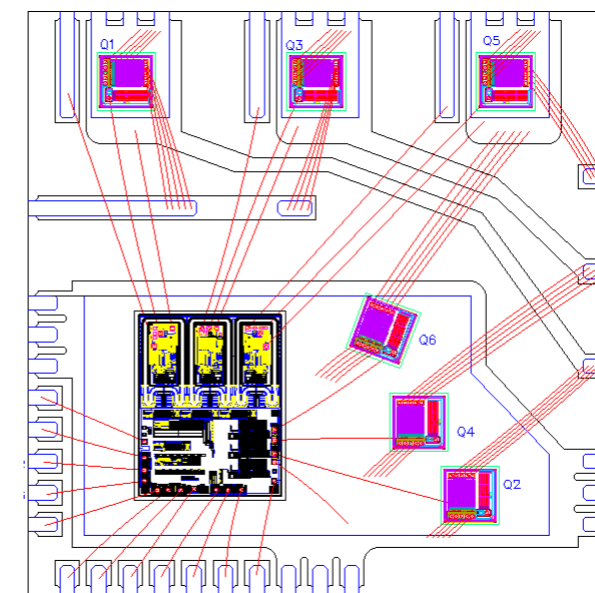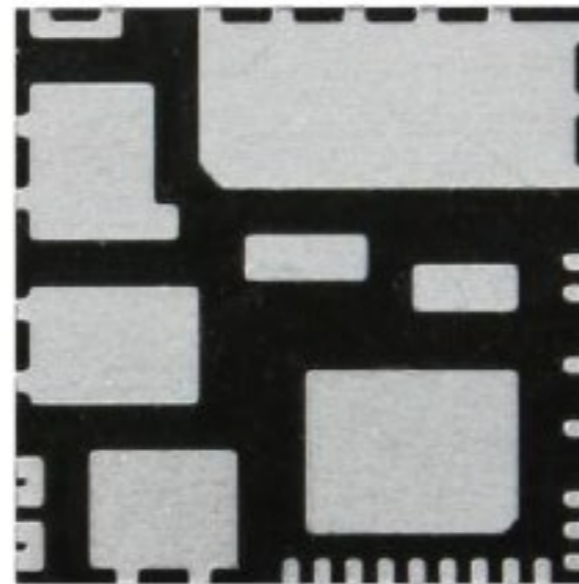
Nano IPM w/ 1Ω GaN

What about short-circuit withstand capability of GaN?

- When driven with the proposed gate drive method, CoolGaN™ has good SCSOA
  - Has a predictable, repeatable current-collapse that reduces I_D similar to IGBT desaturation

Test Conditions:

70 mΩ GaN transistor

350 V Bus

125° C starting temperature

8 µs input pulse-width

Gate drive = 110/10 mA

Infineon is assessing reliability impact of repetitive short-circuit events in a new arpa-e funded program

Goals of this work

- Develop **low-cost** Silicon 3-phase gate-driver IC for CoolGaN™ that can:
  - **Accurately control voltage slew-rate** (dv/dt)
  - (on both turn-on **and turn-off** edges)
  - **Eliminate the need for external passive components** except for bootstrap cap
  - (because packaging passives in the IPM is expensive)
- Package driver IC with 6 GaN transistors in 12x12 mm PQFN package
- Successfully demonstrate controlled slew-rate motor drive
- **Improve power density** of existing 12x12 mm MOSFET IPM **by a factor of 2**
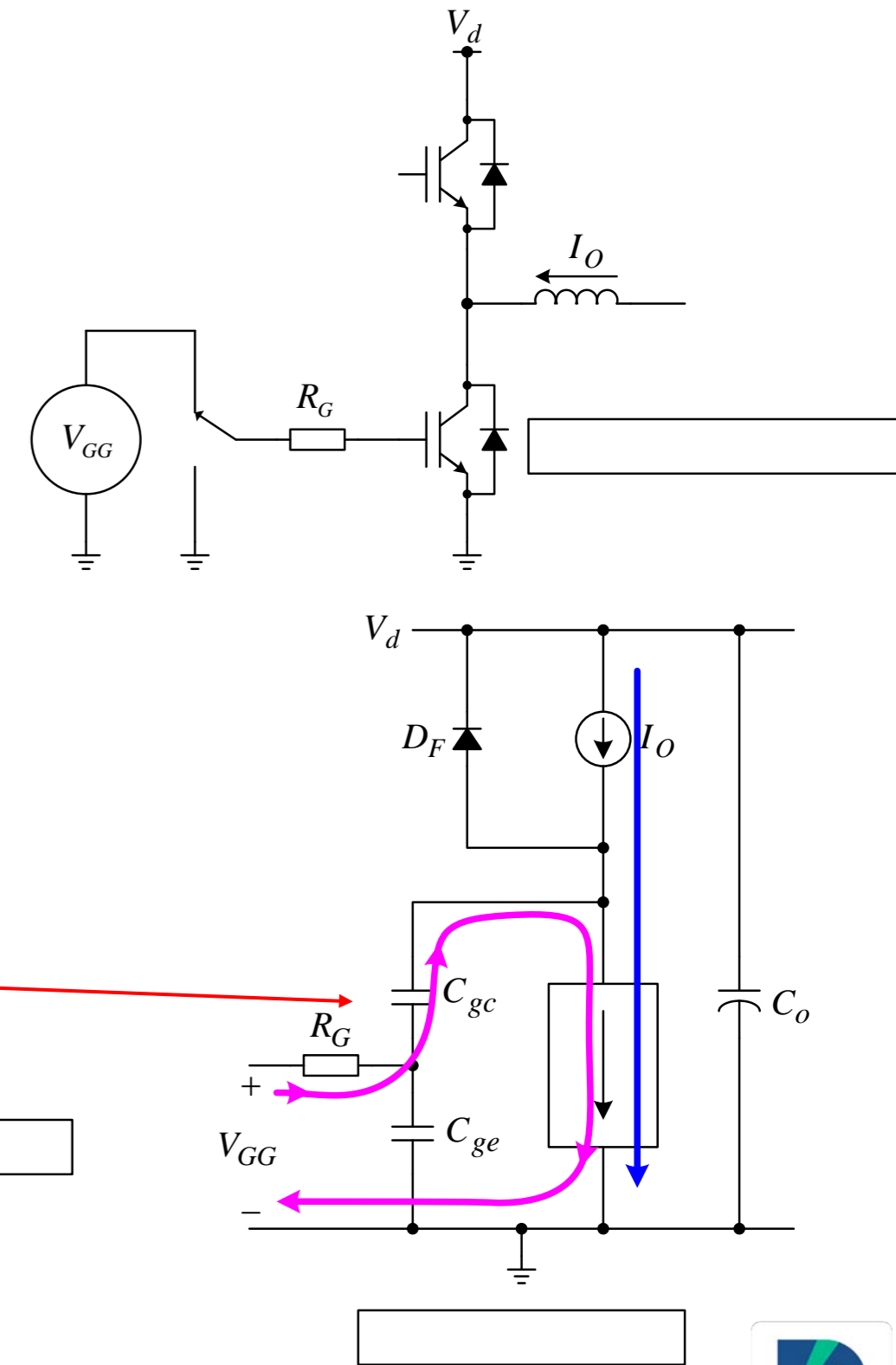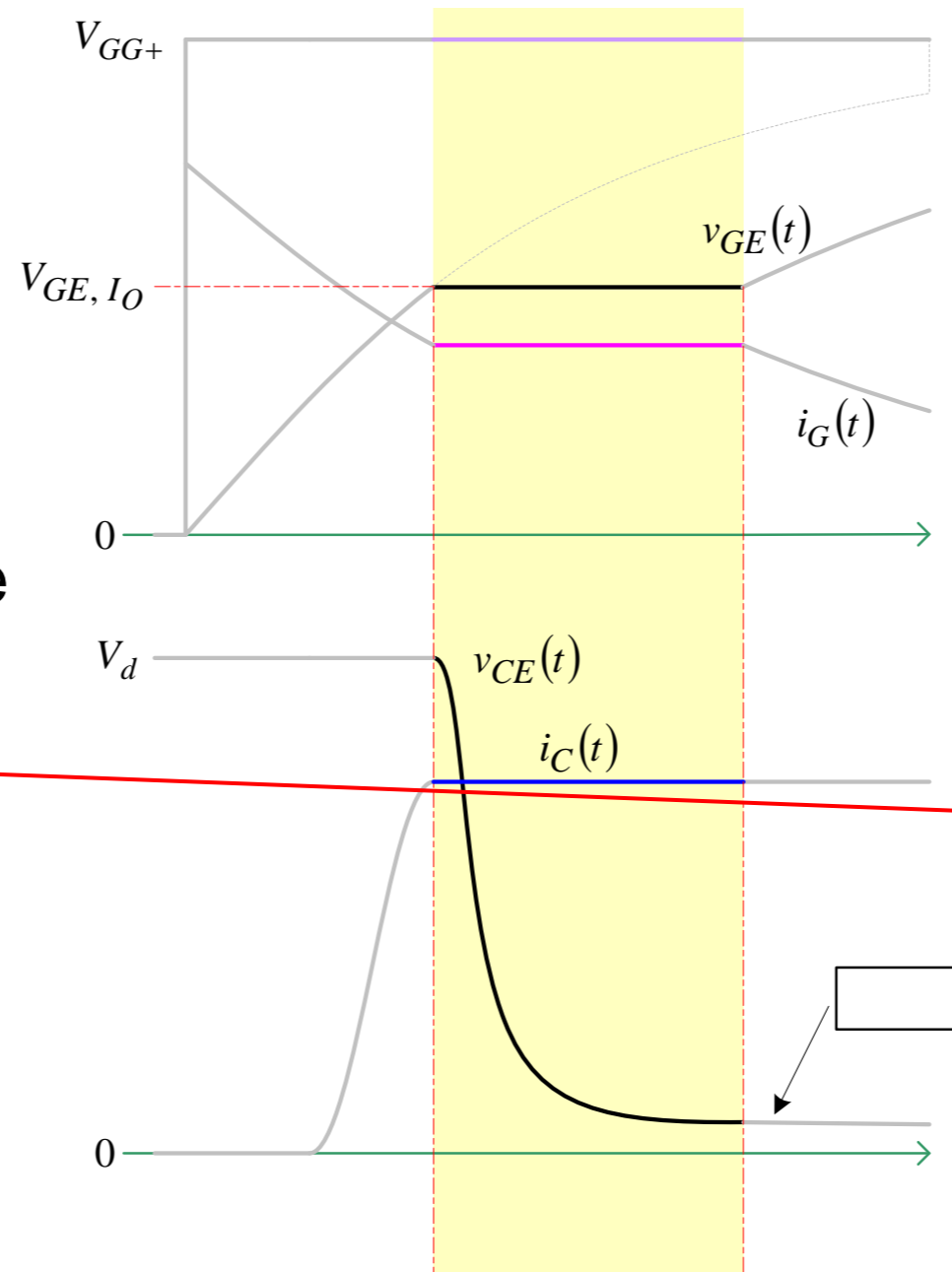
The challenge: how to control dv/dt

- For Si IGBT or FET, adjusting gate drive current is common
  - Simplest way is to **adjust Rg**

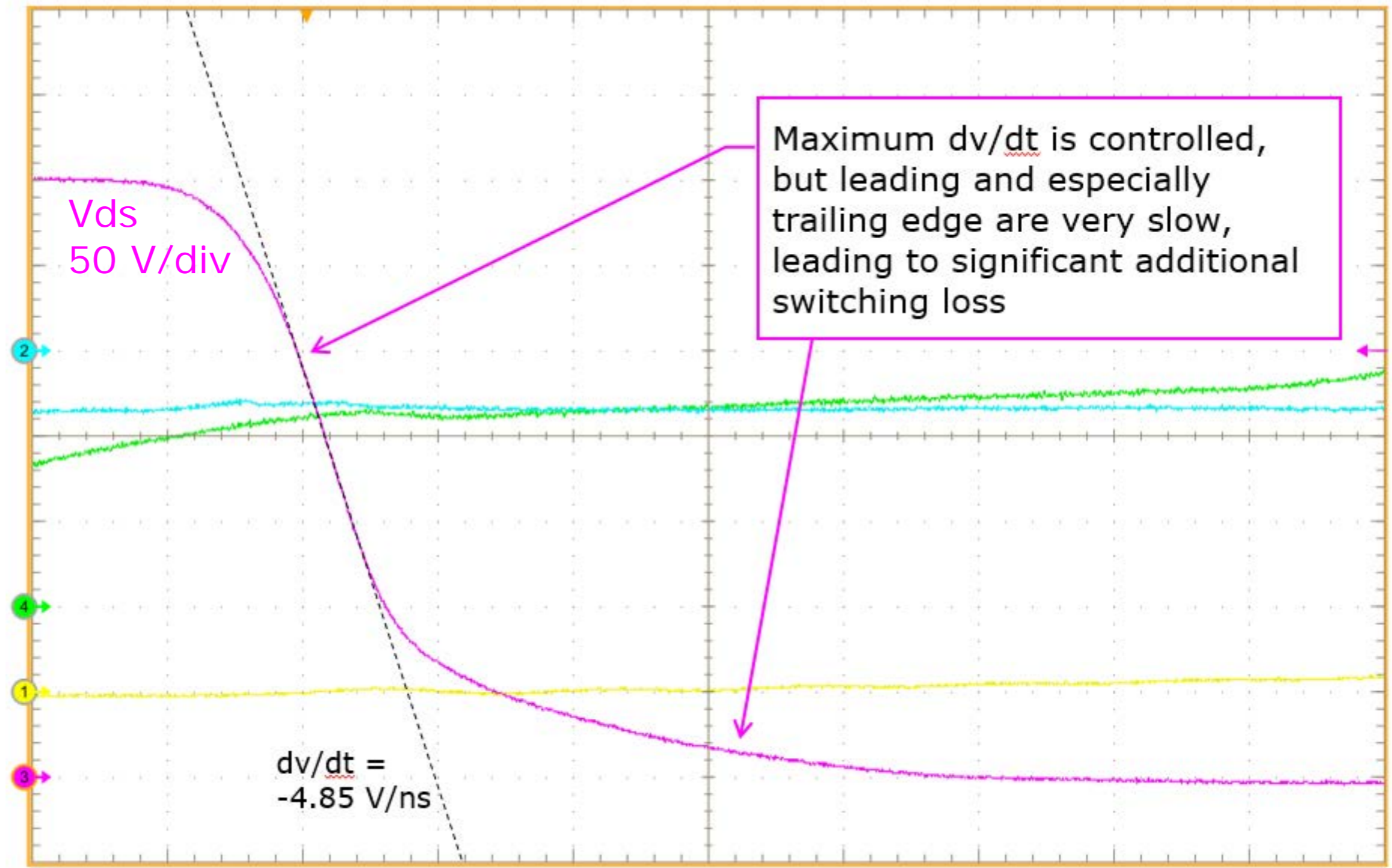During the "plateau" region, **all** of the gate input current is discharging gate-collector capacitance

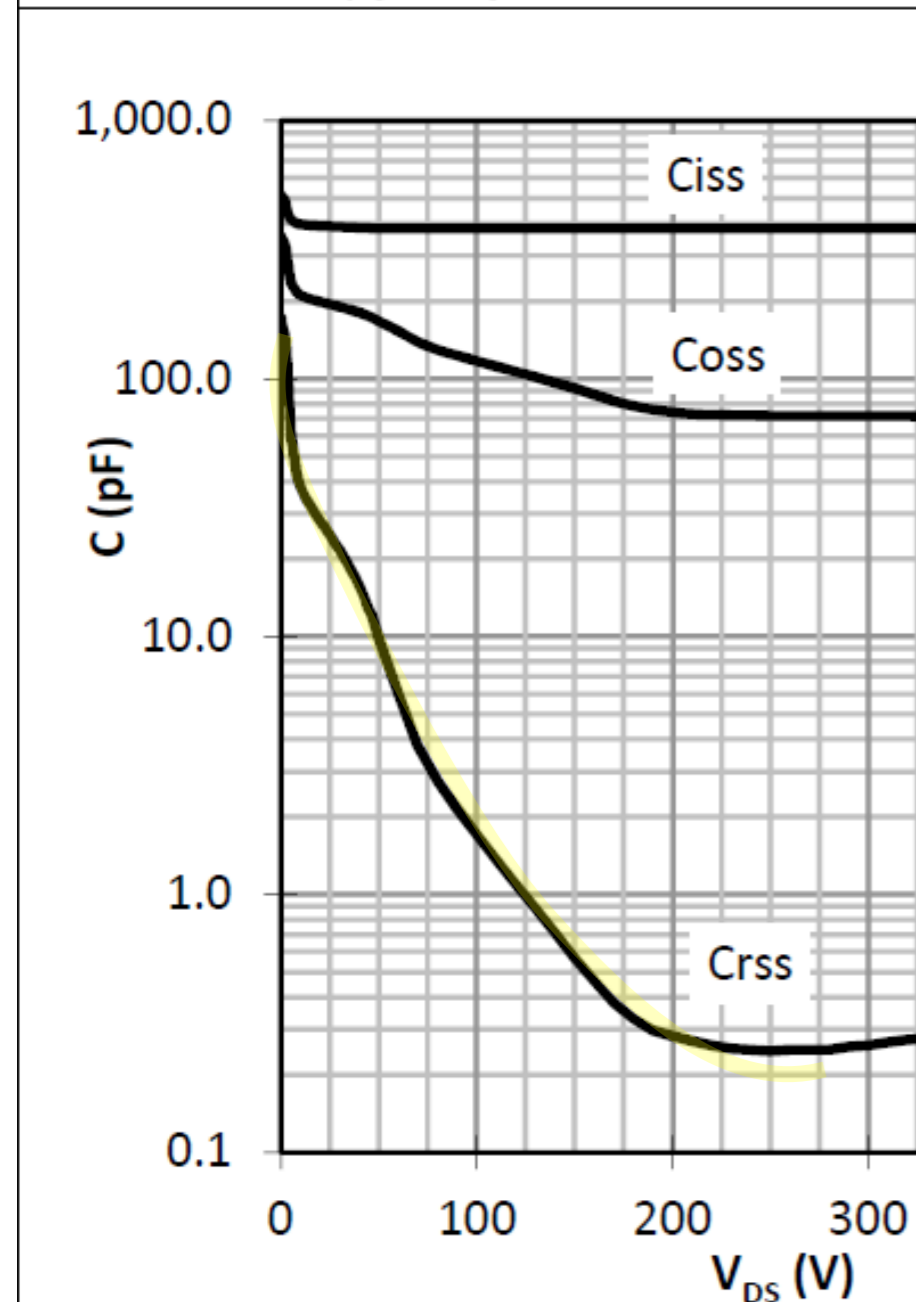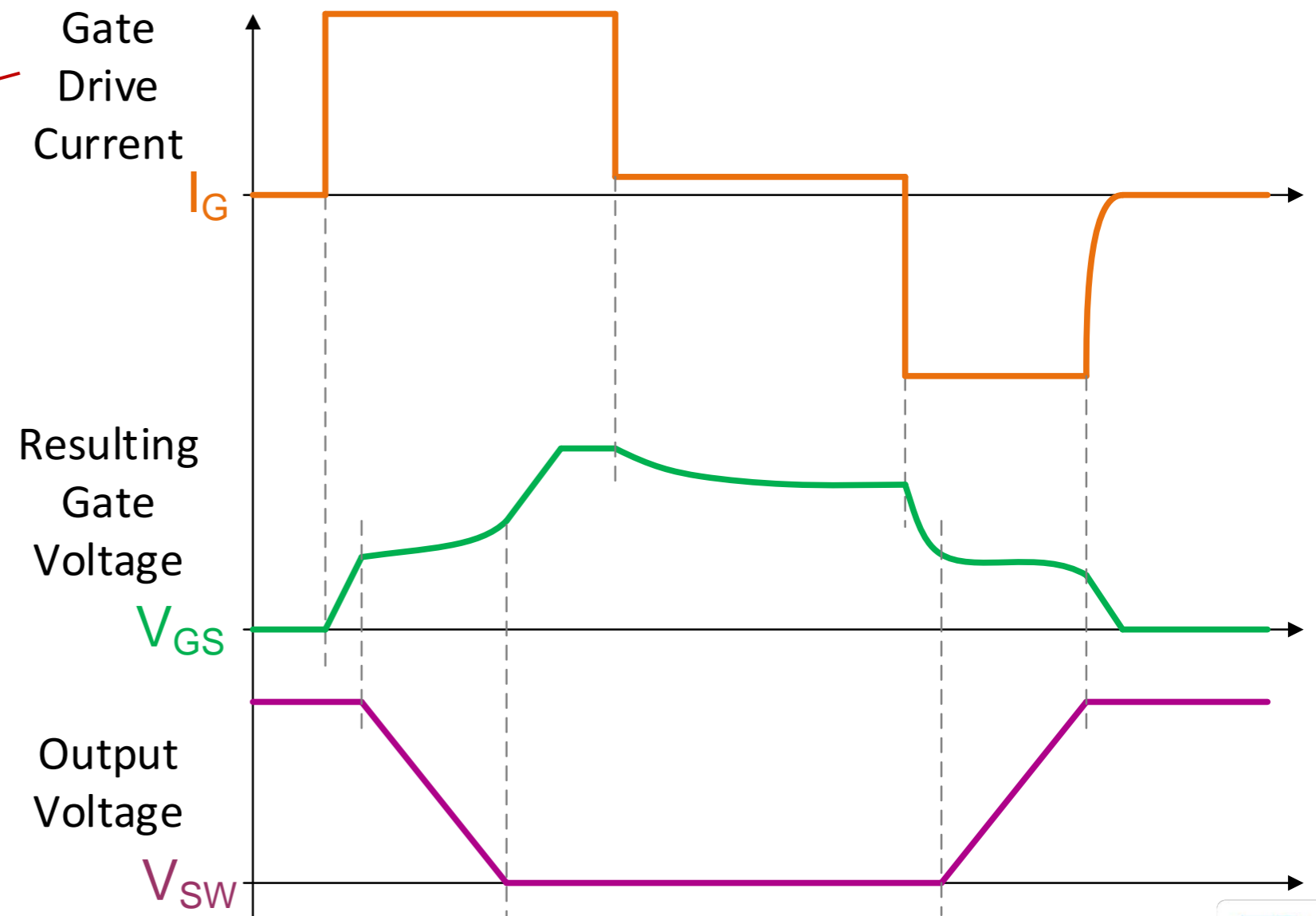**So dv/dt = Ig/Cgc**

But – GaN has very nonlinear Cgd

- Thus – the dv/dt is also very **nonlinear for a fixed gate-drive resistor** (current)

Figure 20   Typ. capacitances

Ciss

Coss

Crss

C (pF)

V_{DS} (V)

Vds
50 V/div

Maximum dv/dt is controlled, but leading and especially trailing edge are very slow, leading to significant additional switching loss

dv/dt =
-4.85 V/ns

The solution: add small linearizing capacitor to Cgd

- Now – a simple fixed-time 2-phase gate drive will provide linear dv/dt control

- Gate charge is doubled, but at 16 kHz PWM, it is still so low it is insignificant

For a 1Ω HEMT

C_{rss} including 1.2 pF linearizing capacitor

C_{rss} of HEMT alone

V_{DS} (V)

Gate Drive Current I_G

Resulting Gate Voltage V_{GS}

Output Voltage V_{SW}
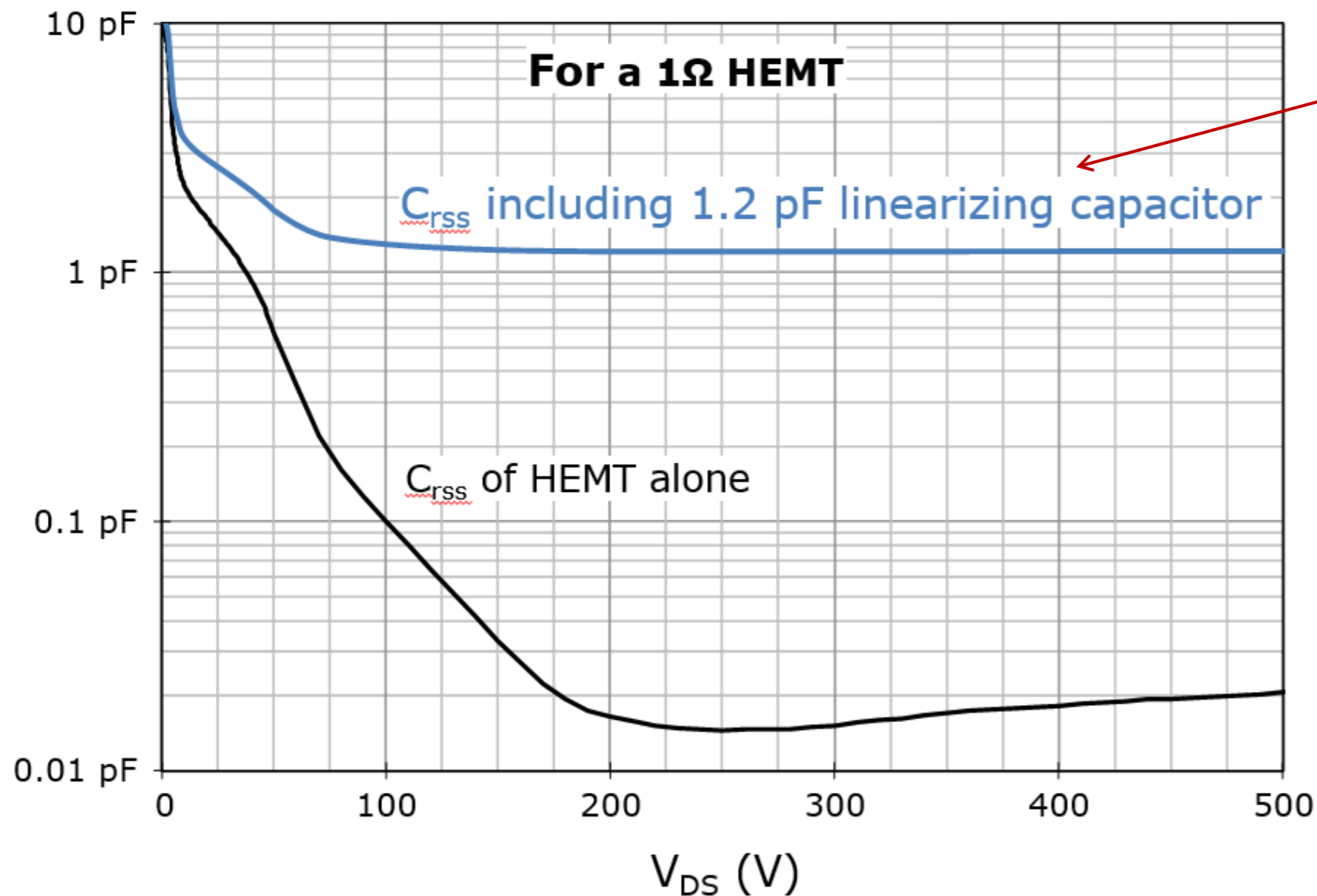
Block diagram of gate driver IC (one channel)

dv/dt-Controlled Gate Driver for CoolGaN
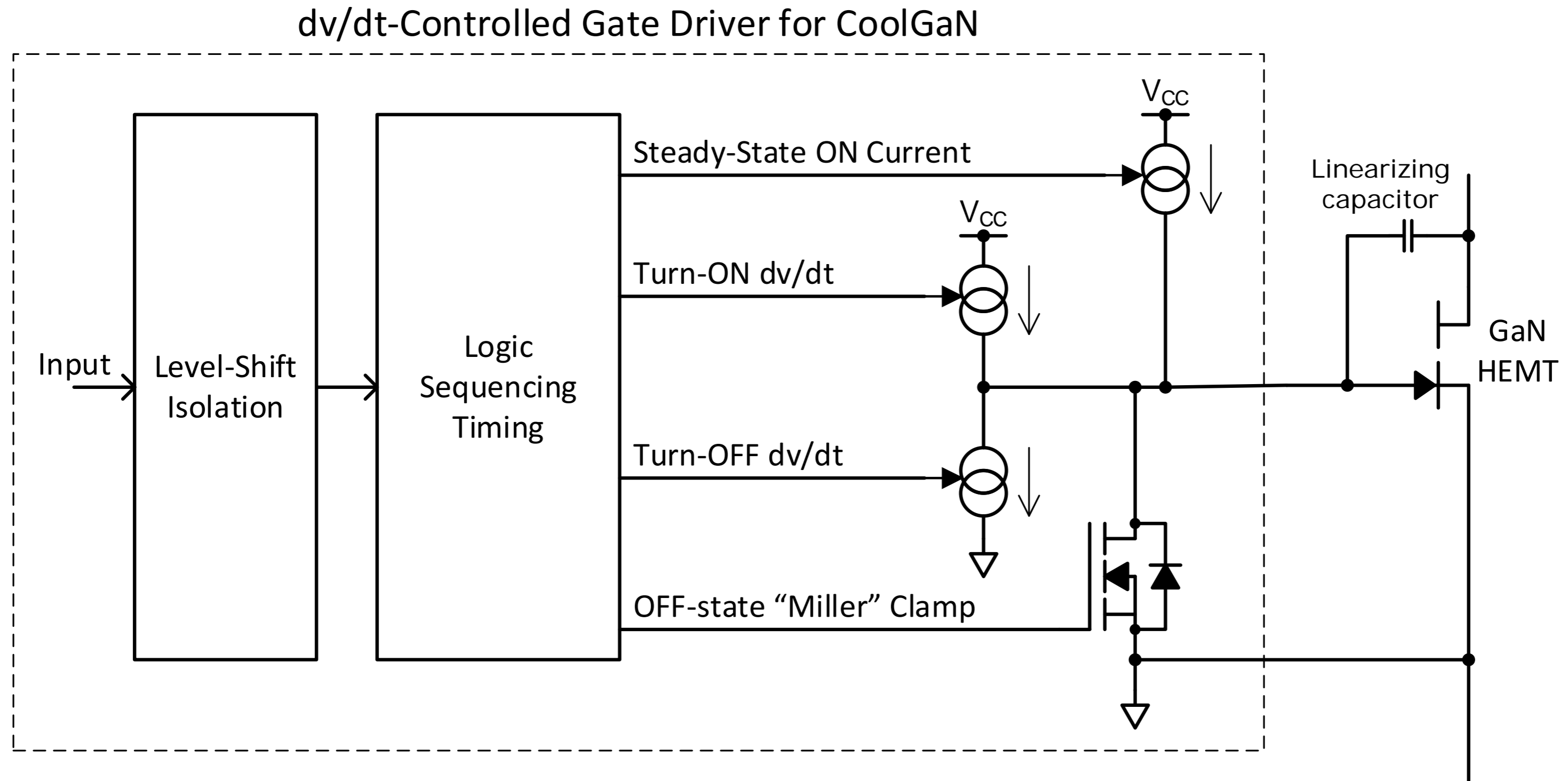
Note no negative gate drive is necessary with slower dv/dt and driver IC in same package as GaN

Gate drive circuit provides precise, linear dv/dt control

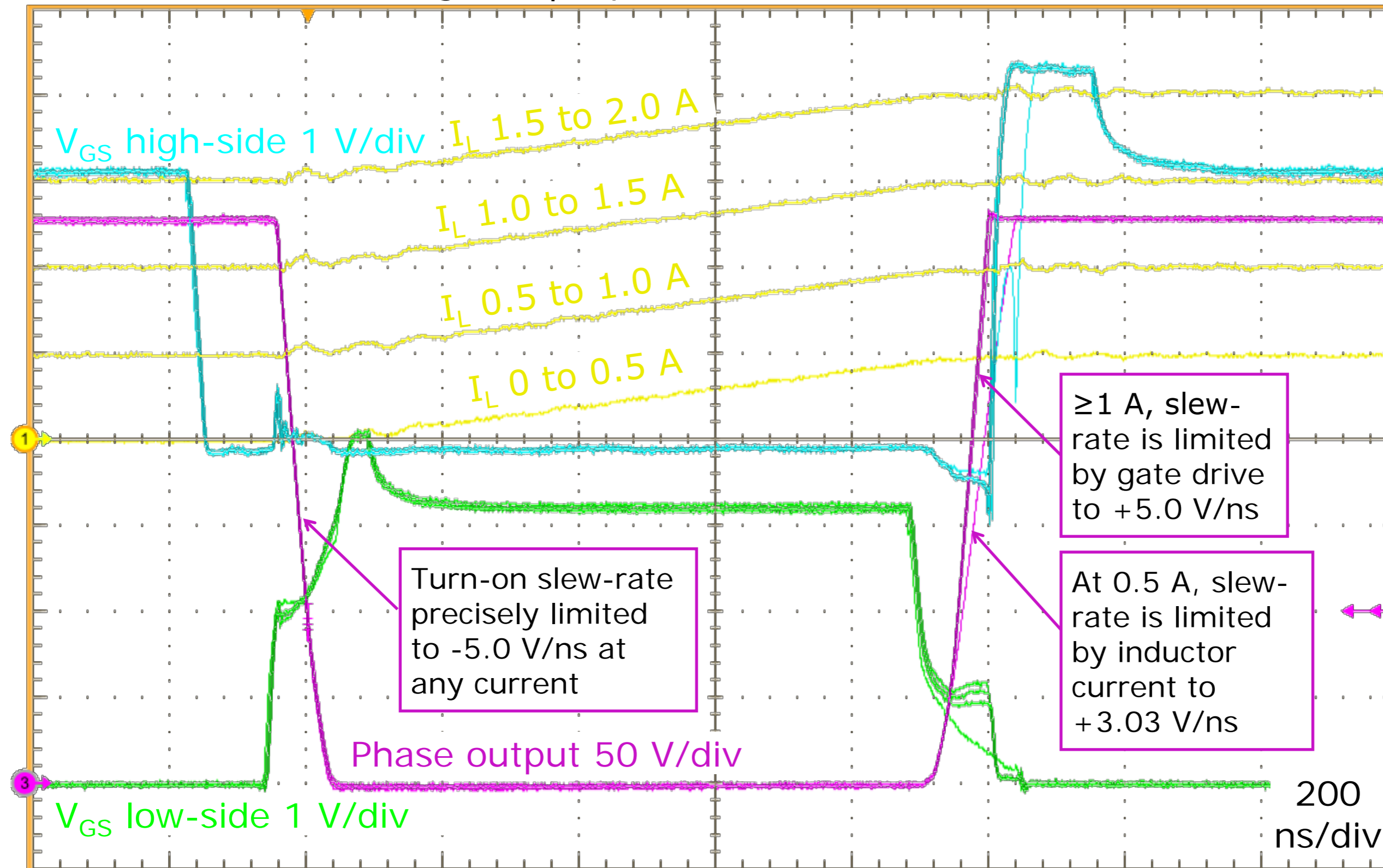Low-side hard-switching 620 µH phase inductance

V_{GS} high-side 1 V/div

I_L 1.5 to 2.0 A

I_L 1.0 to 1.5 A

I_L 0.5 to 1.0 A

I_L 0 to 0.5 A

≥1 A, slew-rate is limited by gate drive to +5.0 V/ns

Turn-on slew-rate precisely limited to -5.0 V/ns at any current

At 0.5 A, slew-rate is limited by inductor current to +3.03 V/ns

Phase output 50 V/div

V_{GS} low-side 1 V/div

200 ns/div

Excellent dynamic transition from slow dv/dt to controlled commutation

PVM E-400 motor, 325 V bus, 720 RPM, 88 W

Phase output 50 V/div

V_{GS} high-side 1 V/div
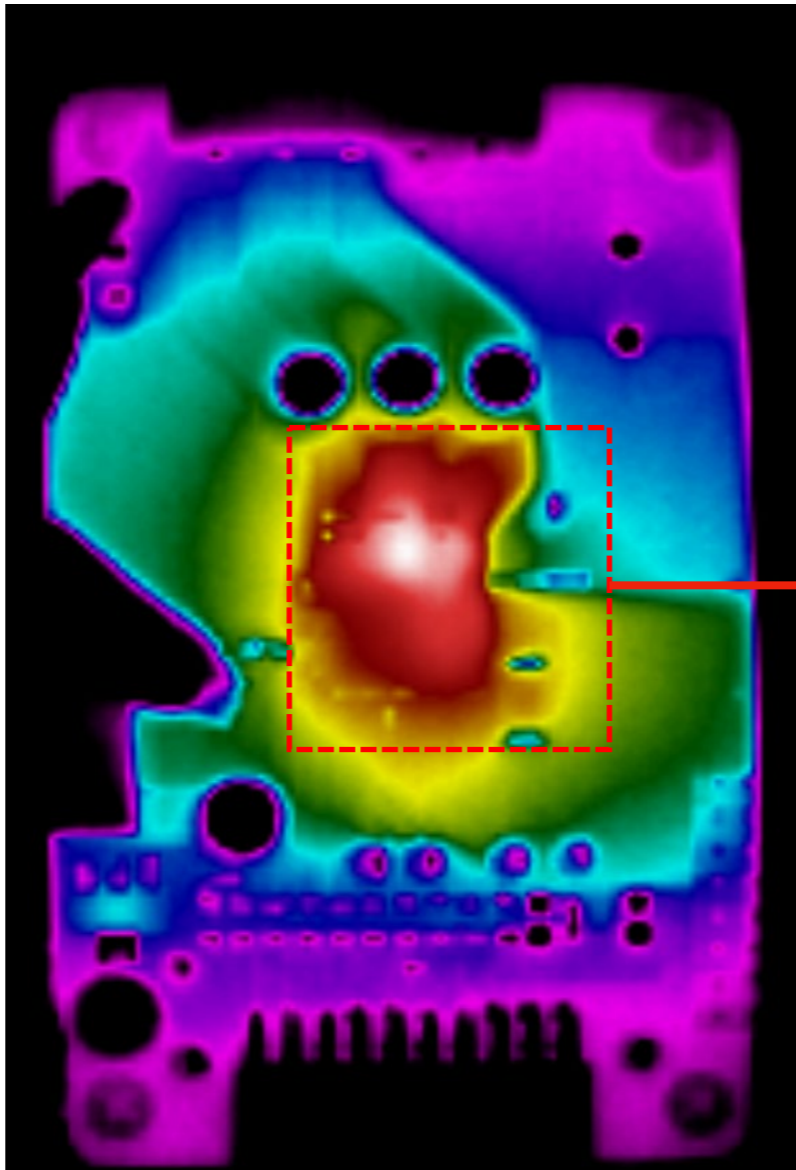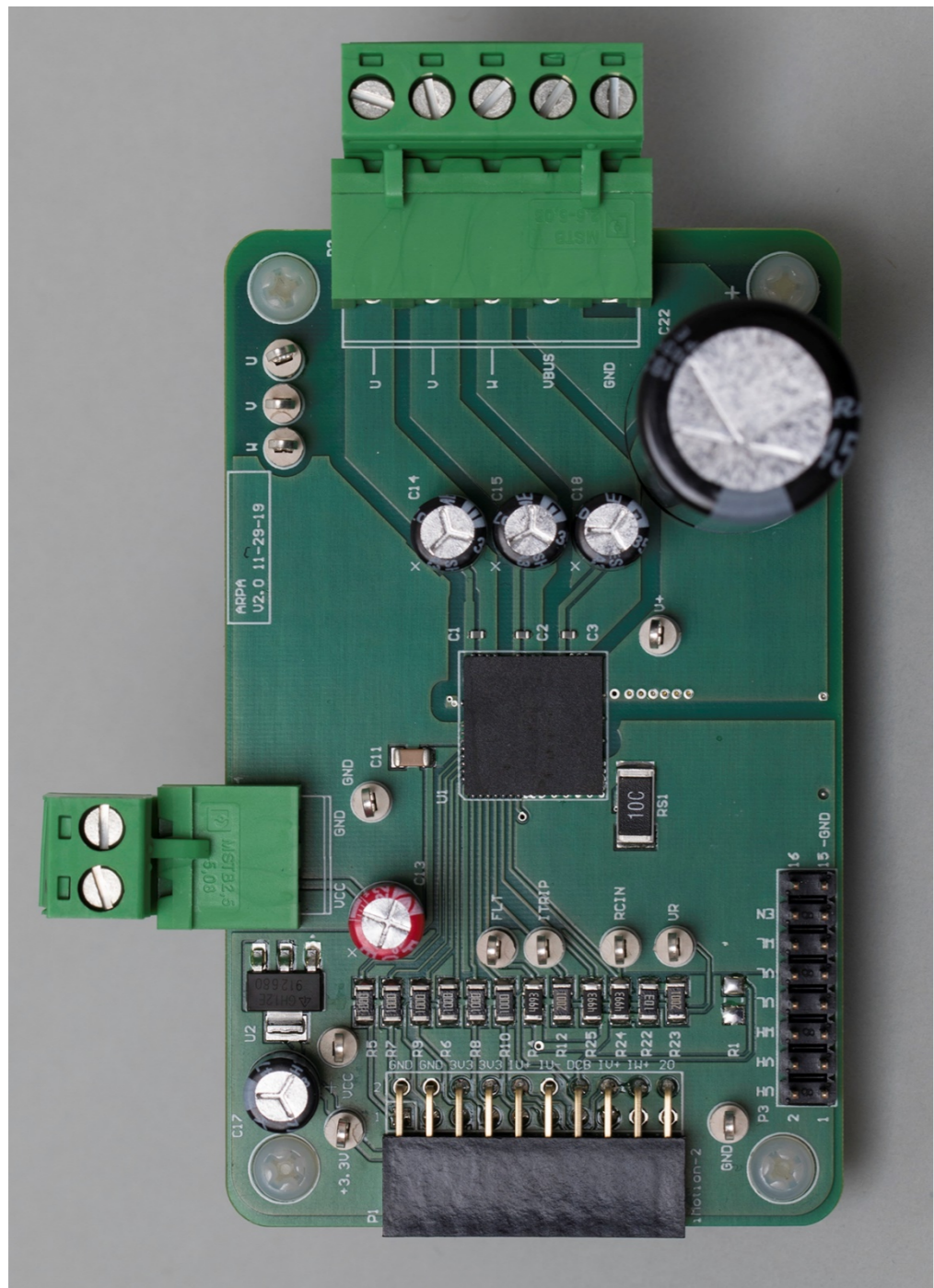
Then hard-switched 5 V/ns slew-rate at end of deadtime

Phase current

Natural slew-rate 0.17 V/ns so transition not completed by end of deadtime

V_{GS} low-side 1 V/div

200 ns/div
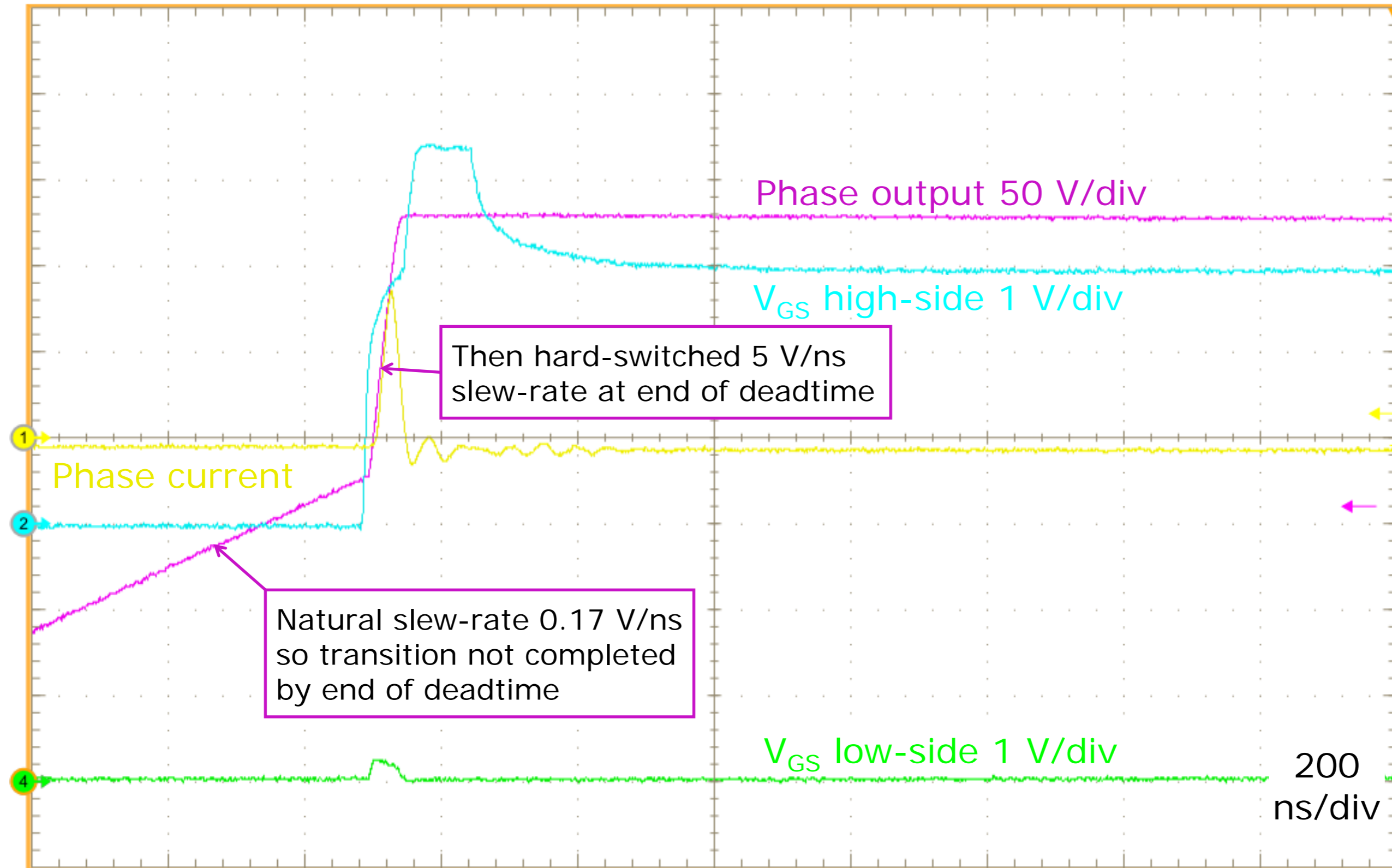
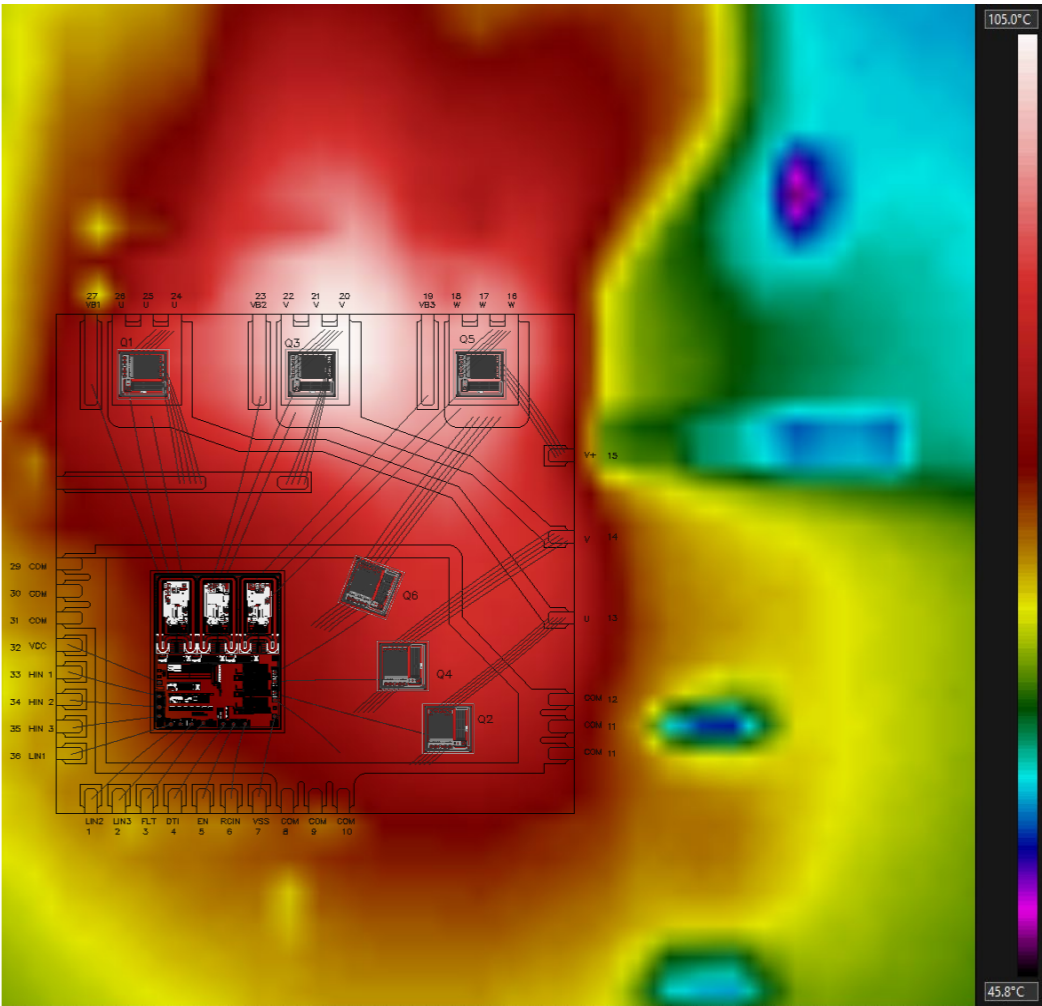# 3-phase motor drive test board temperature rise using thermal imaging

Local Max. surface temperature for each device

Q1	Q3	Q5	Q2	Q4	Q6	IC
97°C	105°C	100°C	90°C	91°C	92°C	84.4

Test Condition: Vbus=320V, Ta=25°C, Fsw=16 KHz, 2-phase modulation
1.07 A rms phase-current, 233 W output

Comparing performance results between existing Si vs GaN solution

- All 3 IPMs compared are 12x12mm PQFN package

- All 3 gate driver ICs are made with the same HVJI Silicon process

- The test is:
  How much power can each technology deliver with 80° C max temp-rise?

Device	Transistor technology	Rds(on) (typ)	Phase current	Motor power	Increase in delivered power
IRSM836 (existing product)	Trench FREDFET	1.5 Ω	0.23 A rms	50 W	(baseline 0%)
IMMxx-046M (in development)	CoolMOS™	1.4 Ω	0.54 A rms	117 W	134%
GaN with new IC driver prototype	Gen 1 CoolGaN™	0.8 Ω	1.04 A rms	226 W	**352%**

- **GaN with controlled dv/dt driver provides clear power density benefit**

- Allowing faster dv/dt will directly reduce switching loss, enabling even higher power

Conclusions

- GaN can be effective solution in low-frequency, slow-dv/dt VSI motor drive

- Switching loss is lower than any competing technology

- Conduction loss can be very low and fit inside IPM due to low specific Rds(on)

- Performance is enabled by low-cost Si gate driver IC in Integrated Power Module

- Smooth waveforms for low EMI signature

- Performance exceeds expectations, >2X power density improvement

- Ongoing work assessing reliability of GaN and SCSOA for motor drive applications

Acknowledgements

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- **Support from Infineon arpa-e gate driver project team**

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  - Steve Clemente, Andrea Gorgerino, Kim Le, Chuan Cheah, Aung Tu, Jeff Fu

Thank you