Thermal simulations of SiC MOSFETs under short-circuit conditions: influence of various simulation parameters

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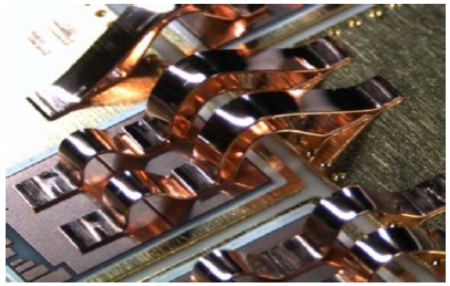
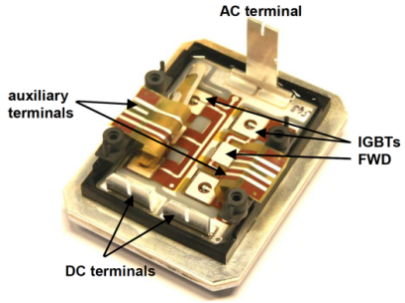
This work was supported by a grant overseen by the
French National Research Agency (ANR-15-CE05-0010) – project HIT-TEMS

Context : top-side connection techniques

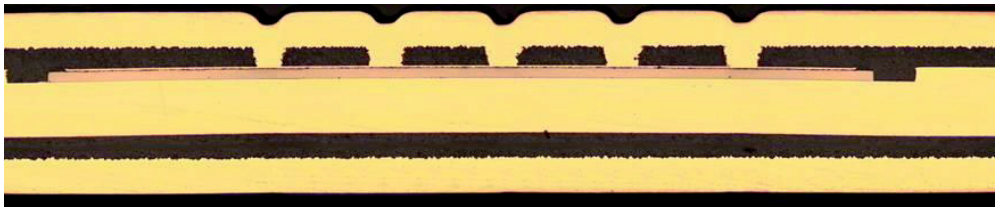
- Bond wires:
  - Mature & economical
  - Relatively high inductance and resistance
  - Limited reliability & robustness
  - Single side cooling



- Many replacement candidates:
  - Al or Cu bonding ribbons or clips
  - Cu posts
  - Sintered/soldered flexible PCB
  - PCB embedding
  - Etc.



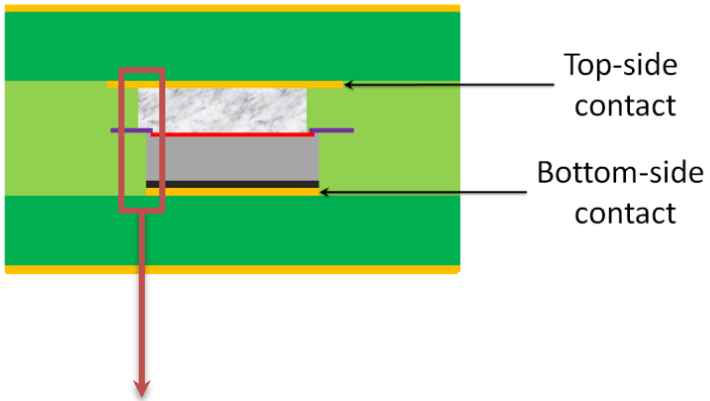
[Beckedahl et al. APEC'13]



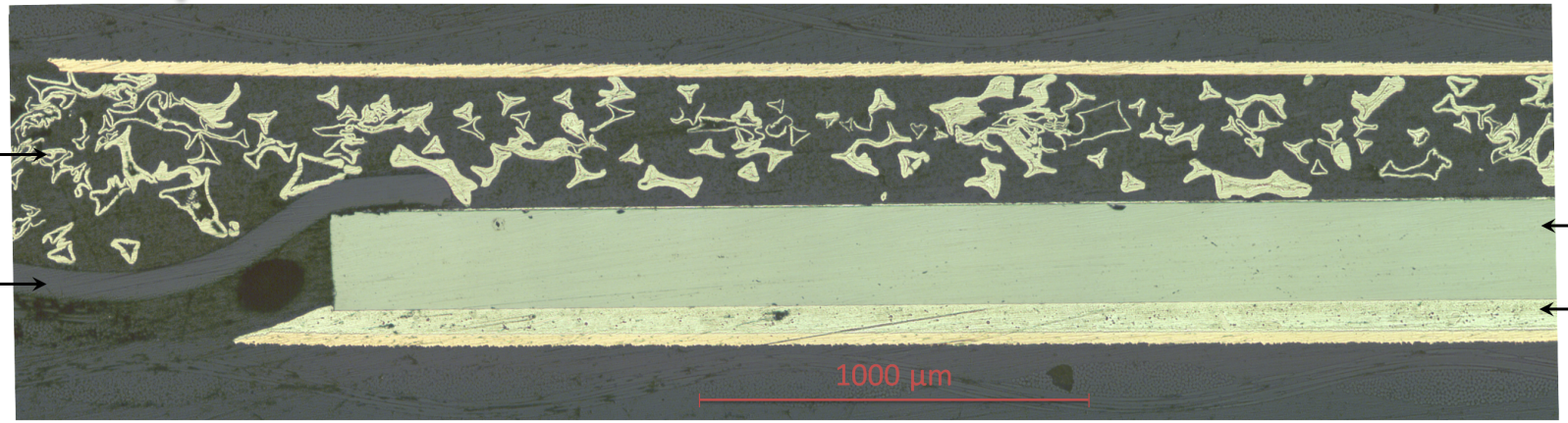
[Gottwald et al. PCIM'14]

Context: proposed die top-side connection technique

Proposed process:



- Process simple and low cost
- Compatible with standard PCB-facilities
- Electrical performances close to that of bond-wires *[Y. Pascal et al, PCIM Europe 2018]*
- Nickel foam with high porosity (96 %) and small cells (350 µm)
- Process not mature, not industrialised



Foam
Mask
Top PCB
Die
Solder
Bottom PCB

Outline

1. Context: an original die top-side connection technique using pressed metal foam
2. Litterature review : junction temperature simulation during short-circuits
3. SiC MOSFET T_j simulation during short-circuits
    1. Proposed model
    2. Influence of the model of power source
    3. Can one simplify Fourier's equation?
    4. Influence of the boundaries
4. Robustness improvement brought by the proposed process
5. Discussion & Conclusion

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Litterature review

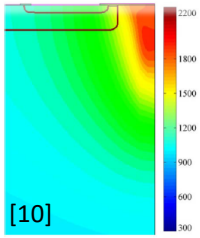
Various simulation parameters:

Ref n°	[14]	[14]	[8]	[9]	[7]	[4]	[10]	[2]	[13]	[12]	[12]	[19]	[15]	[20]	[16]
N. dimensions	1D	EZ3D	EZ3D	EZ3D	3D	2D	2D	3D	1D	1D	1D	1D	1D	1D	1D
power source depth				> 0		> 0		> 0	> 0	> 0	> 0	> 0	> 0	> 0	= 0
power source width				> 0		> 0		> 0	> 0	> 0	> 0	> 0	> 0	> 0	= 0
$0 \neq d(\lambda, cp)/dT$	SiC only	SiC only	SiC only	no						no	yes		no		SiC only
Top boundary	∇T=0	∇T=0	∇T=0			∇T=0		∇T=0	∇T=0	∇T=0	∇T=0	∇T=0	∇T=0	∇T=0	∇T=0
Bot boundary	T=Ta	T=Ta	T=Ta			T=Ta		T=Ta	RC	T=Ta	T=Ta	T=Ta	RC	T=Ta	RC
E-Field profil				Δ		Δ		Δ	□	Δ	Δ	Δ	Δ	Δ	δ

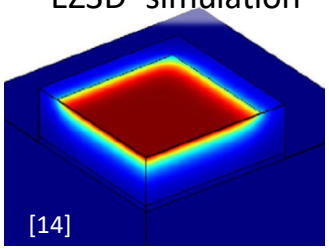
References detailled in the paper

2D vs. EZ3D vs. 3D simulations:

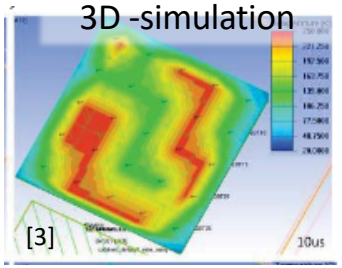
2D -simulation



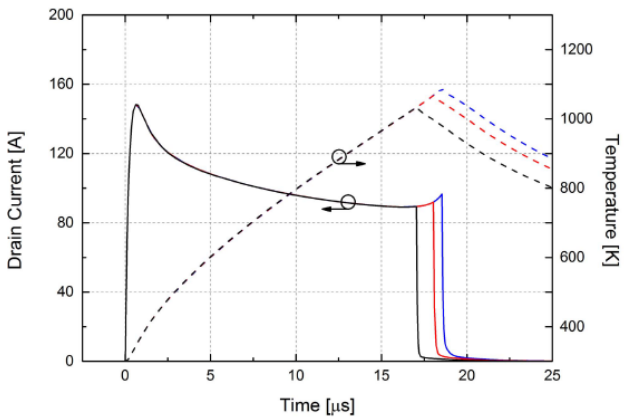
EZ3D -simulation



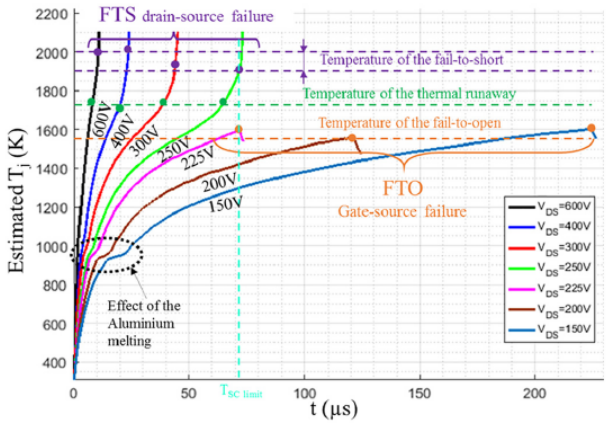
3D -simulation



Some simulation results:



[Romano et al. IEEE JESTPE, 2016]



[Boige et al. Microelec. Rel. 2018]

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Proposed model (1)

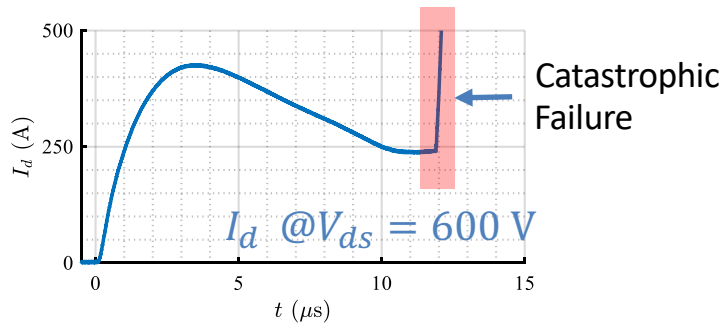
- 1D-model
- Heat equation : $\rho c_p \frac{\partial T}{\partial t} - \frac{d}{dz}(\lambda \nabla T) = \dot{q_v}$
- Dicretised equation: finite difference method, solved in Matlab

  with: $\Delta t = 10$ ps, $\Delta z = 150$ nm
- Boundaries: irrelevant
- Power source :

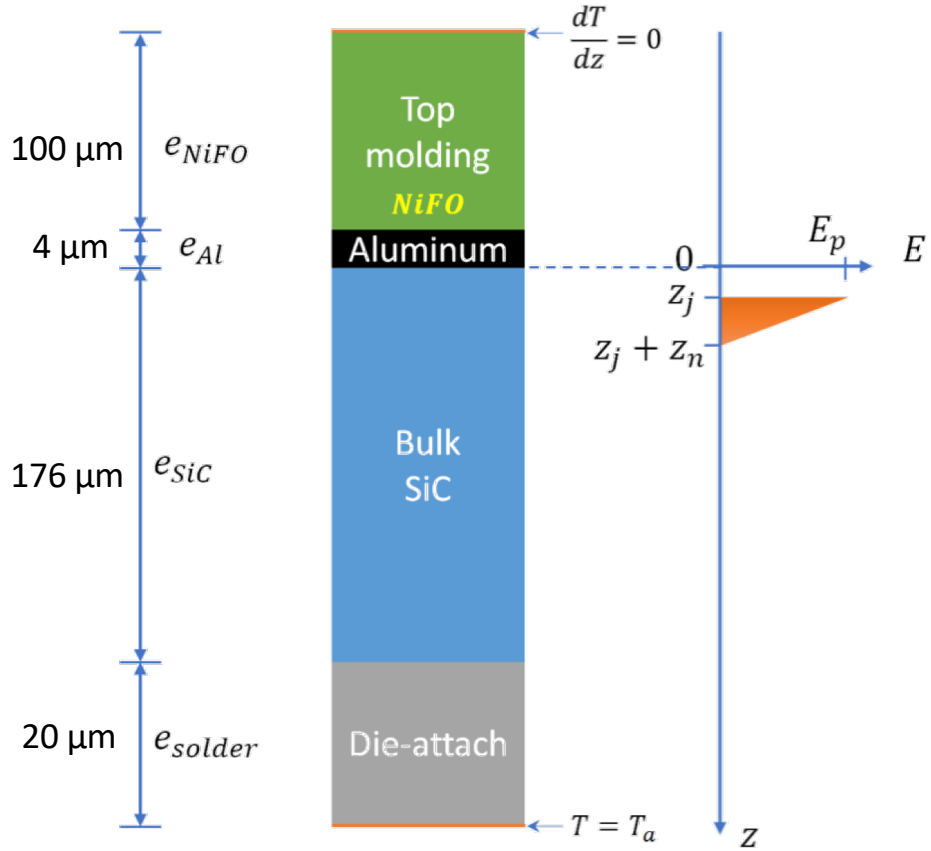
$z_n = \sqrt{\frac{2\epsilon_{SiC} V_{ds}}{q N_d}} \approx 8\ \mu\text{m}$ ← Depletion layer width

$z_j = 1\ \mu\text{m}$ ← Depletion layer depth

Current waveform taken from measurements:



Short-Circuit duration: 11 μs (until failure)



Proposed model (2)

- Temperature dependance of (λ, c_p) taken into account for :
  - Aluminum, Nickel, SiC

- Top molding : nickel foam & epoxy filler homogenised:

$$\lambda_{NiFO} = \alpha_{Ni} \cdot \lambda_{Ni} + (1 - \alpha_{Ni}) \cdot \lambda_{epoxy}$$

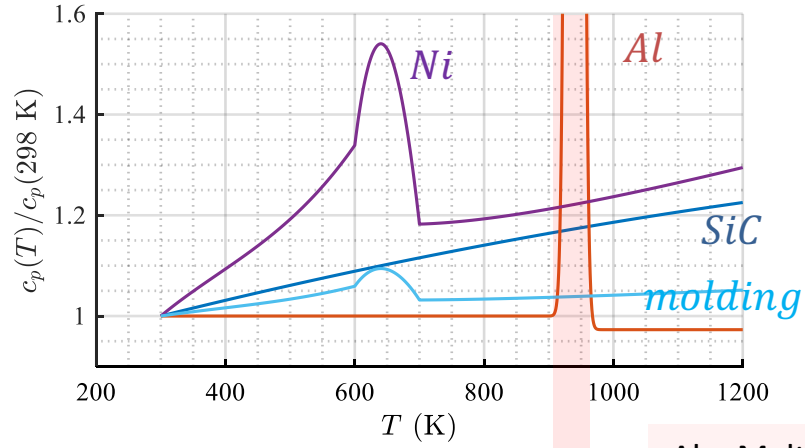
Idem for density and thermal capacity

$\alpha_{Ni} = 30\ \%$: our process

$\alpha_{Ni} = 0\ \%$: pure resin ≈ discrete wire-bonded die

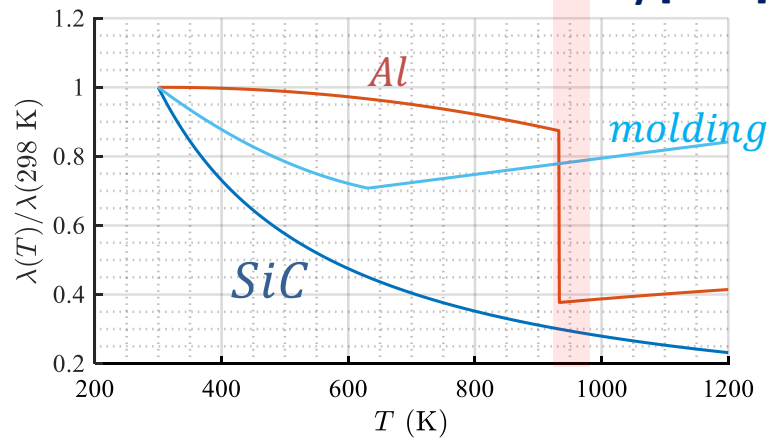
@298 K	λ (W/mK)	c_p (J/K· kg)	ρ (kg/m^3)
Aluminium	239	910	2699
Nickel	91	443	8902
Epoxy	0.3	900	1250
Molding	27.6	763	3546
SiC	353	1031	3211
Solder	60	160	7400

Normalised heat capacity [25-29]



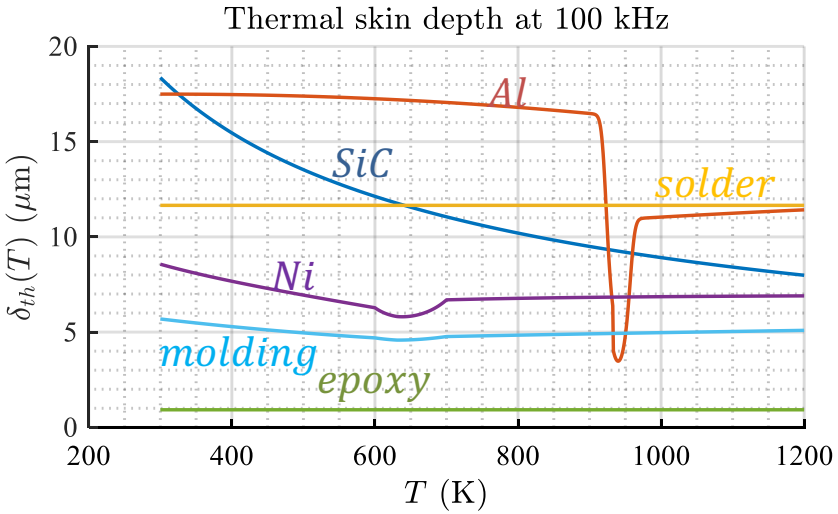
Alu. Melting

Normalised thermal conductivity [25-29]



On the choice of boundary conditions

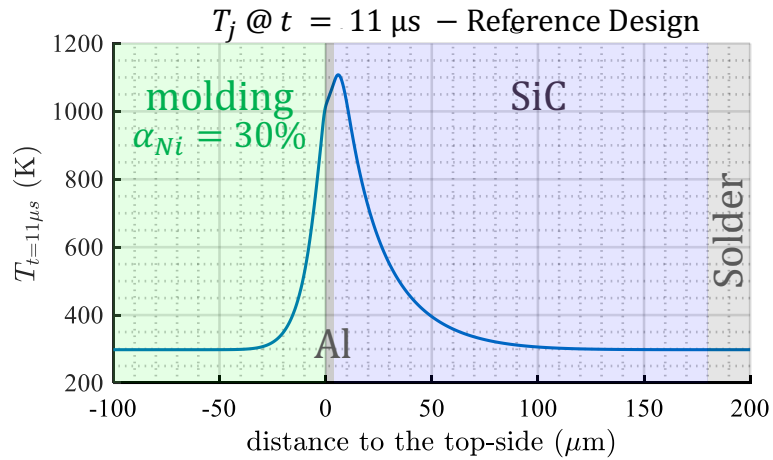
- Short-circuit duration = 11 µs ~ 100 kHz
- Thermal skindepth: $\delta_{th} = \sqrt{\frac{\lambda}{\rho c_p \pi f}}$



- ➢ Heat does not reach solder
- ➢ No energy stored in the epoxy molding

⇒ Limited impact of the bottom-side boundary condition
⇒ No need to model the molding

Temperature at the end of the short-circuit

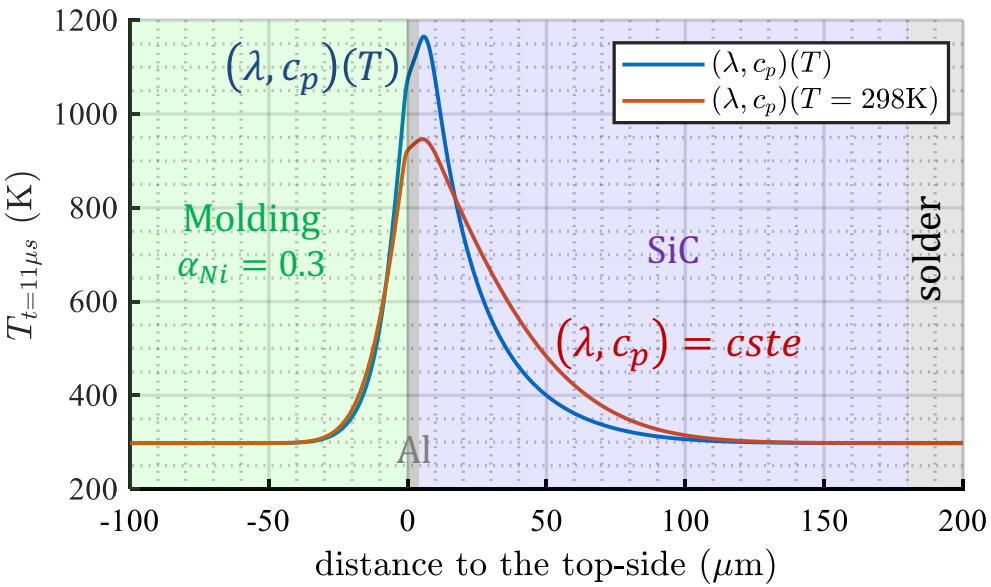


Energy storage:

	α_{Ni}= 0 Pure epoxy	α_{Ni}= 0.3 30 % nickel
Molding	4 %	18 %
Aluminum	13 %	10 %
SiC	83 %	72 %

Impact of the (λ, c_p) temperature dependance?

Temperature at the end of the short-circuit



Energy storage:

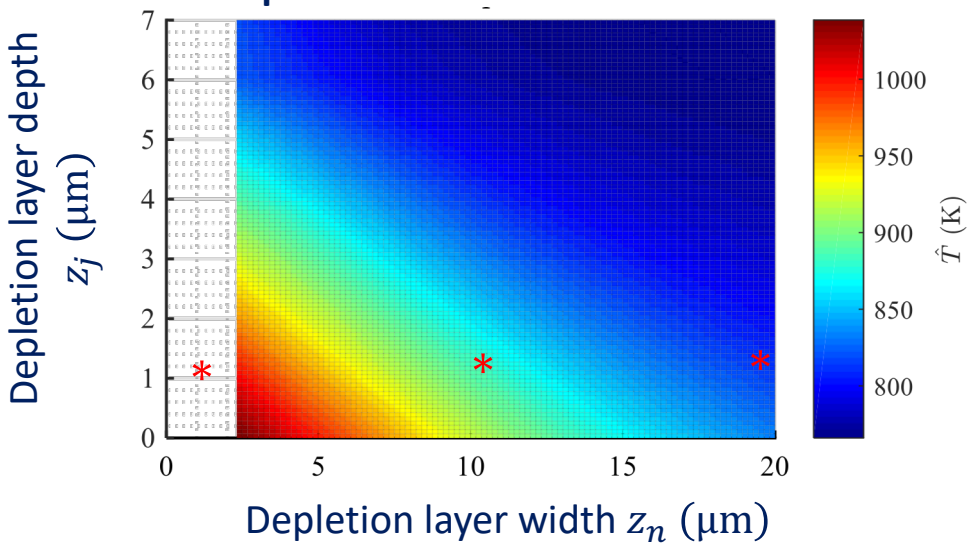
	α_{Ni}= 0 Pure epoxy	α_{Ni}= 0.3 30 % nickel
Molding	4 %	18 %
Aluminum	**13 %**	10 %
SiC	83 %	72 %

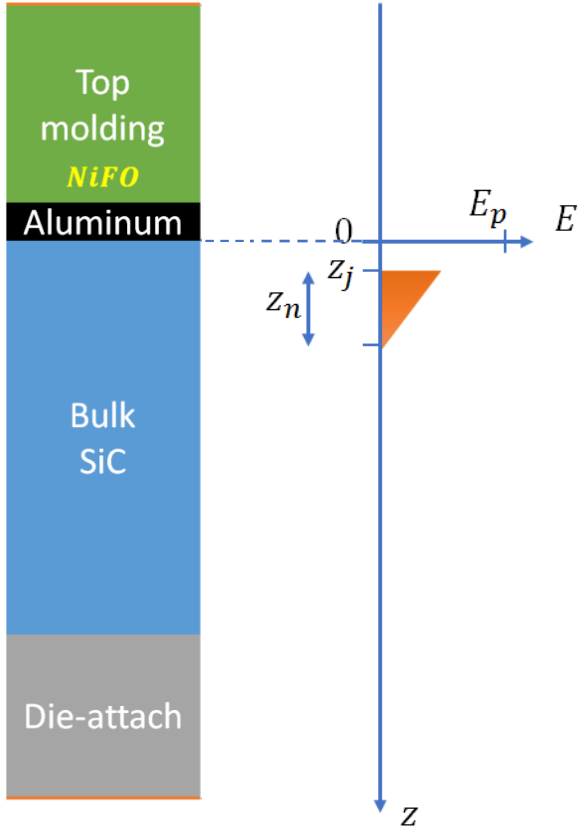
⇒ high impact of the temperature dependance of (λ, c_p)
The aluminium layer should be modeled

Influence of the model of power source

- Litterature review:
  - Field shape: triangular vs. trapezoidal
  - Depletion layer: width $\in [0,\ 21]$ µm $\Leftrightarrow N_d \in [2 \cdot 10^{15}, 6 \cdot 10^{17}]\ \mathrm{cm}^{-3}$
    depth $\in [0,\ 1.1]$ µm

Peak temperature at the end of the short-circuit





(Not to scale)

⇒ Great influence of the power source model on the peak temperature

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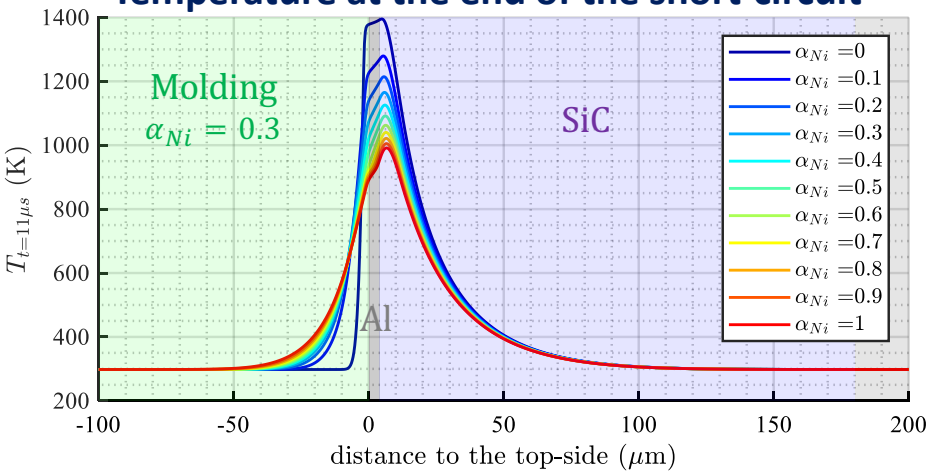
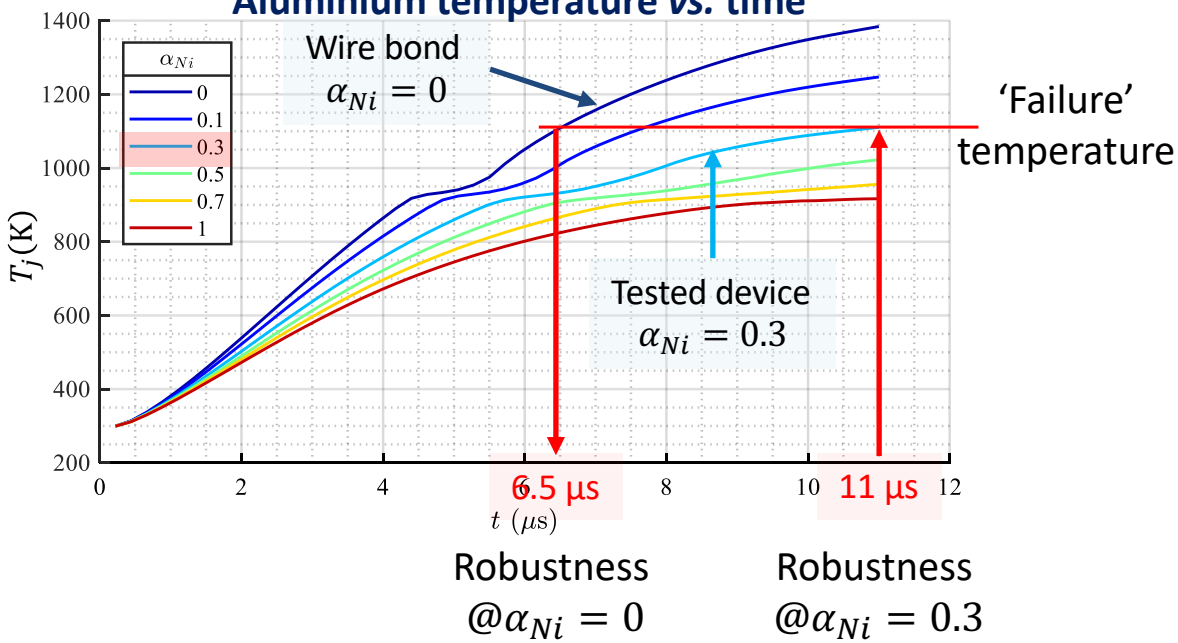
Robusteness improvement @$\alpha_{Ni} > 0$

- Device simulated using various nickel proportions α_{Ni}:
  - from 0 : molding = pure epoxy ~ wire bond
  - Through 0.3 : our embedding process
  - To 1 : molding = pure nickel

Temperature at the end of the short-circuit



Aluminium temperature *vs.* time



@$\alpha_{Ni} = 0$, the 'failure' temperature is reached 4 µs before @$\alpha_{Ni} = 30\%$

⇒ this could correpond to a 60 % improvement when using Foam rather than bond wires

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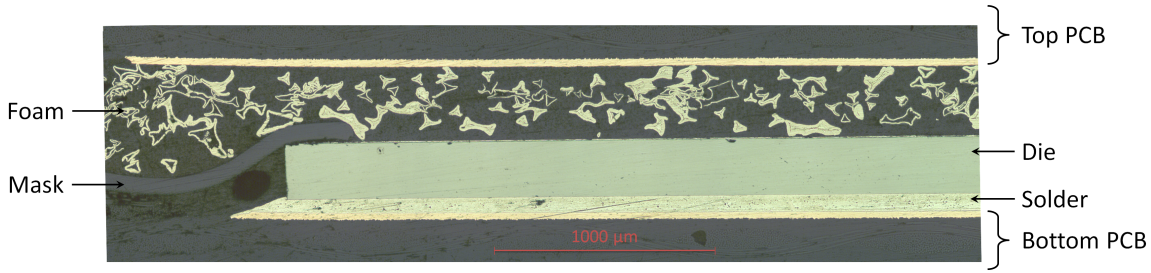
Discussion & Conclusion

- The influence of some simulation parameters has been studied:
  - Limited impact of the choice of bottom-side boundary conditions
  - High impact of the temperature dependance of (λ, c_p)
  - The aluminium layer should be modeled, the molding may not
  - Great influence of the power source model
- Other parameters are yet to be assessed:
  - 1D model?
  - Effect of SiC doping concentration on (λ, c_p)?

- On the process with top-side connection using pressed metal foam:
  - Simulated time to failure increased by 4 µs when using $\alpha_{Ni} = 30\ \%$ rather than $\alpha_{Ni} = 0$



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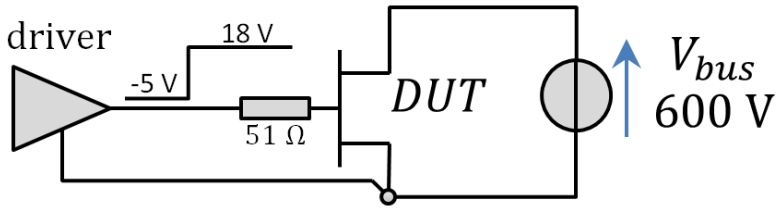
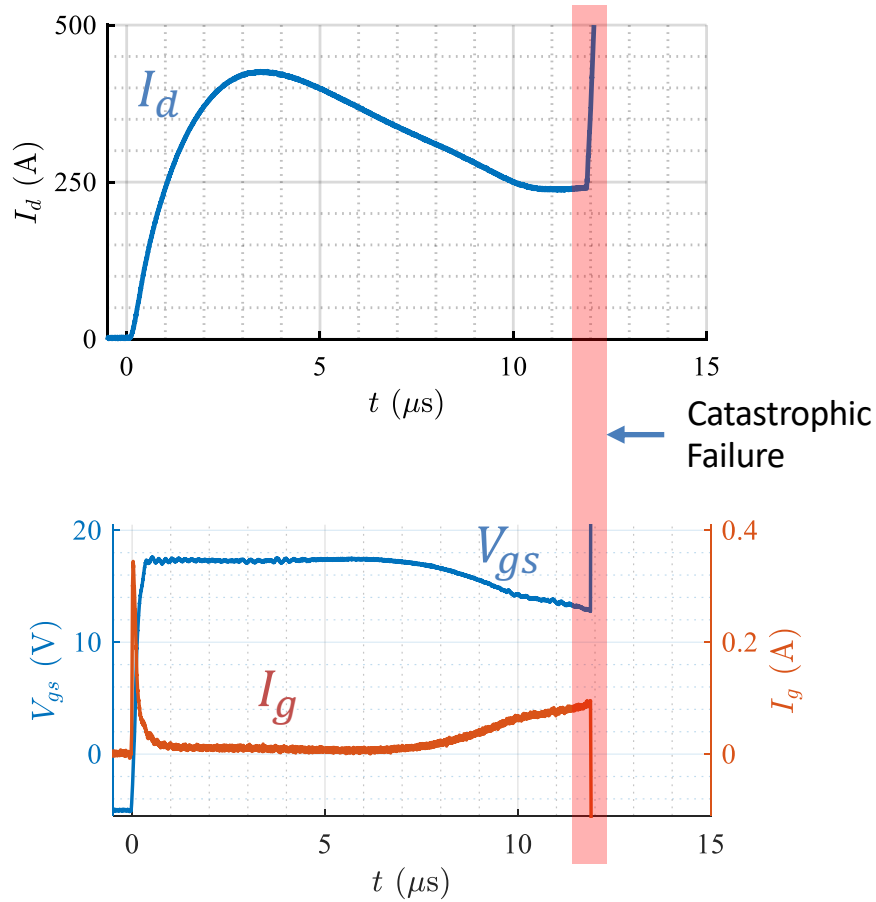
Short-circuit measurement

- Dies under study: C2M-1200-0025b
  - SiC MOSFET from Cree
  - 1200 V – 98 A – 25 mΩ
- Test conditions:
  - Drain-source voltage: 600 V
  - Driving voltage: -5/+18 V
  - Gate resistance: 51 Ω



Measured waveforms:

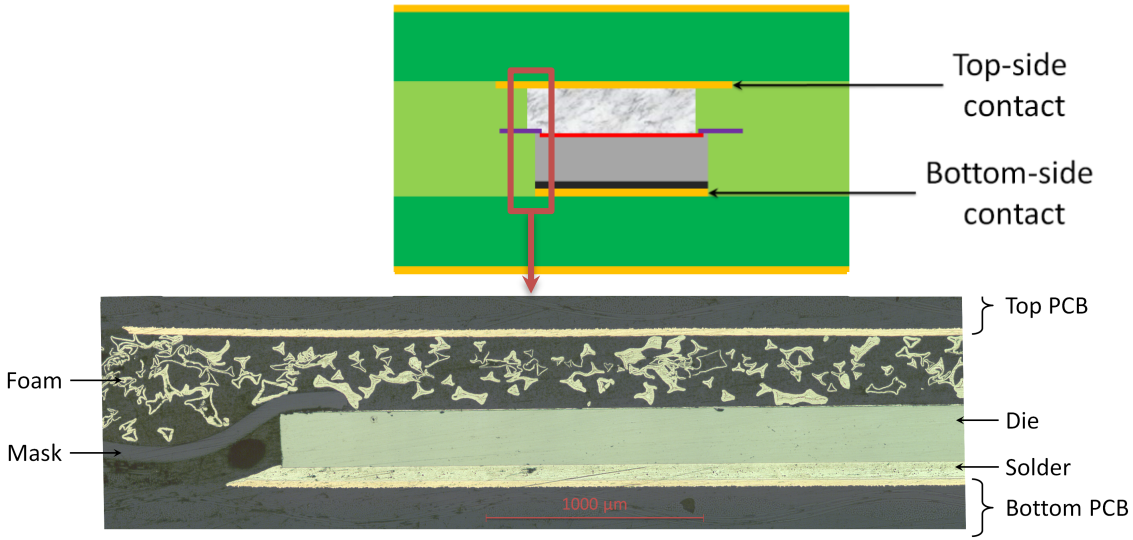


Context : die PCB-embedding techniques

Standard process:

- Quite costly
- Require dies with a specific top-side layer
- Good electrical performances

Proposed process:



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