Stacked DBC Cavitied Substrate for a 15-kV Half-bridge Power Module

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Outline

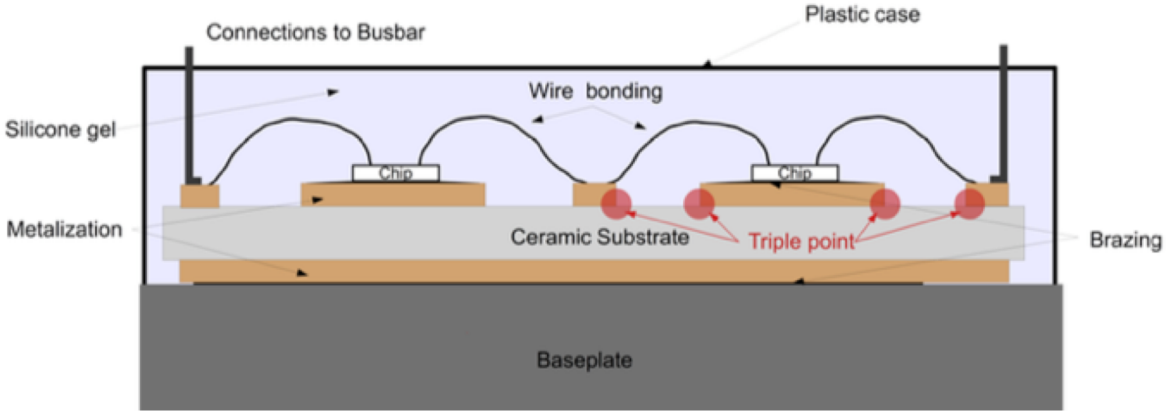
- Motivation
- High Voltage Substrate Design Considerations
- Literature Review: High Voltage Substrate Design
- Proposed Substrate Design
  - Parametric E-field Map
  - Parametric Thermal and Stress Map
  - PCM Integration
  - Stacking Procedure
- Conclusion and Future Work

Motivation

- **Medium Voltage Applications:**
  - High voltage circuit breakers
  - Solid-state transformers
  - Power conversion for shipboards and railroads
- **Simplification of the Systems:**
  - LV WBG devices: Multi-level topologies required
  - HV (≥10 kV) SiC devices: Simpler topologies
- **Packaging of HV SiC Devices:**
  - High power-density

HV Substrate Design Considerations

- **High voltage isolation**
  - Alumina & AlN DBC/DBA
    - DC: 20 kV/mm
    - AC: 16 kV/mm
- **Electric field (E-field) mitigation**
  - Triple points
  - Partial-discharge control
- **Low parasitic capacitance**
  - Low conducted EMI emissions
- **High thermal conductivity**
- **Low parasitic inductances (power-loop**
  - High switching speeds SiC devices
  - Ensure low voltage stress



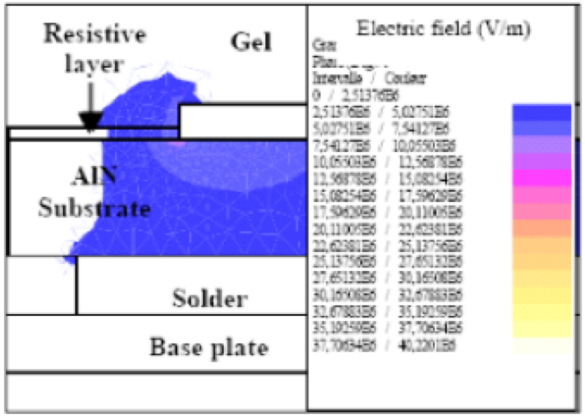
Cross-section of a typical power module

H. Hourdequin, L. Laudebat, M. L. Locatelli and P. Bidan, "Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation," 2016 IEEE International Conference on Dielectrics (ICD), Montpellier, 2016, pp. 999-1002.

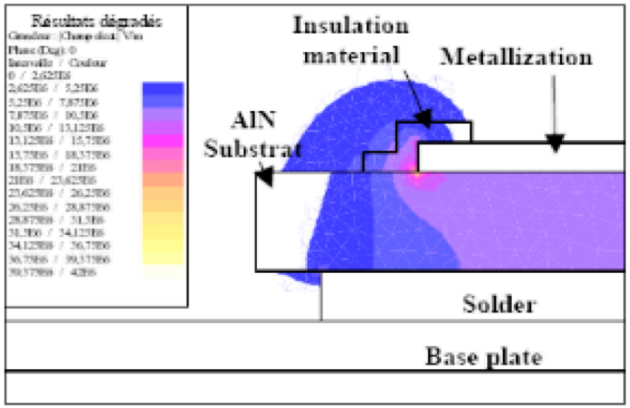
E-field Mitigation (1/2)

➢ Change E-field distribution

- Linear Resistive Material (conductivity not dependent on field)
- Non-linear Resistive Material (ZnO-Polyimide)
- Insulation/Passivation Material (PAI/ BCB)
- Refractive Grading Materials
  - Polymeric matrix filled with high permittivity particles ($BaTiO_3$)



Resistive Material



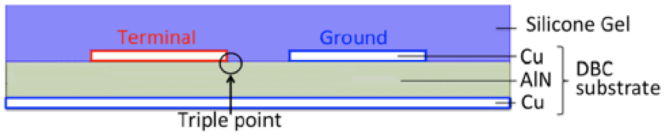
Insulation Material

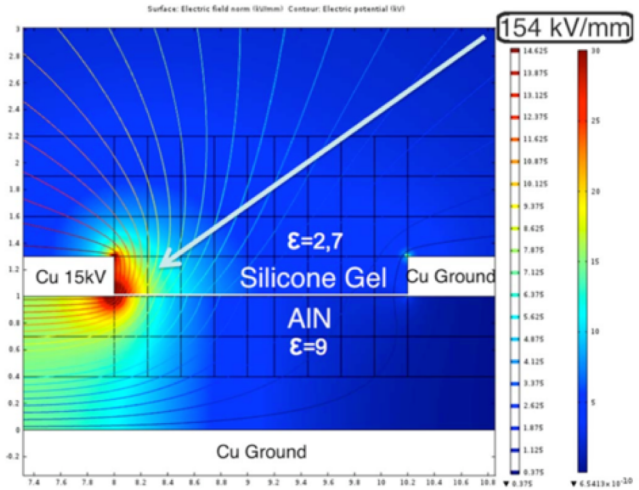
Passivation Material

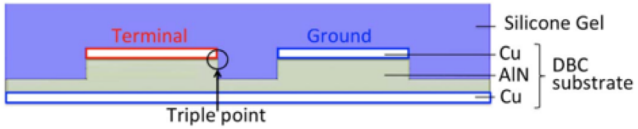
G. Mitic, T. Licht, and G. Lefranc, "IGBT module technology with high partial discharge resistance," in Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248), 2001, pp. 1899-1904 vol.3.
D. Frey, J. L. Schanen, J. L. Auge, and O. Lesaint, "Electric field investigation in high voltage power modules using finite element simulations and partial discharge measurements," in 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003., 2003, pp. 1000-1005 vol.2.
L. Donzel and J. Schuderer, "Nonlinear resistive electric field control for power electronic modules," IEEE Transactions on Dielectrics and Electrical Insulation, vol. 19, pp. 955-959, 2012.
U. Waltrich, C. F. Bayer, M. Reger, A. Meyer, X. Tang, and A. Schletz, "Enhancement of the partial discharge inception voltage of ceramic substrates for power modules by trench coating," in2016 International Conference on Electronics Packaging (ICEP), 2016, pp. 536-541.
J. Zhou, S. Ang, A. Mantooth, and J. C. Balda, "A nano-composite polyamide imide passivation for 10 kV power electronics modules," in2012 IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 4262-4266.

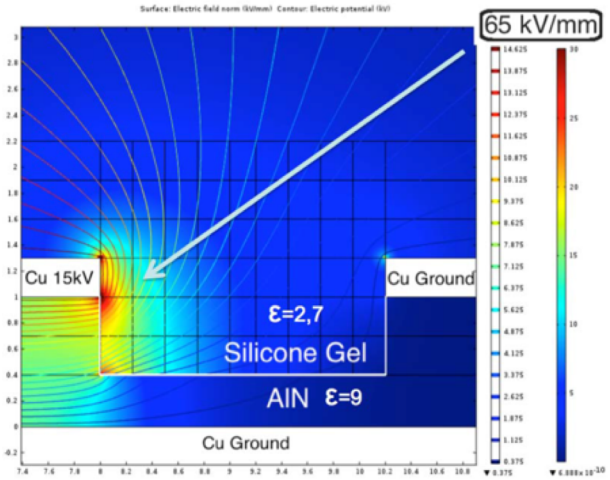
E-field Mitigation (2/2)

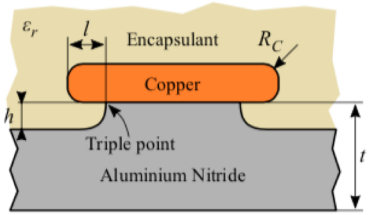
➢ Modify substrate structure and edge

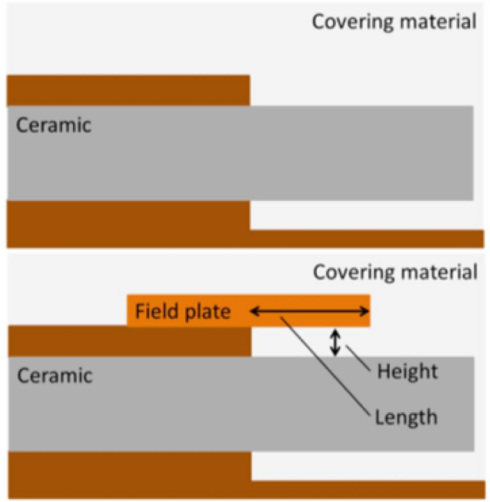




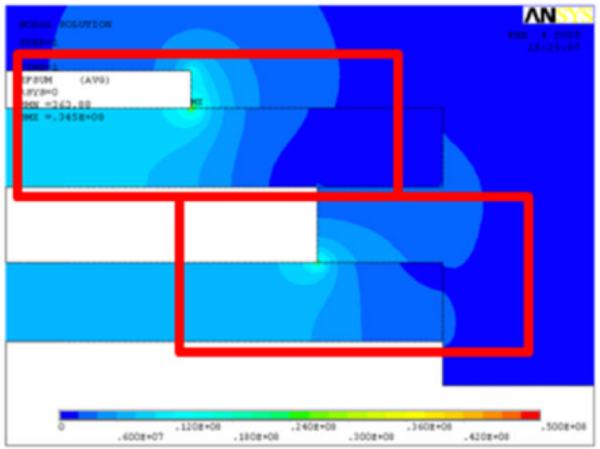








Field plate



Conventional **MESA structures/ Protruding ceramics** **Stacked substrates**

C. F. Bayer, U. Waltrich, A. Soueidan, E. Baer, and A. Schletz, "Stacking of Insulating Substrates and a Field Plate to Increase the PDIV for High Voltage Power Modules," in2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016, pp. 1172-1178.
H. Hourdequin, L. Laudebat, M. L. Locatelli and P. Bidan, "Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation," 2016 IEEE International Conference on Dielectrics (ICD), Montpellier, 2016, pp. 999-1002.
H. Reynes, C. Buttay, and H. Morel, "Protruding ceramic substrates for high voltage packaging of wide bandgap semiconductors," in2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2017, pp. 404-410.
O. Hohlfeld, R. Bayerer, T. Hunger, and H. Hartung, "Stacked substrates for high voltage applications," in2012 7th International Conference on Integrated Power Electronics Systems (CIPS), 2012, pp. 1-4.

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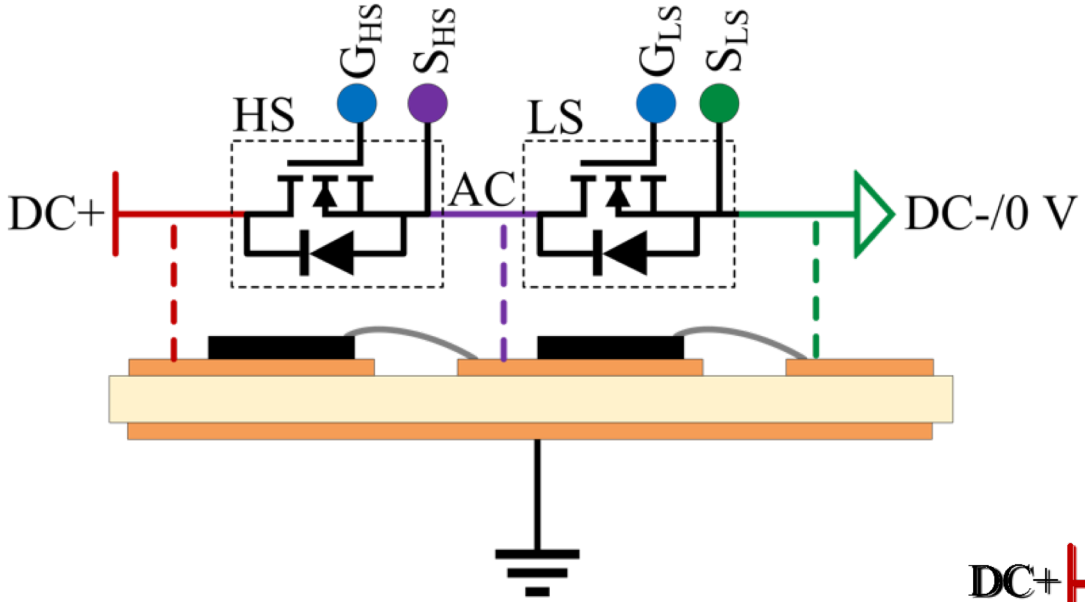
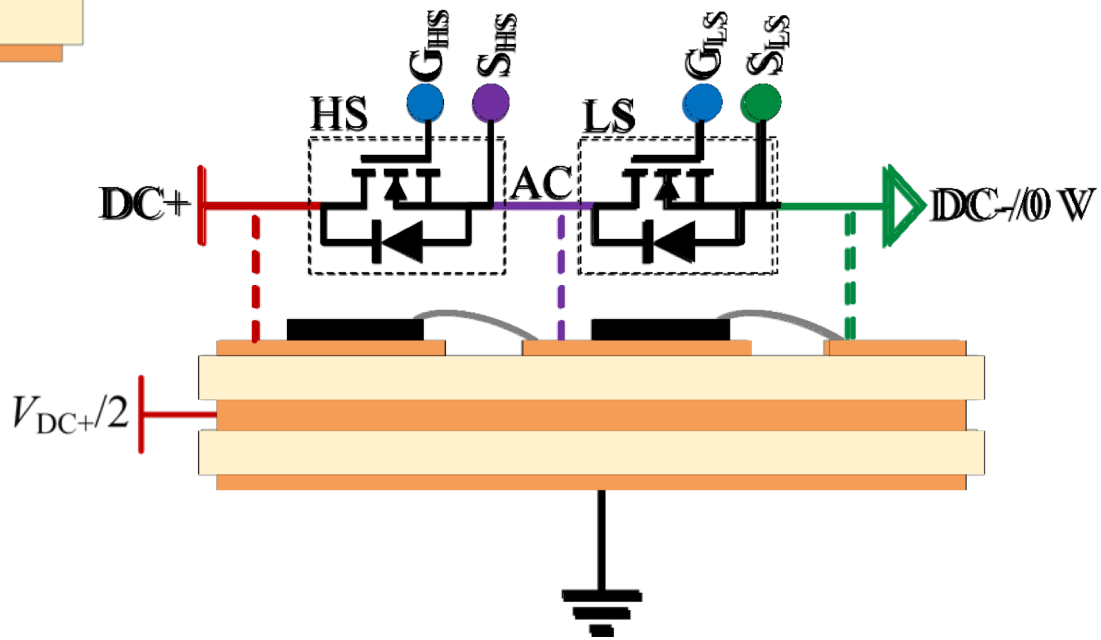
Stacked Substrate



Cross-section of a conventional DBC substrate for LV-HB power module



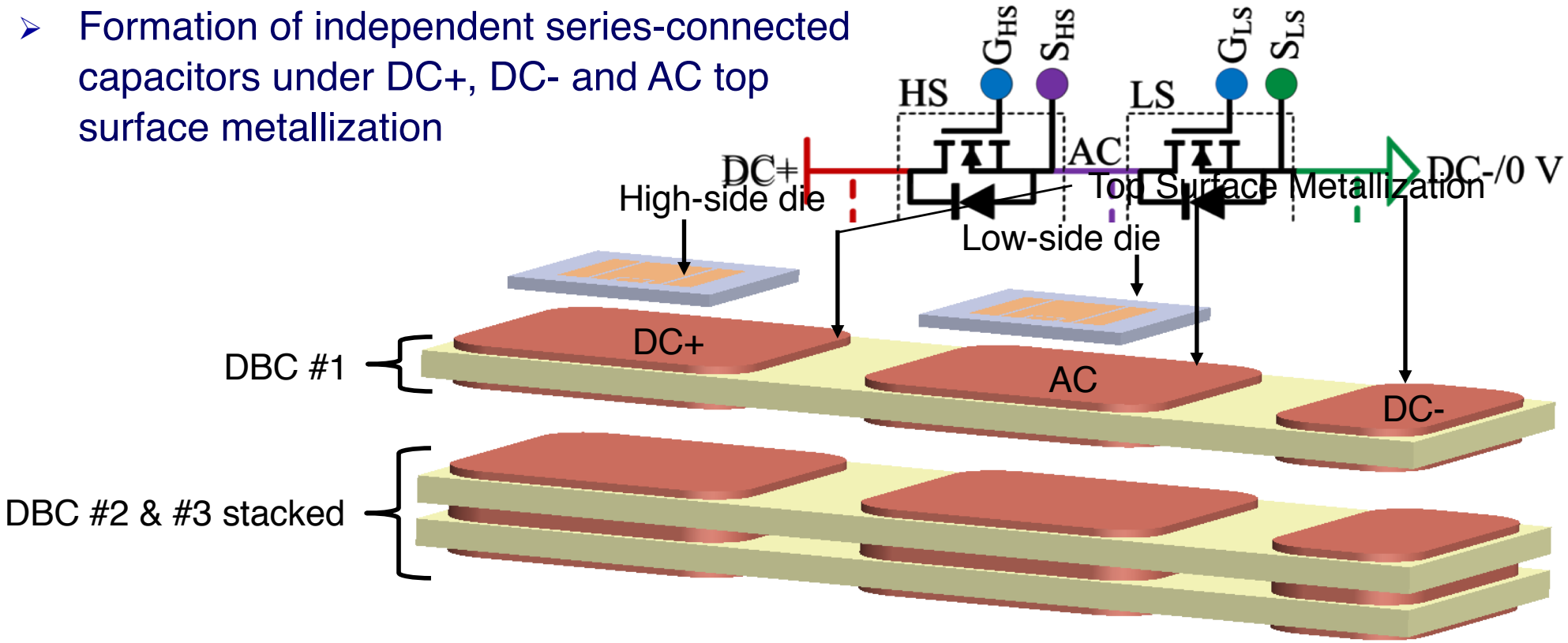
Cross-section of a stacked DBC substrate for HV-HB power module

O. Hohlfeld, R. Bayerer, T. Hunger, and H. Hartung, "Stacked substrates for high voltage applications," in 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), 2012, pp. 1-4.

C. DiMarino, B. Mouawad, K. Li, Y. Xu, M. Johnson, D. Boroyevich, et al., "A Wire-bond-less 10 kV SiC MOSFET Power Module with Reduced Common-mode Noise and Electric Field," in PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2018, pp. 1-7.

Proposed Stacked DBCs Cavitied Substrate

- Replicate the top surface metallization pattern on each interlayer and the bottom surface metallization
- Formation of independent series-connected capacitors under DC+, DC- and AC top surface metallization

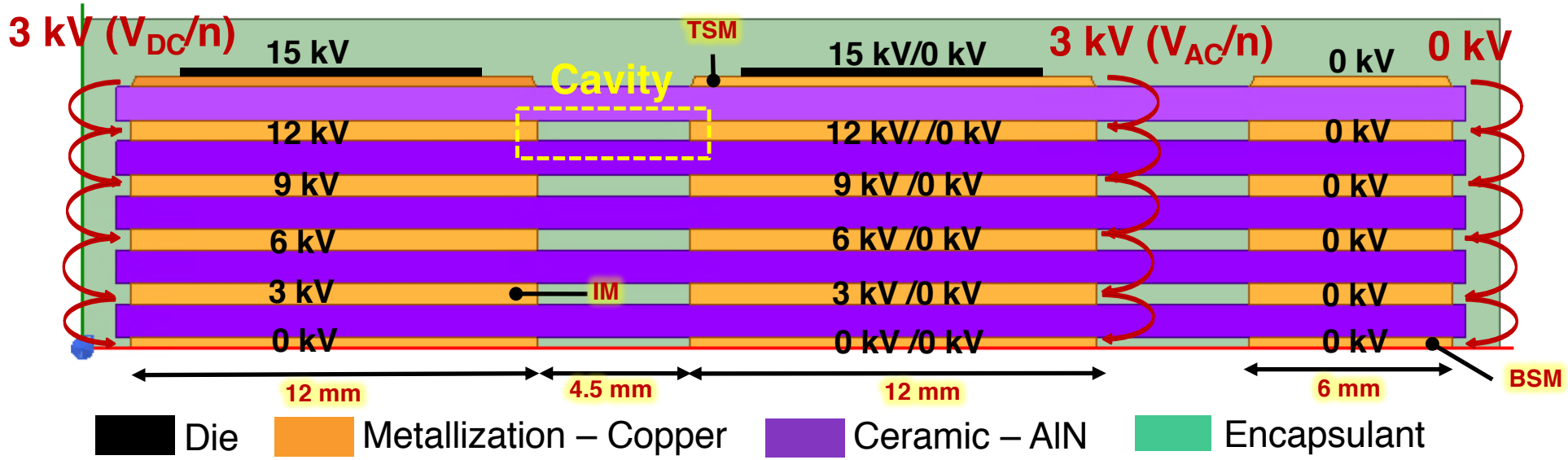


Exploded view of the proposed stacking of DBCs

Cross-section of the proposed substrate

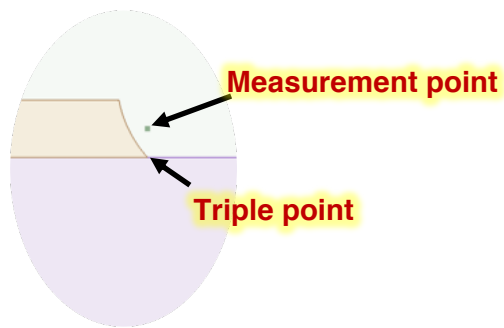
For $n = 5$, 80% reduction in the common-mode capacitance

E-field Parametric Map: 2D Model



Stacked DBC cavitied substrate with n = 5 ceramic layers

		No. of ceramic layers				
		1	2	3	4	5
Total ceramic thickness (mm)	1	✓	✓	✓	✓	✓
	2		✓	✓	✓	✓
	3			✓	✓	✓
	4				✓	✓
	5					✓



Mesh Independent Measurement

C. F. Bayer, E. Baer, U. Waltrich, D. Malipaard, and A. Schletz, "Simulation of the electric field strength in the vicinity of metallization edges on dielectric substrates," IEEE Transactions on Dielectrics and Electrical Insulation, vol. 22, pp. 257-265, 2015.

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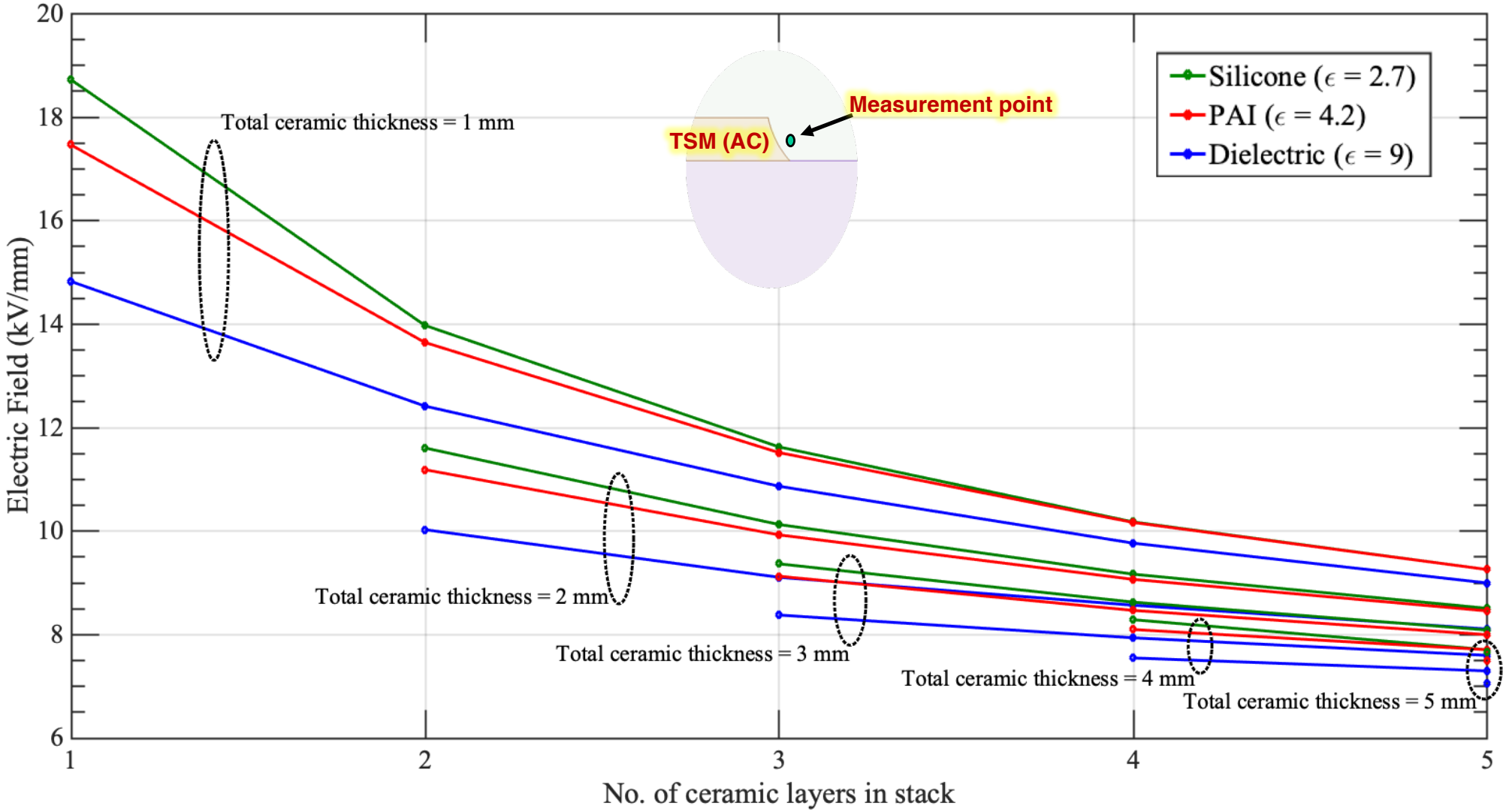
E-field Parametric Map



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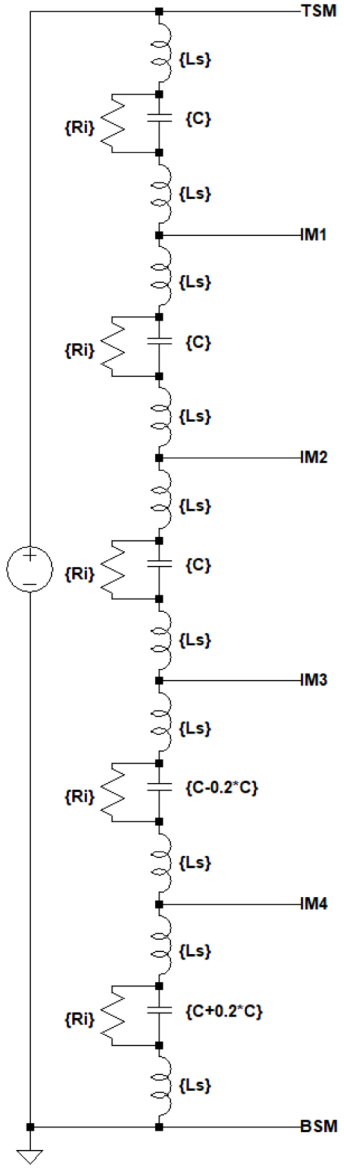
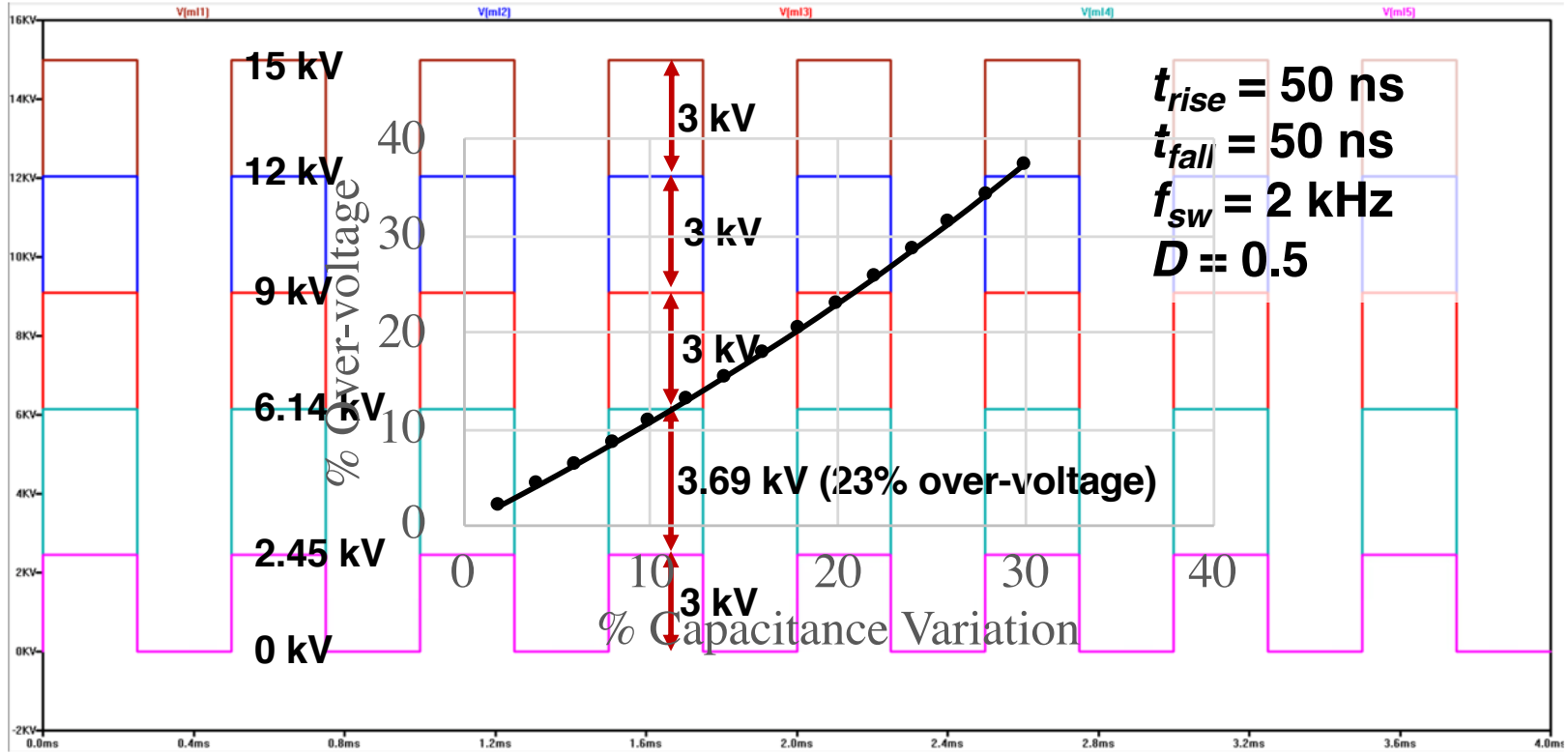
Voltage Distribution in DBC Stack





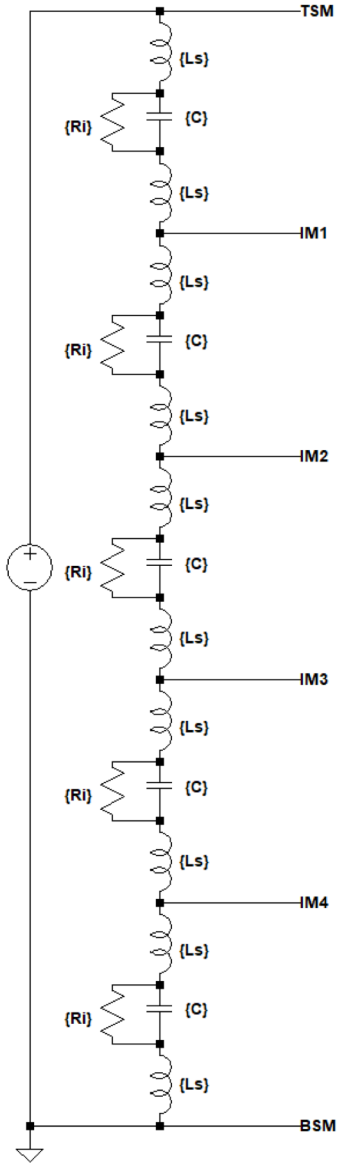
Trapezoidal waveform on the AC pad

-20% & +20% capacitance on C_4 and C_5

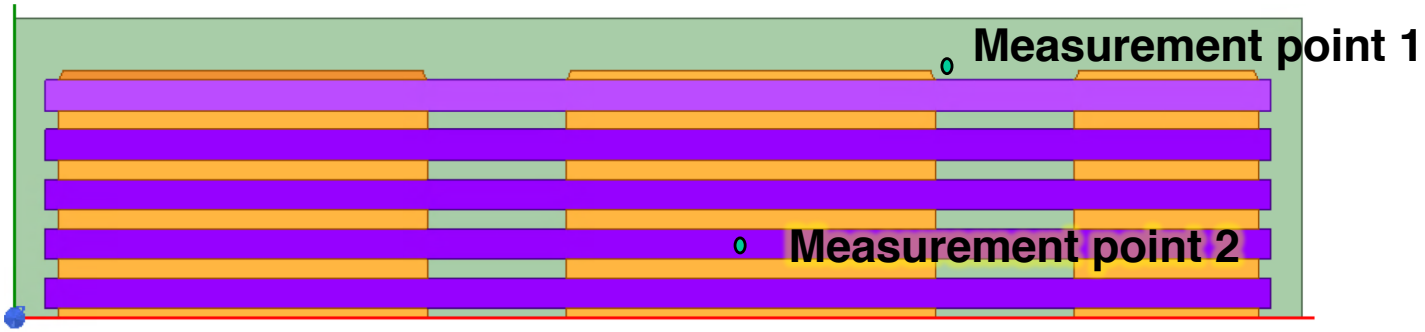
L_s = 50 pH
C = 149.74 pF
R_i = 905.3 GΩ

Parasitic Network

Voltage Distribution in DBC Stack



Parasitic Network



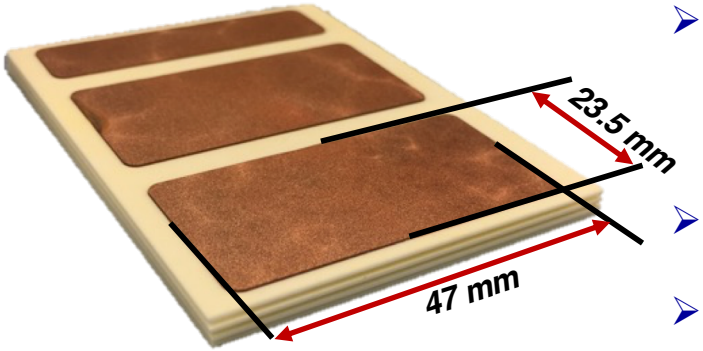
	E-field @ Measurement Point 1 (kV/mm)	E-field @ Measurement Point 2 (kV/mm)
Perfect Voltage Distribution	7.368	3
Voltage distribution for ±20% case	7.368	3.688

-20% & +20% capacitance on C_4 and C_5

L_s = 50 pH
C = 149.74 pF
R_i = 905.3 GΩ

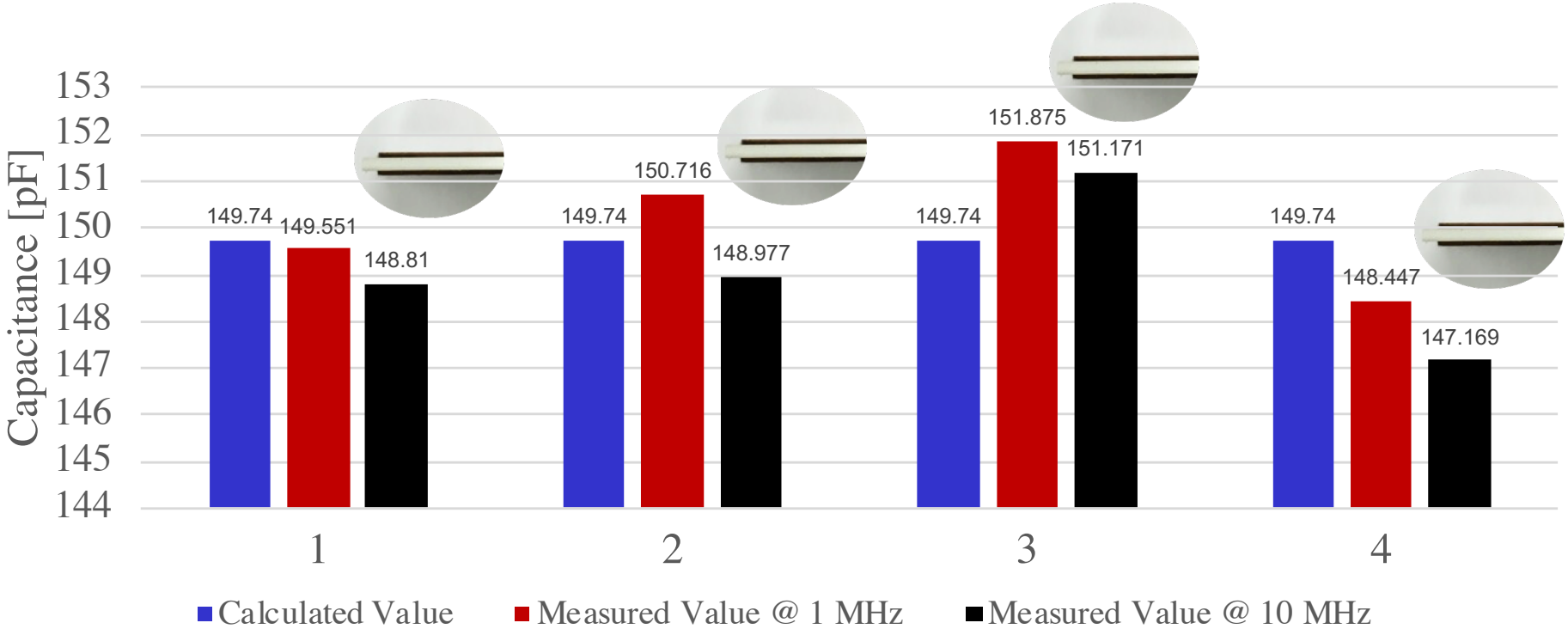
- **The e-field near the TSM triple points is unaffected.**
- **Only the bulk e-field in the stressed ceramic will be affected.**

Capacitance Measurement: Single Layers



Stacked DBC Cavitied Substrate

- **4 patterned samples**
  - Singulated from a single DBC master card
  - 0.3 mm Cu/ 0.64 mm Al_2O_3/ 0.3 mm Cu
- **Measured using Keysight E5061B Network Analyzer**
- **< ±2% tolerance in the capacitance for single layer**
  - No voltage clamping is required
  - Avoid drilled vias: a complicated fabrication step
  - Avoid changes in e-field distribution



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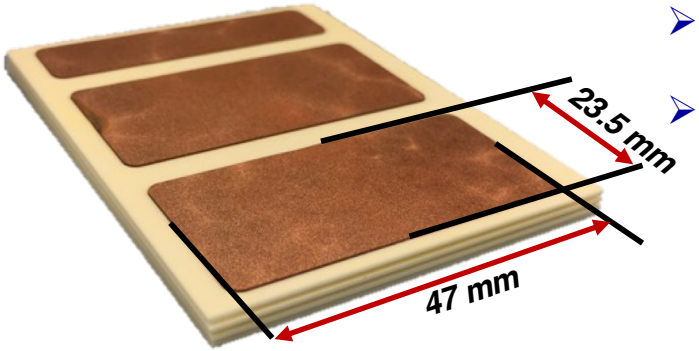
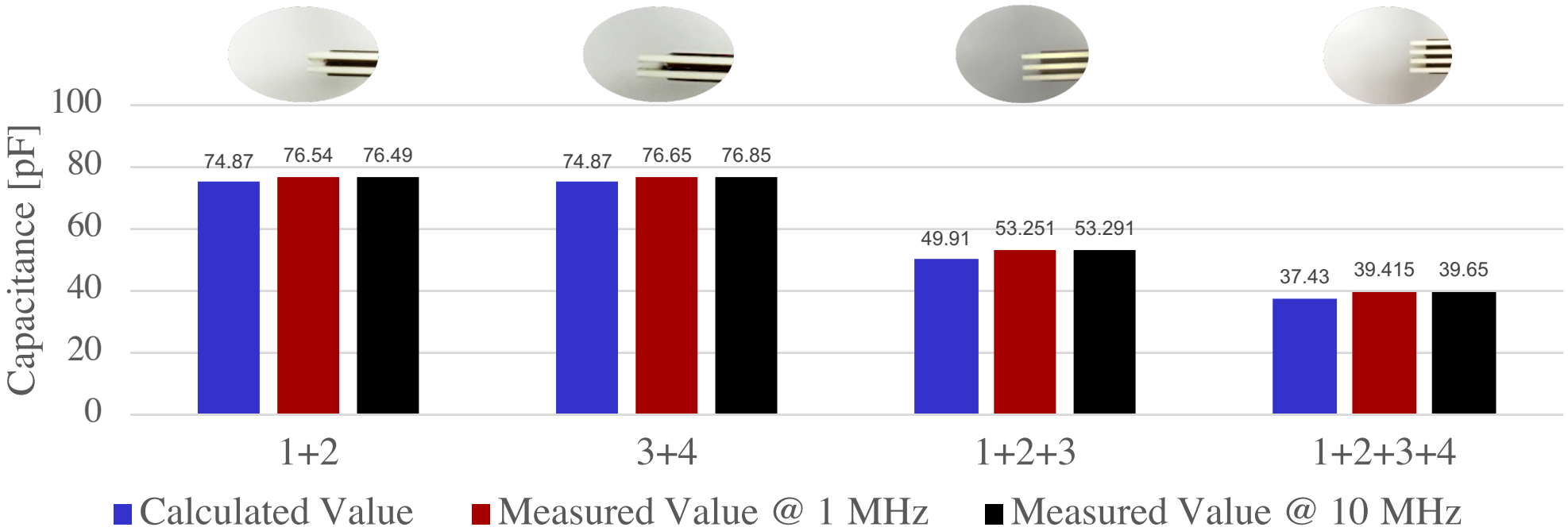
Capacitance Measurement: Stacks



- Stacked samples
- Measured using Keysight E5061B Network Analyzer

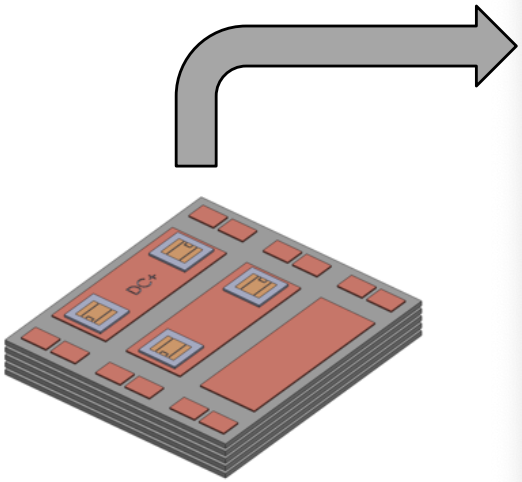
Stacked DBC Cavitied Substrate

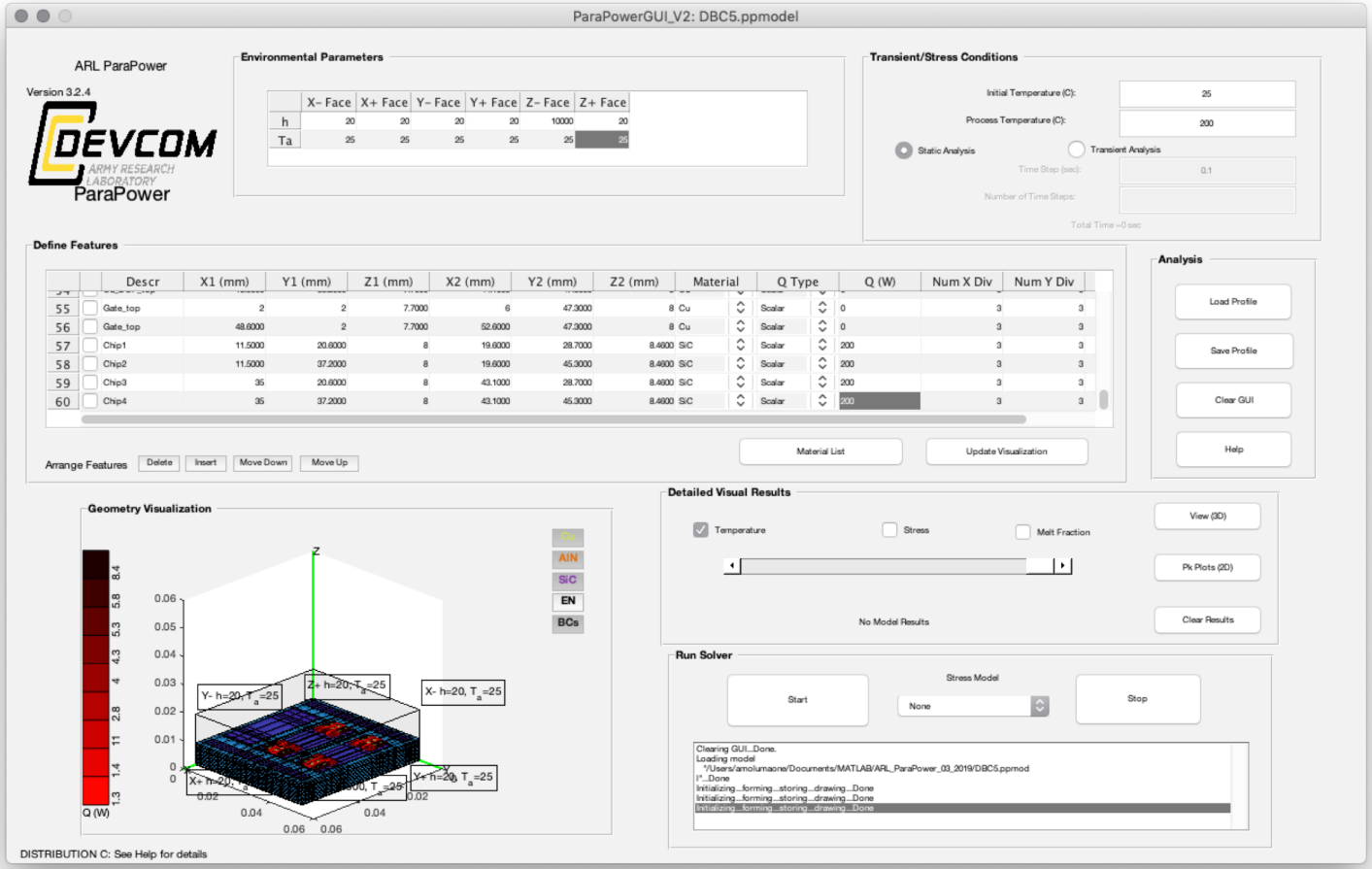


Thermal & Stress Map

➢ ARL ParaPower

- Co-design-Parametric analysis tool
- Fast run-times (>100x) for analyzing large multi-disciplinary parameter space
- Reasonable accuracy
- Compact 3D thermal resistance and stress network model





L. M. Boteler, S. M. Miner, and M. Hinojosa, "Co-Designed High Voltage Module," in 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2018, pp. 824-830.

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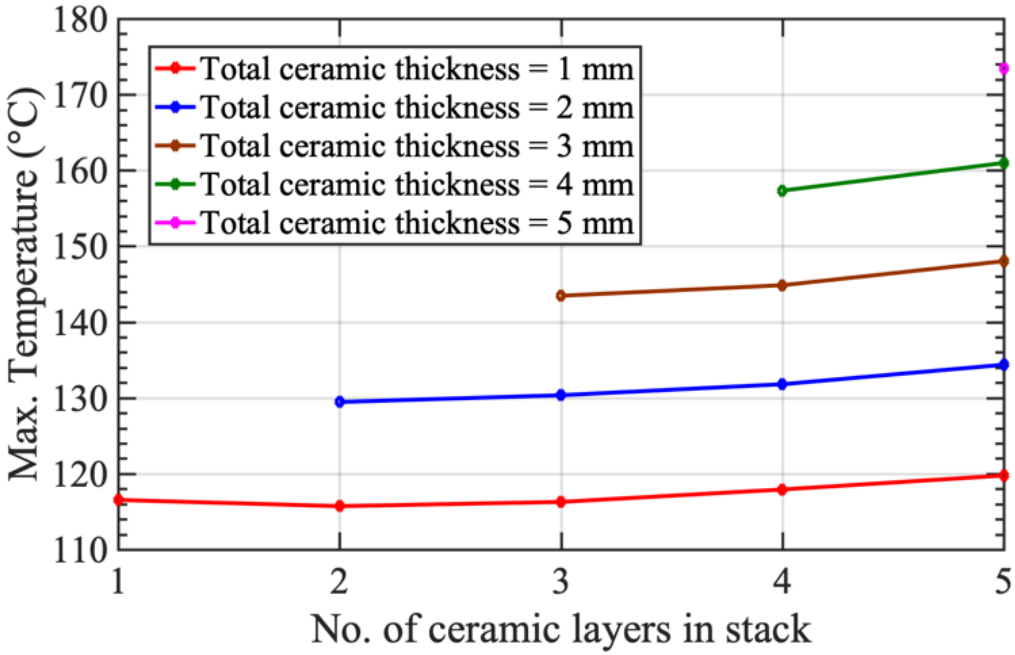
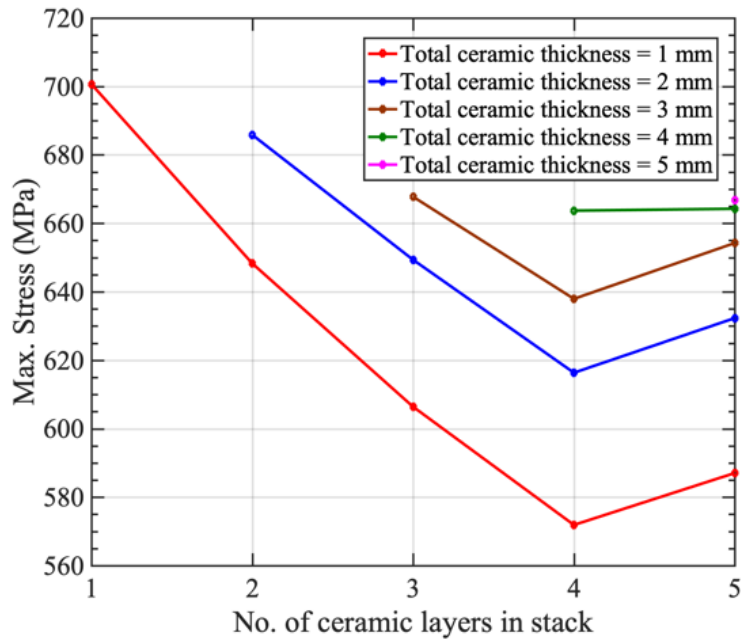
Thermal & Stress Map

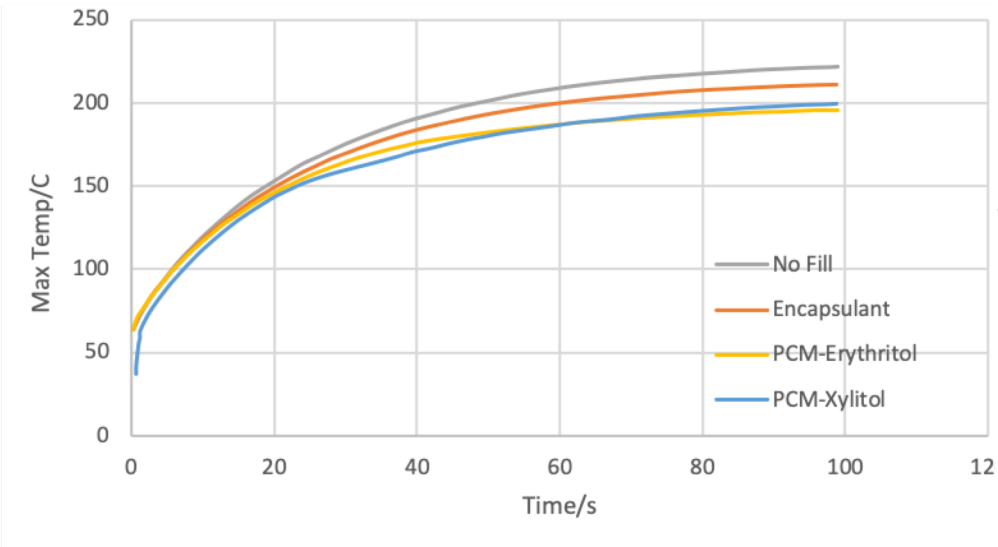




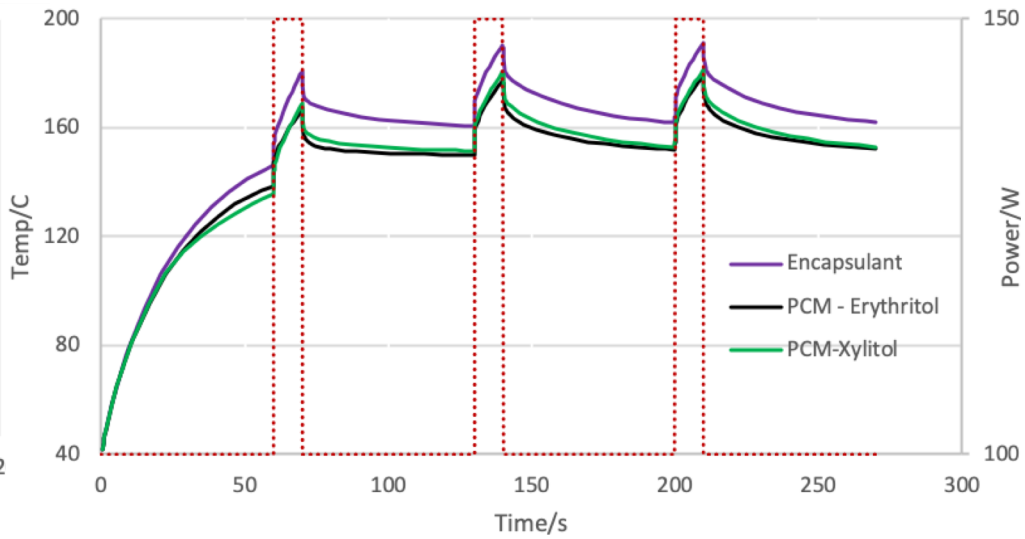
- **Environmental conditions/ Stress conditions:**
  - Process temperature: 200 °C
  - Initial node temperature: 20 °C
  - Power dissipation per die: 200 W
  - Convective heat coefficient: 10000 W/m^{2}K
- **Conclusions:**
  - Min T_j and E-field mitigation trade-offs

PCM Integration in Cavities

- **Phase-change material (PCM) integration in the cavities**
  - Mitigate transient loads by passive means
  - Sugar-alcohol based PCMs: Erythritol, Xylithol
  - Transient analysis and power cycling results

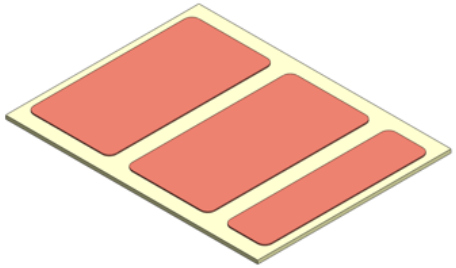


Transient analysis results



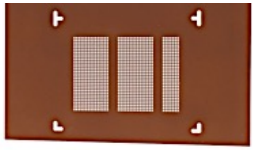
Power cycling results

Stack and Attach Procedure

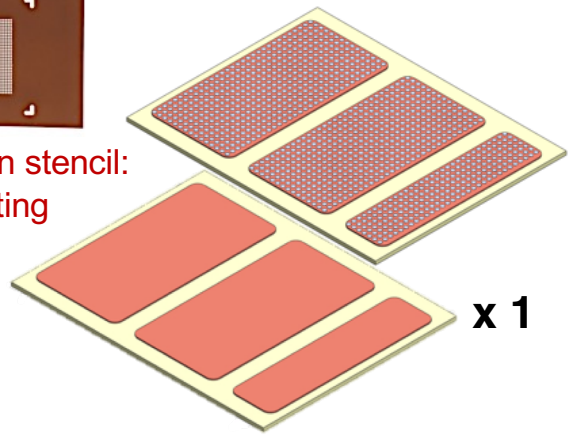


x 5

Double-sided patterned DBC layers



3-mil Kapton stencil:
screen-printing

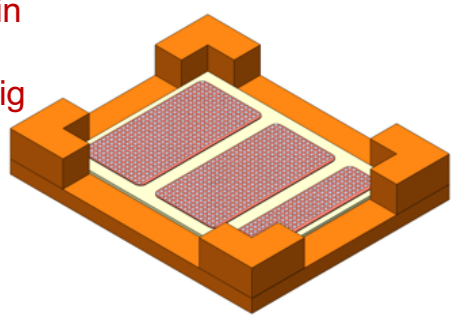


x 4

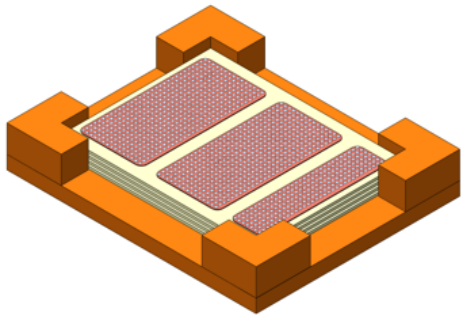
x 1

Screen-printed silver-epoxy on DBCs

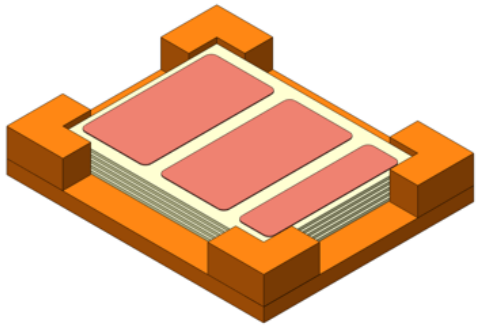
Liquid Resin
3D-printed
alignment jig



1 DBC in the alignment jig

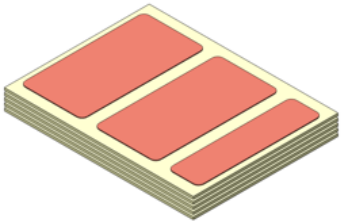


4 DBCs in the alignment jig



Full stack-up of DBCs in the alignment jig

Vacuum oven curing:
150 ℃/ 1 hour
200 ℃/ 1 hour



Final Stacked DBC substrate after epoxy curing

Conclusion and Future Work

- **Conclusions:**
  - More scalability with voltage to a stacked substrate solution
  - High voltage isolation
  - Reduction in PD due to E-field mitigation
  - Simple fabrication
  - E-field mitigation and thermal performance trade-offs
  - Cavities could be utilized for passive cooling with PCM integration

- **Future Work:**
  - DC and AC breakdown tests
  - PD inception and extinction voltage tests
  - Thermal resistance measurements
  - High-voltage breakdown strength nano-particle infused PCMs

Acknowledgement

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Thank You!

Questions?