

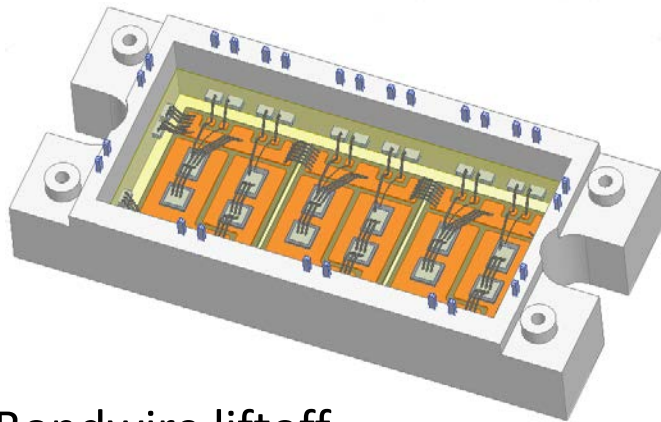
FEA-Based Thermal-Mechanical Optimization for DBC Based Power Modules

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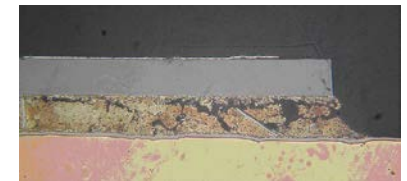
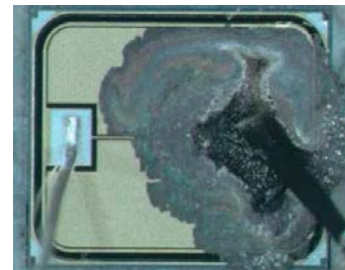
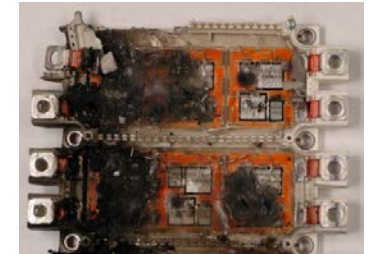
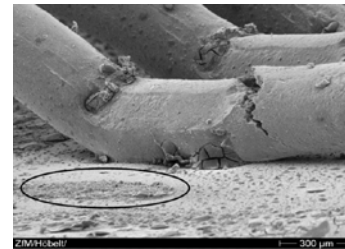
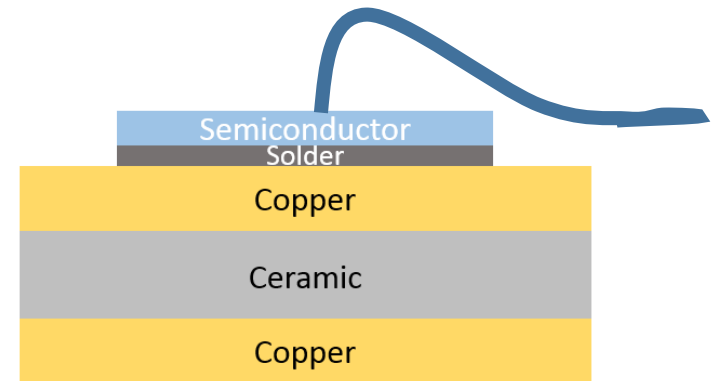
DBC failure modes



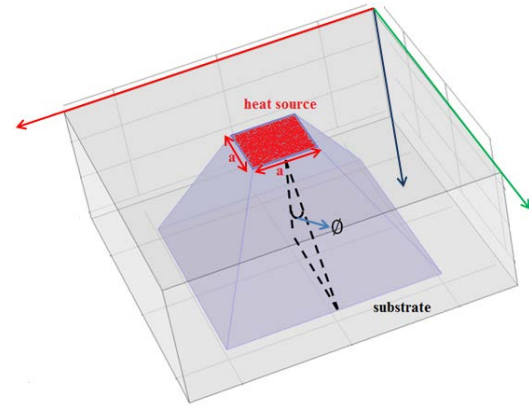
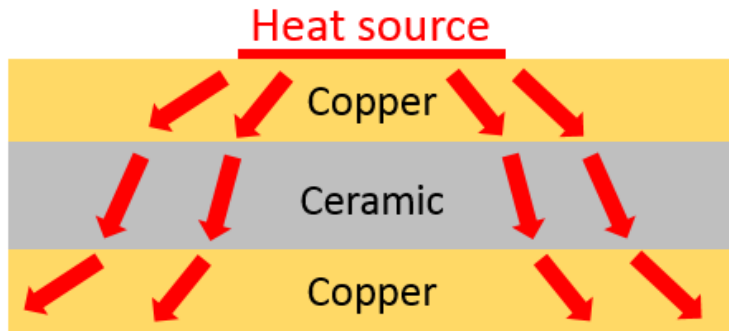
- Bondwire liftoff
- Solder degradation
- Cracks in silicon die
- Cracks in substrate
- Electro-migration in bonding wires

Failure rate:

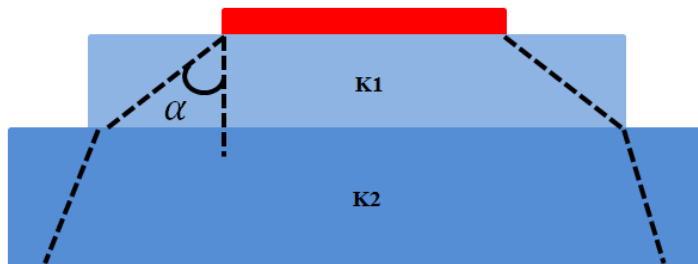
$$F = Ae^{-E_A/KT}$$



Thermal spreading



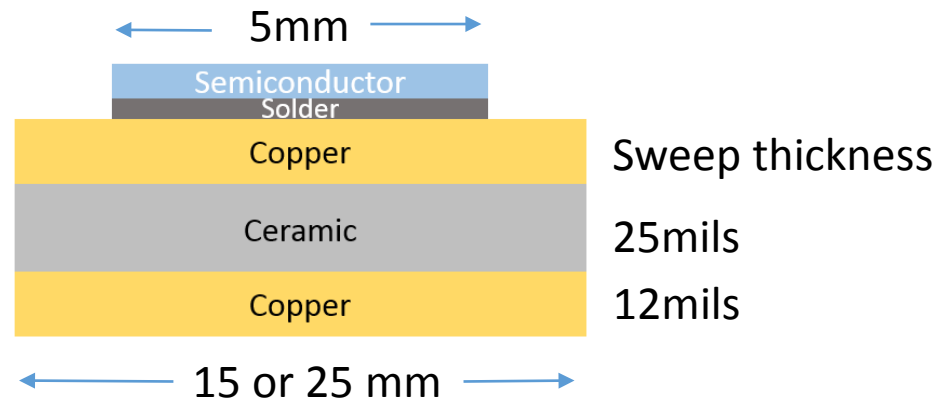
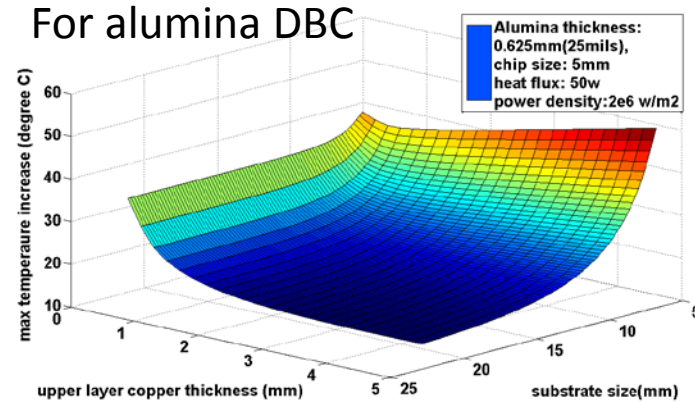
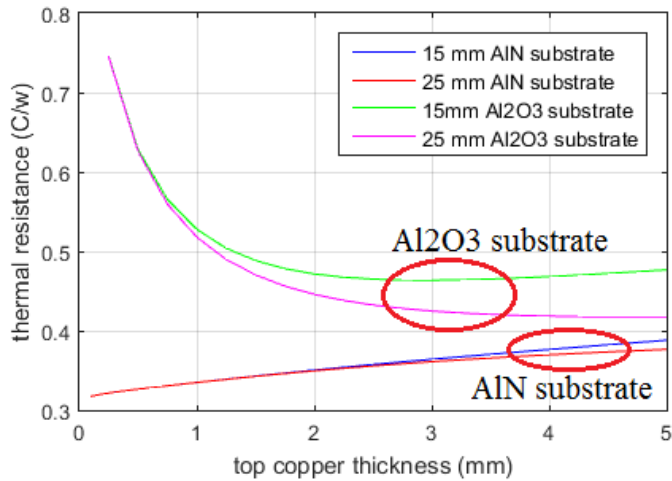
- $R_{th} = \frac{L}{kA}$
- $R_{th} = \int_0^{t_s} \frac{1}{k(a+2z \cdot \tan\theta)^2} dz = \frac{1}{2k \cdot \tan\theta} \left(\frac{1}{a} - \frac{1}{a+2t_s \tan\theta} \right)$



Ngon Binh Nguyen proposed that for multiple layered IGBT package structure, the spreading angle can be determined by:

$$\alpha = \arctan \frac{k_1}{k_2} \quad (0 < \alpha < 90^\circ)$$

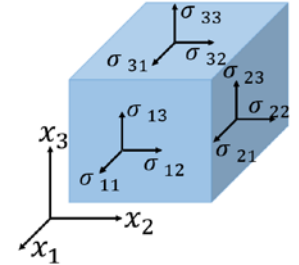
Thermal spreading



Thermal stress and material failure

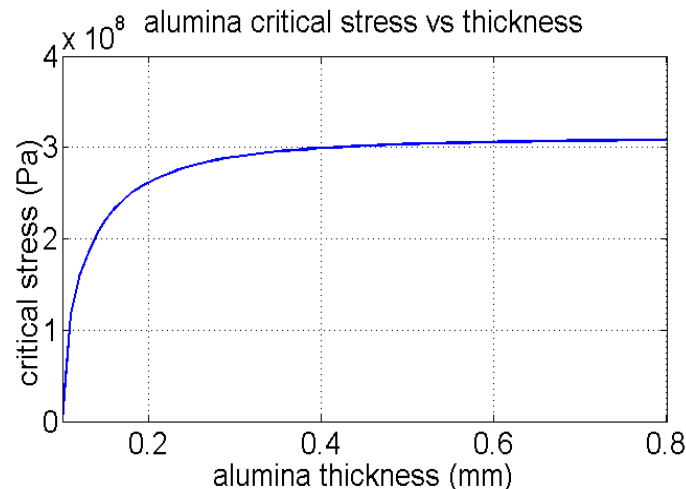
- For copper fracture, Von mises Stress criterion is used:

$$\frac{1}{\sqrt{2}} \sqrt{(\sigma_{11} - \sigma_{22})^2 + (\sigma_{22} - \sigma_{33})^2 + (\sigma_{33} - \sigma_{11})^2 + 6(\sigma_{12}^2 + \sigma_{23}^2 + \sigma_{31}^2)}$$

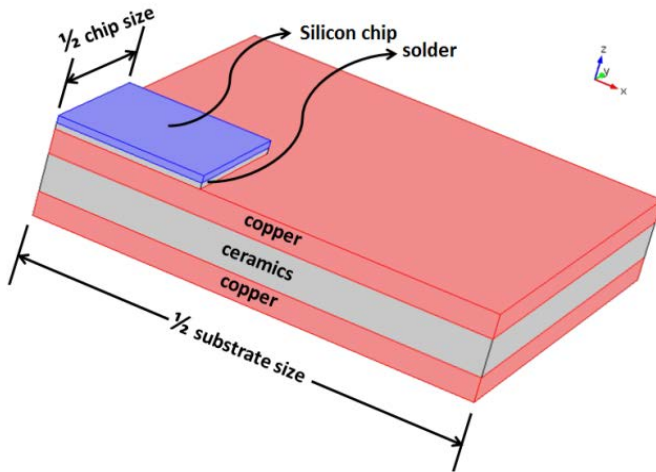


- For ceramic fracture, the plane strain fracture toughness

$$K_{IC} = Y\sigma\sqrt{\pi a} \quad \text{where} \quad Y\left(\frac{a}{W}\right) = \sqrt{\sec\left(\frac{\pi a}{W}\right)} \quad , a \text{ is half of internal crack size}$$



Optimization model definition



Variables	Lower Bound	Upper Bound	Initial Value
DBC Size	6	20	15
Top Cu	0.1	1	0.4
Al_2O_3	0.1	1.2	0.625
Bottom Cu	0.1	1	0.4

Material break:

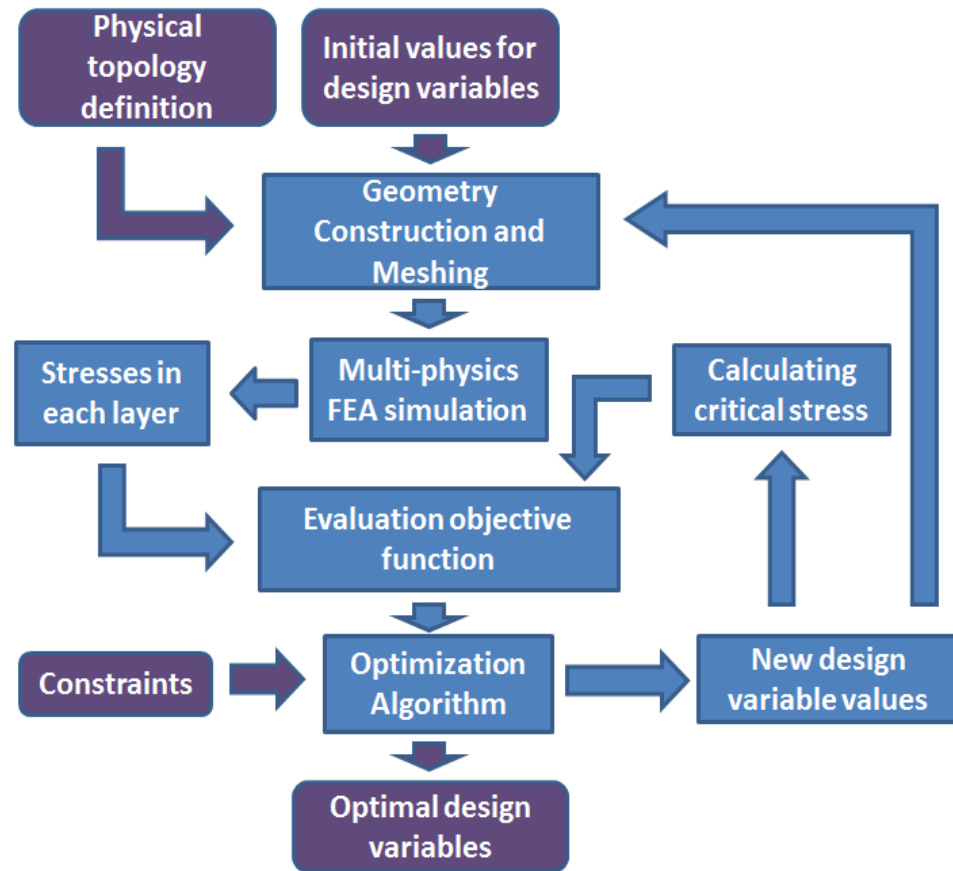
$$\left\{ \begin{array}{l} \sigma'_{Cu_max} > \sigma_{Cu_yield} \\ \sigma'_{ceramic_max} > \sigma_{ceramic_critical} \\ \sigma'_{semiconductor_max} > \sigma_{semiconductor_critical} \\ \sigma'_{solder_max} > \sigma_{solder_critical} \end{array} \right.$$

$$obj = \text{Max} \left(\begin{array}{l} \frac{\sigma'_{Cu_max_top}}{\sigma_{Cu_yield}} , \\ \frac{\sigma'_{ceramic_max}}{\sigma_{ceramic_critical}} , \\ \frac{\sigma'_{semiconductor_max}}{\sigma_{semiconductor_critical}} , \\ \frac{\sigma'_{solder_max}}{\sigma_{solder_critical}} \end{array} \right)$$

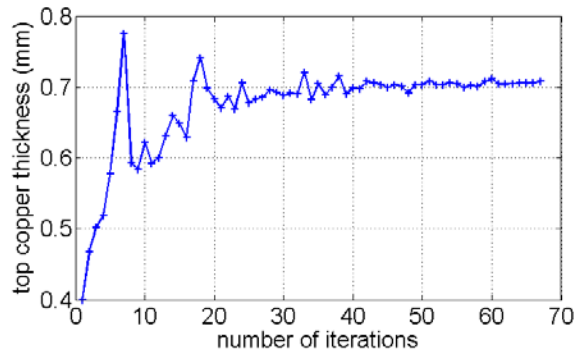
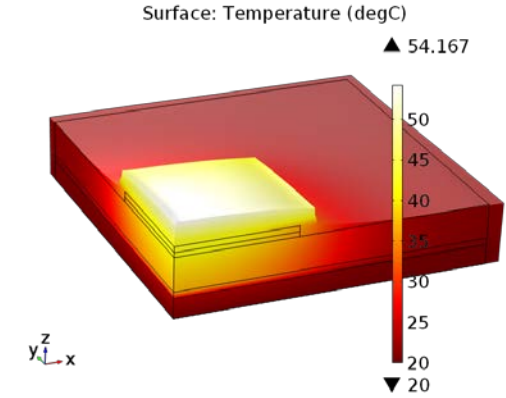
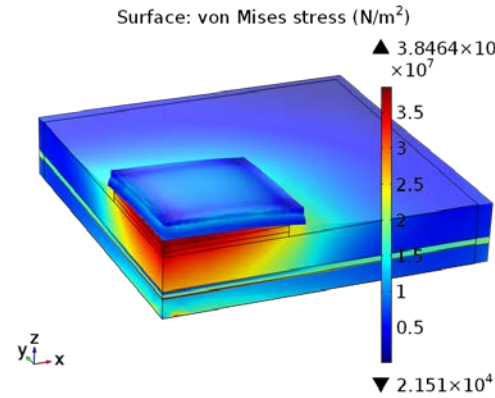
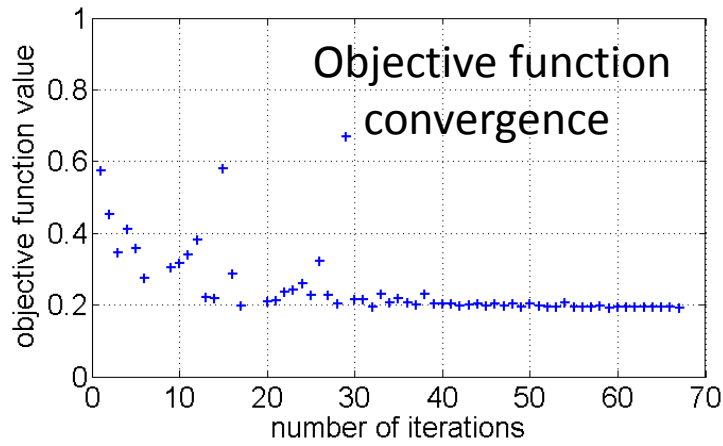
Optimization algorithm options

- Derivative-Free
 1. The bound optimization by Quadratic Approximation
 2. Nelder-Mead
 3. Coordinate search
 4. Monte Carlo method
- Gradient-Based
 1. SNOPT
 2. Levenberg-Marquardt solver
 3. Method of Moving Asymptotes (MMA)

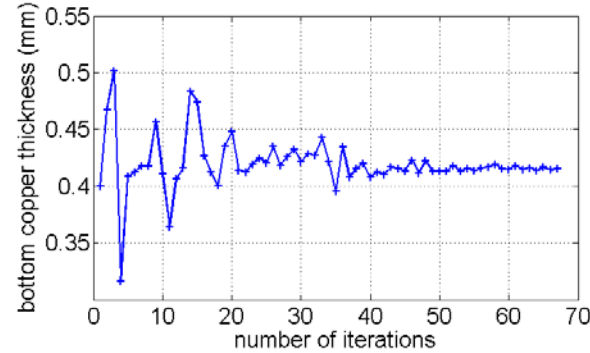
Optimization flow chart



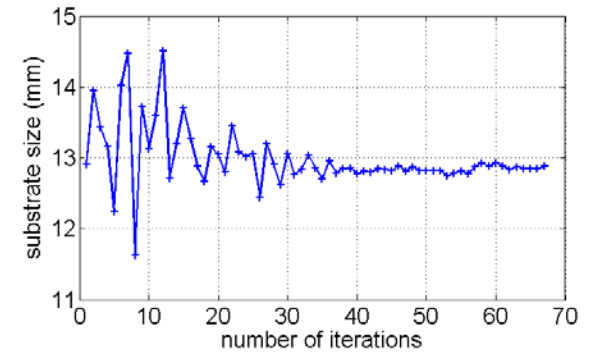
Results



Top copper thickness convergence



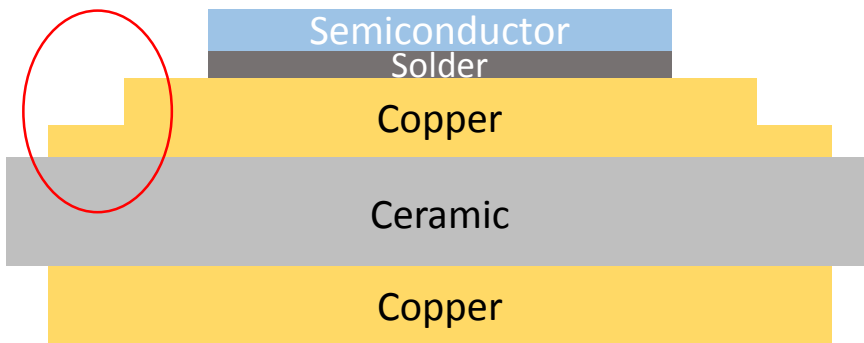
Bottom copper thickness convergence



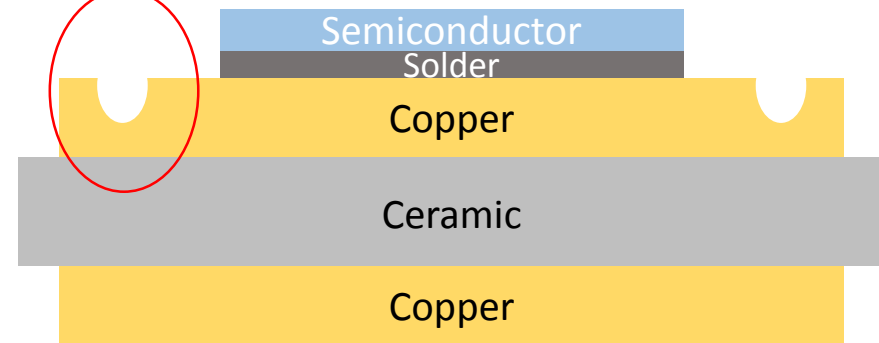
DBC size convergence

Future work

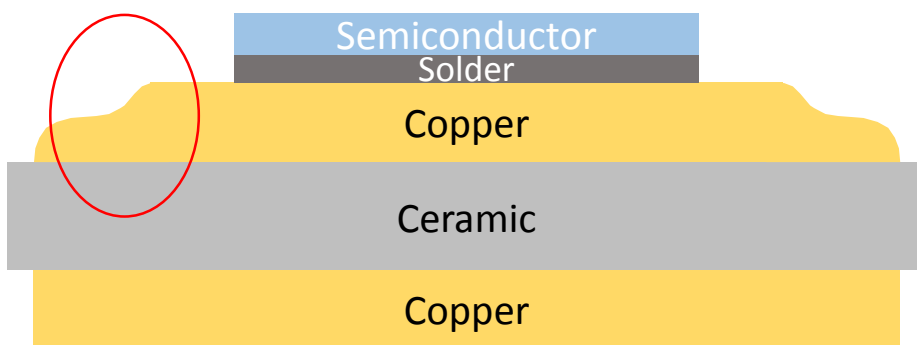
DBC with double edge



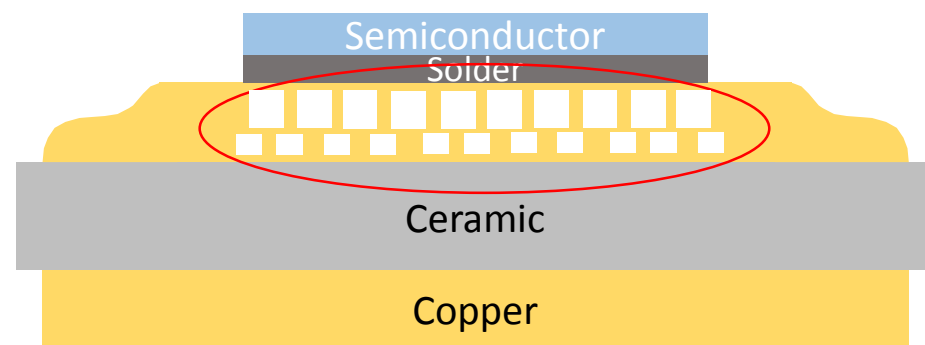
DBC with dimple array



DBC with curvature features



Power substrate with advanced internal features for stress management and heat transfer



References

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