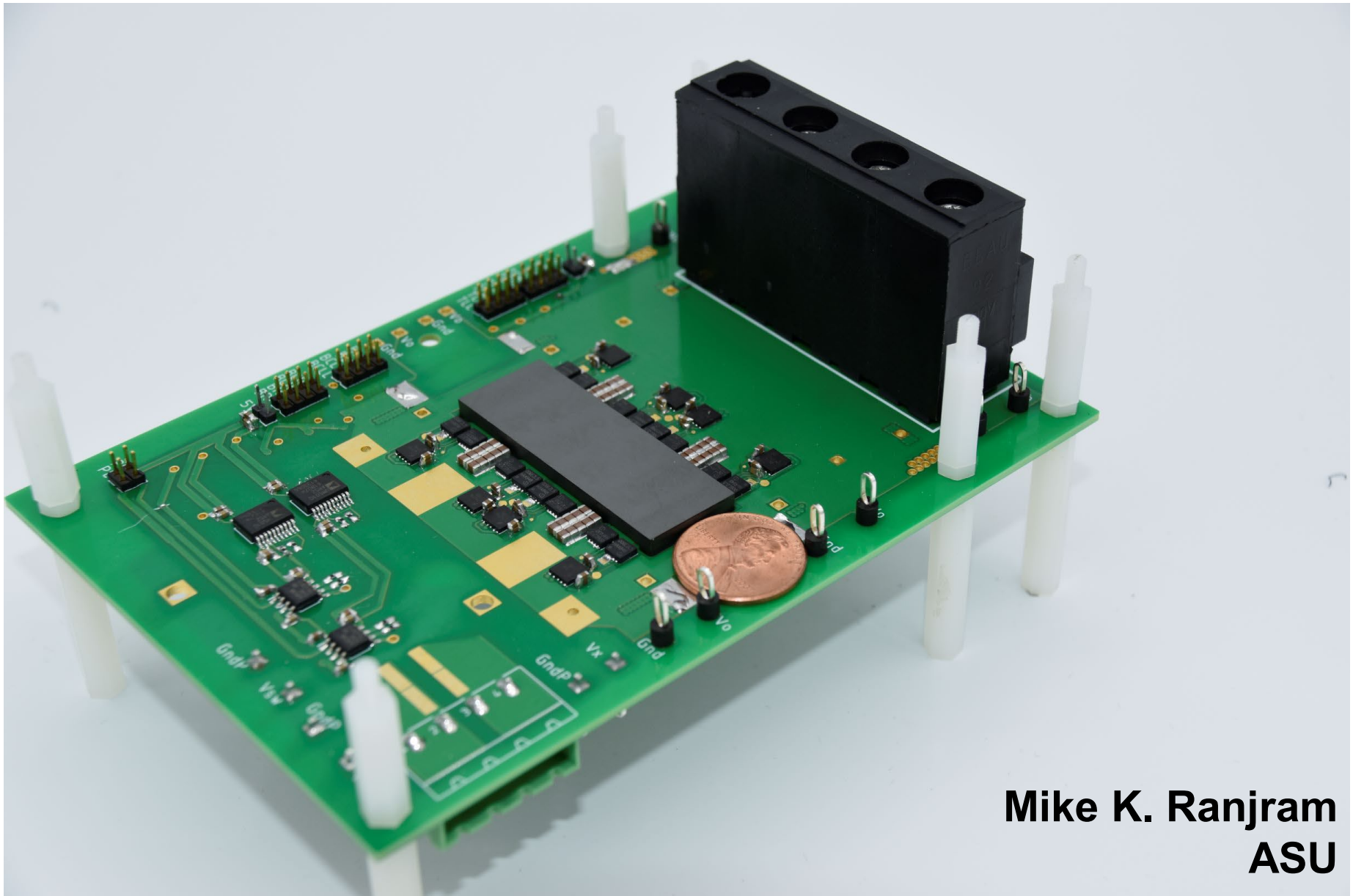
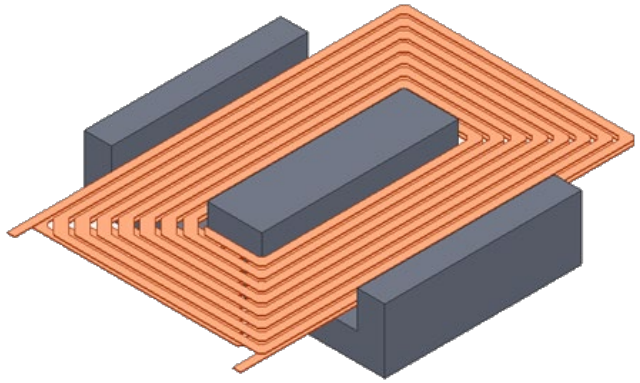
Coupled Electronic and Magnetic Systems for High Performance Power Electronics



Mike K. Ranjram
ASU

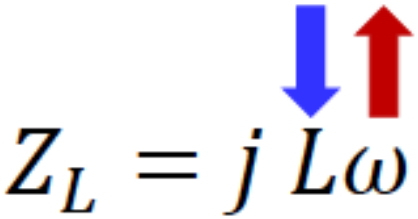
What are Our Approaches to Miniaturize Magnetics?

- Today's active areas of research (component-level)
  - High frequency switching (MHz+)
  - New magnetic materials
  - Leverage planar magnetics
  - Novel winding techniques



High Frequency Switching

- **Key to passives reduction:**
  - Decrease their numerical values
  - Decrease their energy storage requirements
- **Increasing f yields smaller L, C for same impedance**

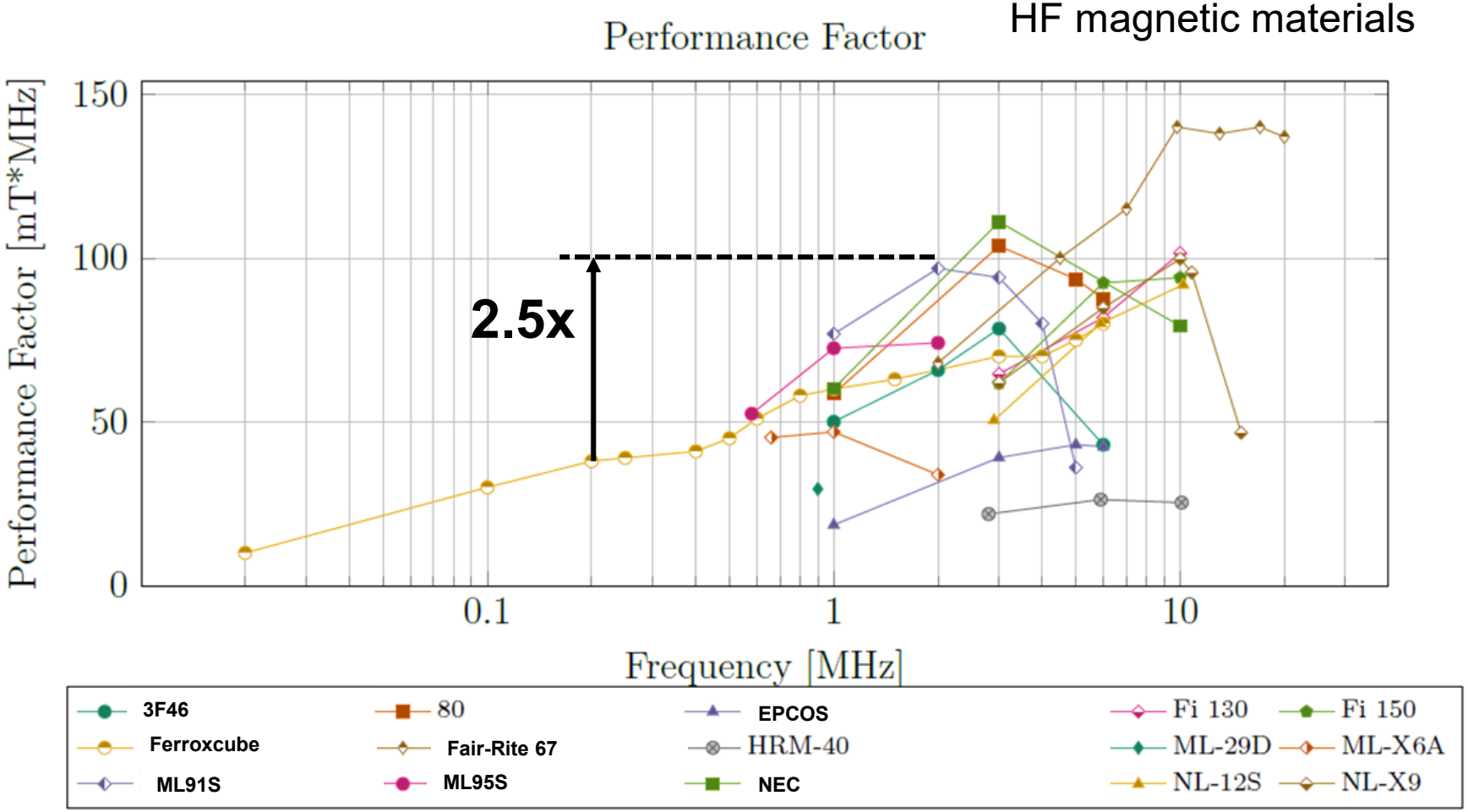


$$Z_L = j\,L\omega$$

High Performance Materials at High Frequencies

Low-permeability
HF magnetic materials

Power handling capability per unit volume

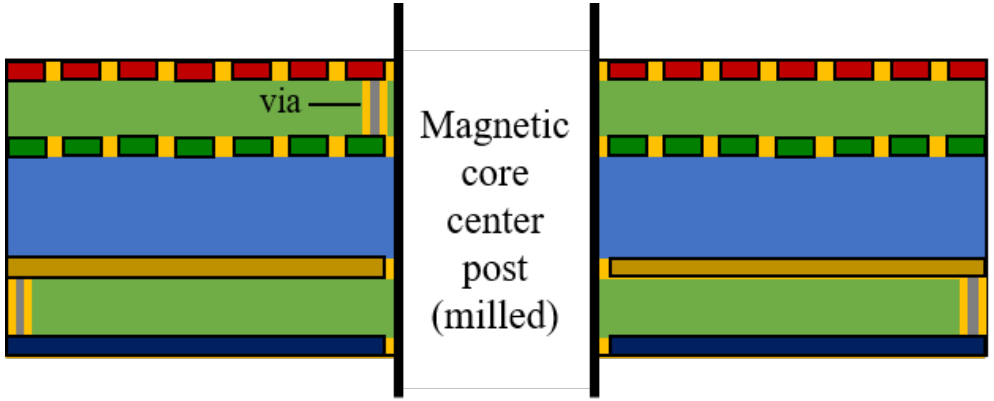


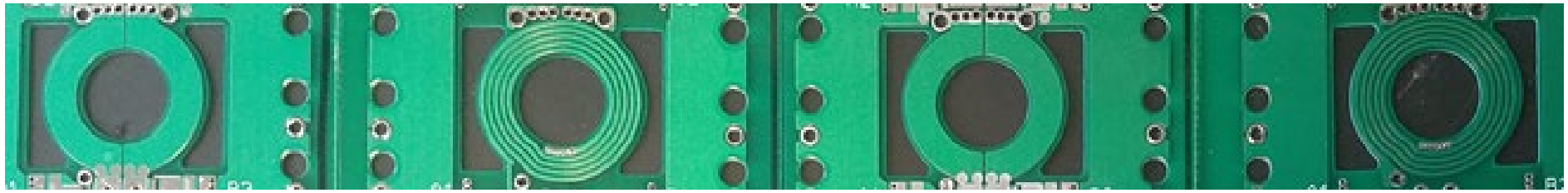
R. Bayliss, "Design, Implementation, and Evaluation of High-Efficiency High-Power Radio-Frequency Inductors," Master's Thesis, MIT, 2021

Employing Planar Magnetics

- **Windings of inductors/transformers implemented as copper traces on printed circuit boards (PCBs)**

Fig. 1. Planar transformer.

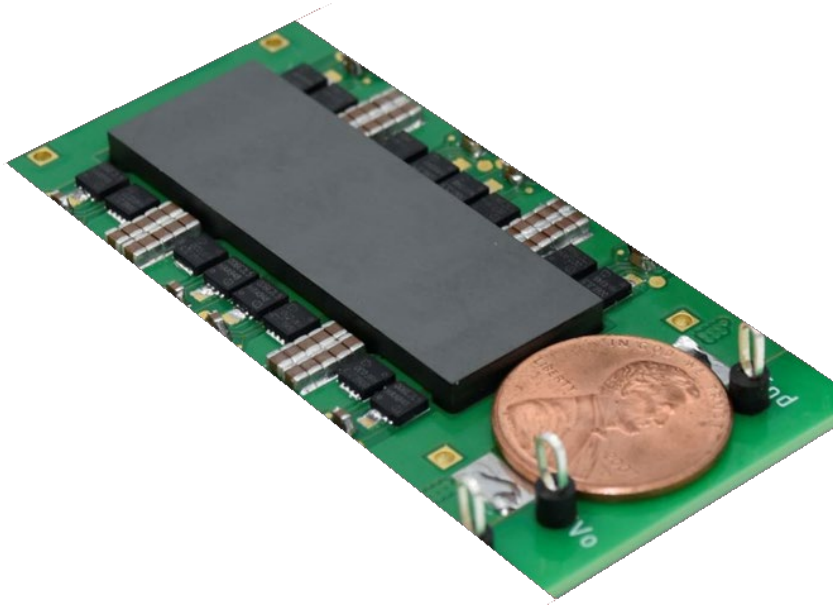


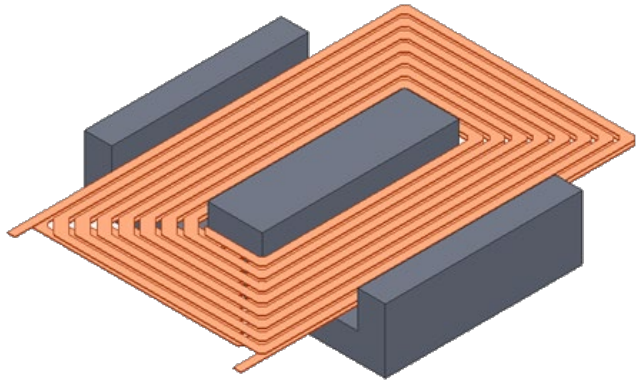


L. H. Dixon, “Designing planar magnetics,” Texas Instruments Application Note. [Online]. Available: http://www.ti.com/download/trng/docs/seminar/Topic4LD.pdf

Planar Magnetics: Cost-Effective, Easy to Build, with Good Thermals

- Low profile (minimize box volume)
- Good thermal characteristics (high surface area to volume)
- Ease of manufacturability
- Highly repeatable
- Lower cost than wire-wound alternatives





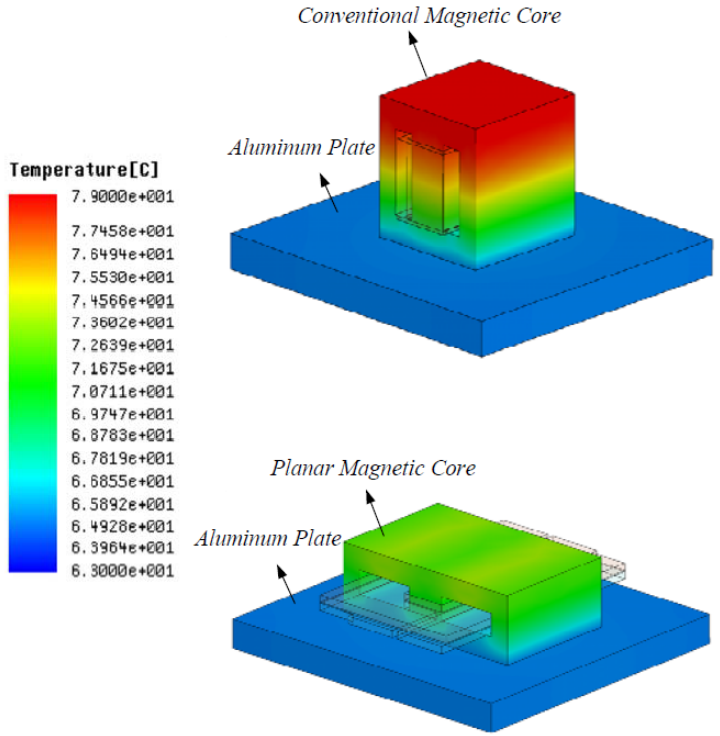
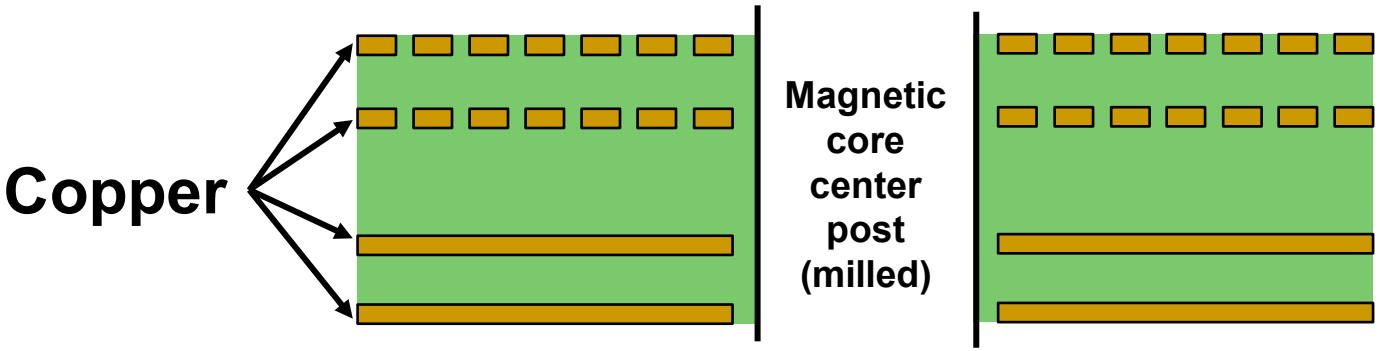


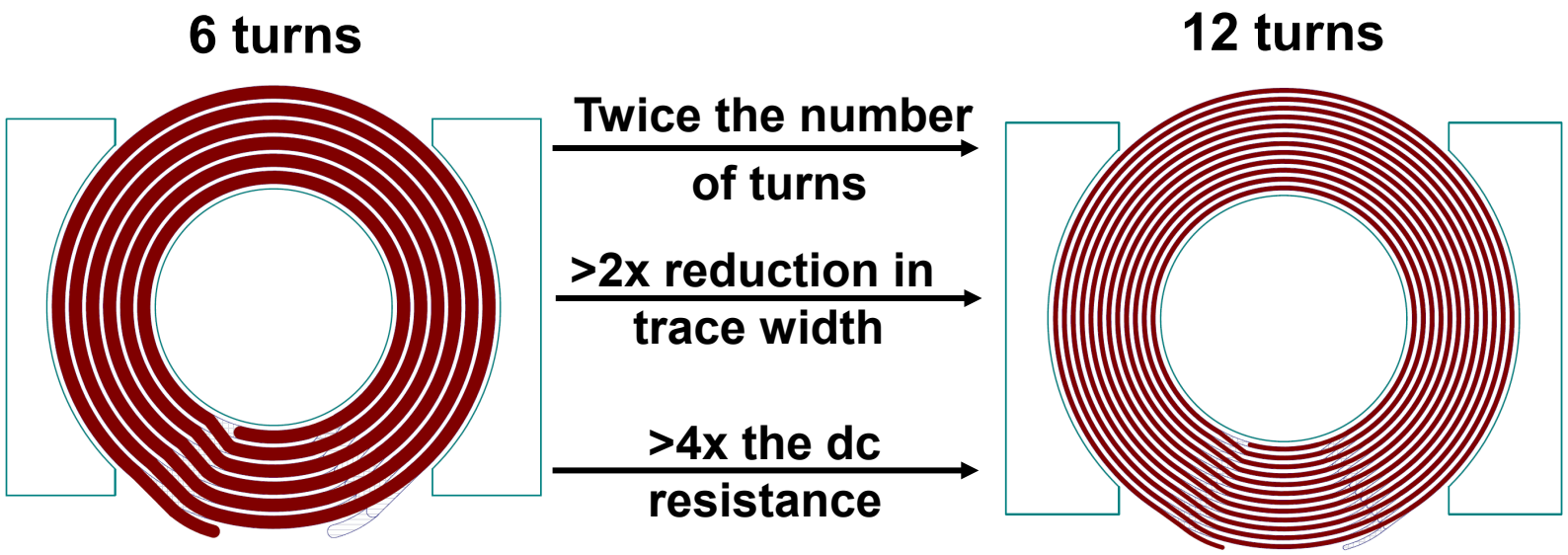
Fig. 1. Comparison of thermal behavior between conventional core and planar core.

Z. Ouyang and M. A. E. Andersen, “Overview of planar magnetic technology - fundamental properties," IEEE Trans. Power Electron., vol. 29, no. 9, pp. 4888-4900, Sep. 2014

Planar Magnetics Difficult w/ High Step-Down, High Current

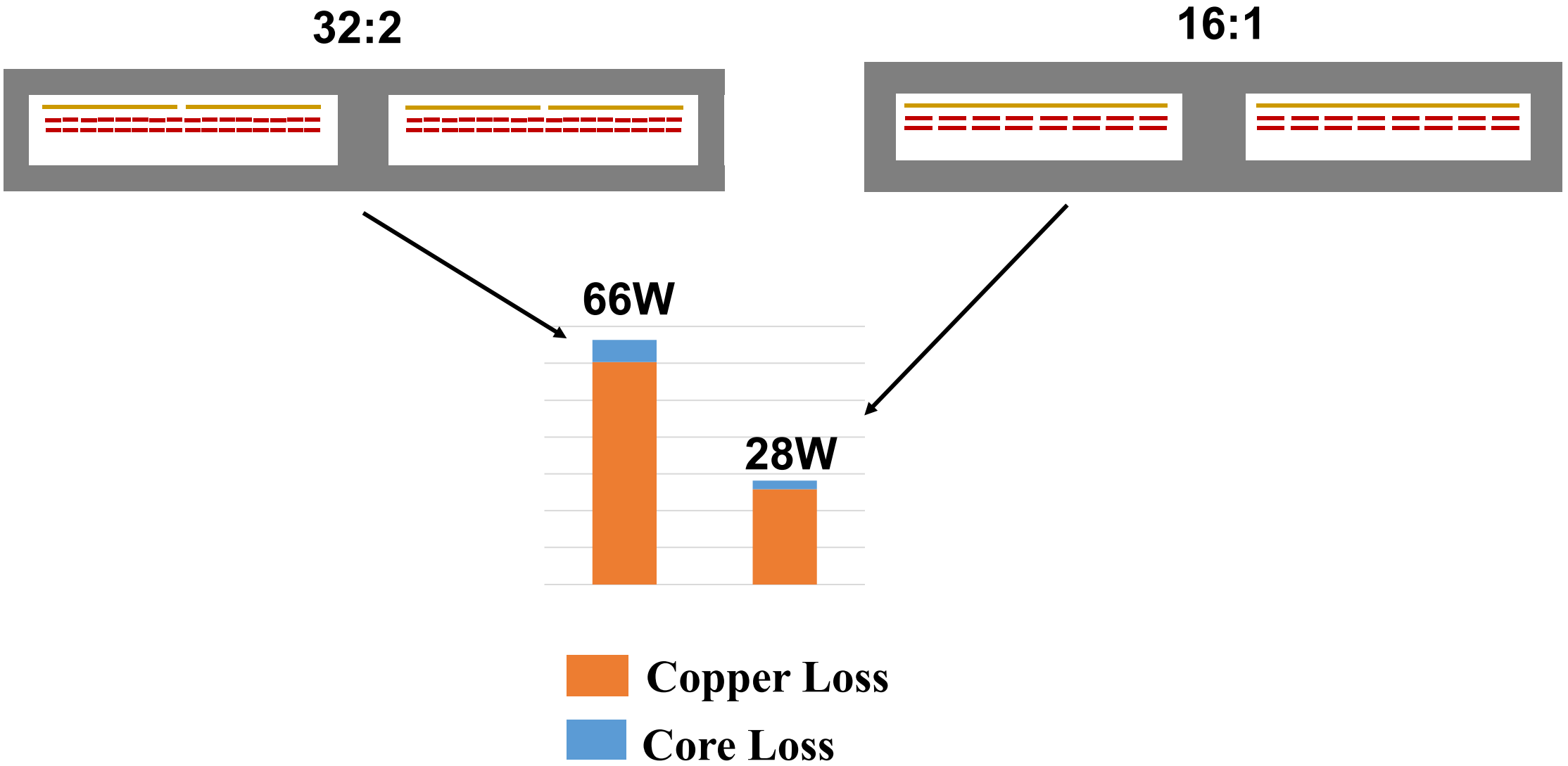


- Poor “fill factor”
- Little area for copper

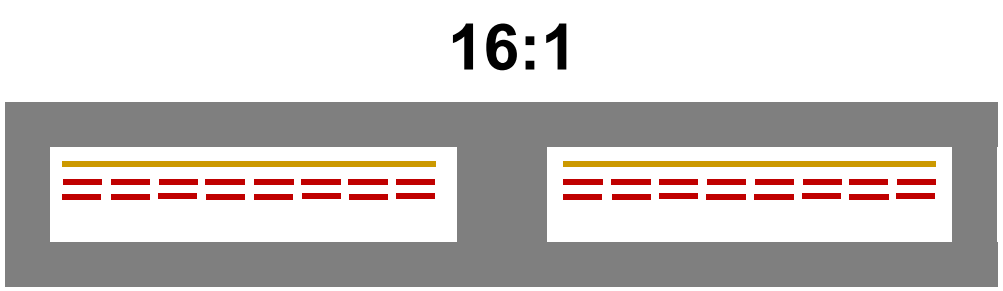


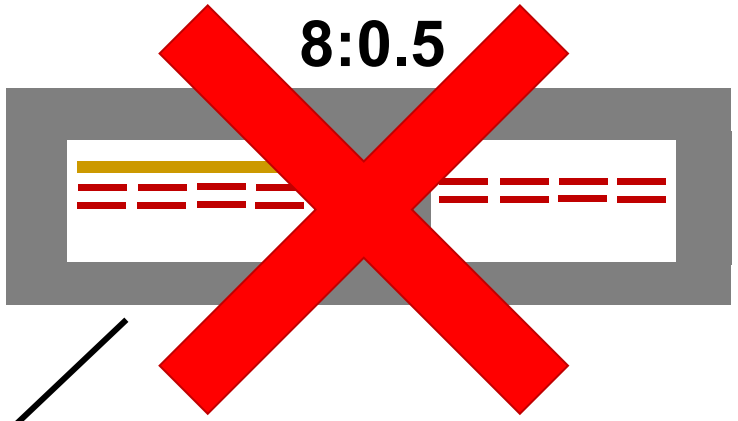
- Large penalty for many turns on a layer

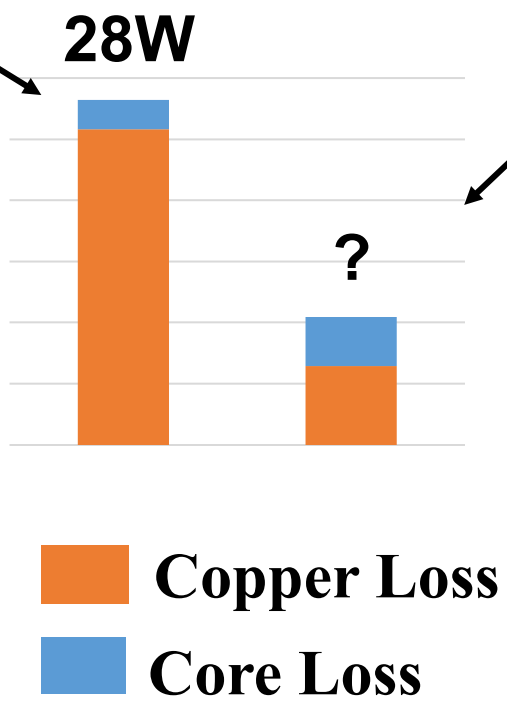
Minimizing Turns Count is Greatly Advantageous

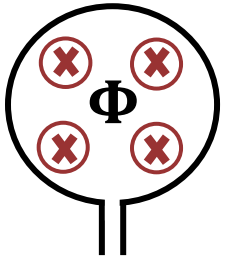


A Fractional Turn as Defined this Way Is Not Practical





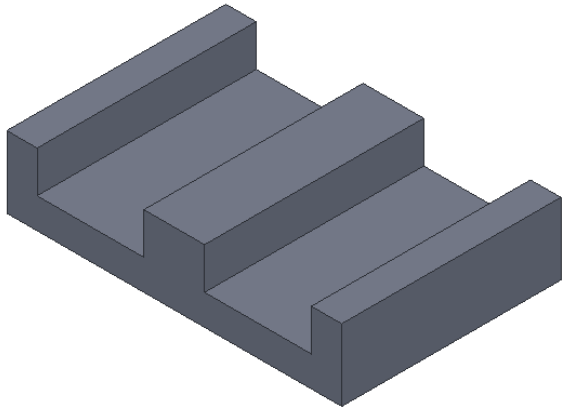




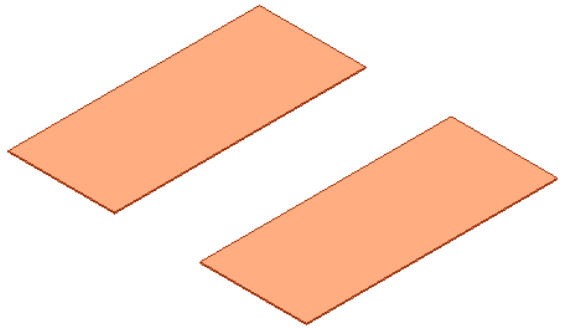
Our courses of action:

- Increase volume
- Try paralleling multiple converters or multiple transformers (matrix transformer)

Taking a Step Back



Magnetic materials

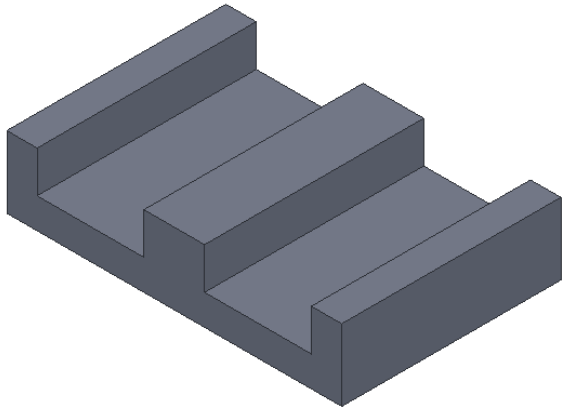


Conductors

Electronics

We can reduce this design into these three key elements

Creating Magnetic Components



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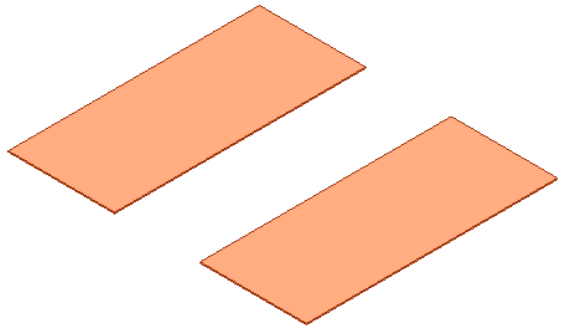
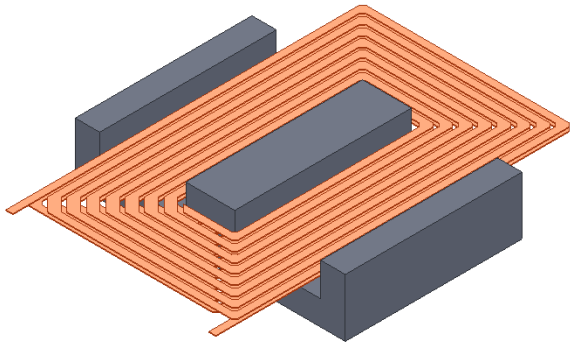


Magnetic materials

Conductors

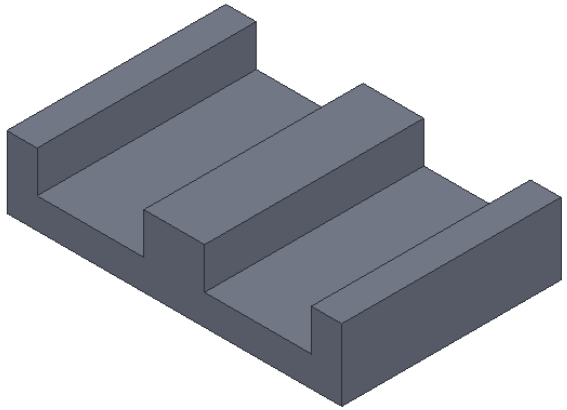
Electronics

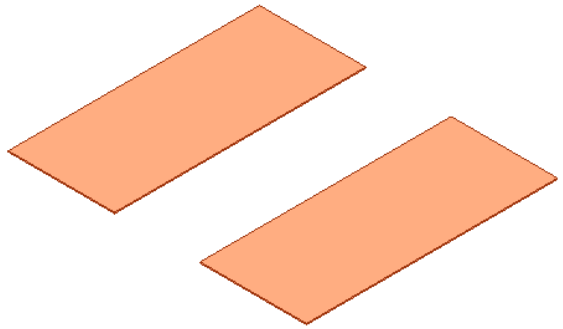


Inductors and transformers

- Today's active areas of research
  - High frequency switching (MHz+)
  - New magnetic materials
  - New winding techniques
  - Planar magnetics
- "Physical domain"

Leveraging Magnetic Components





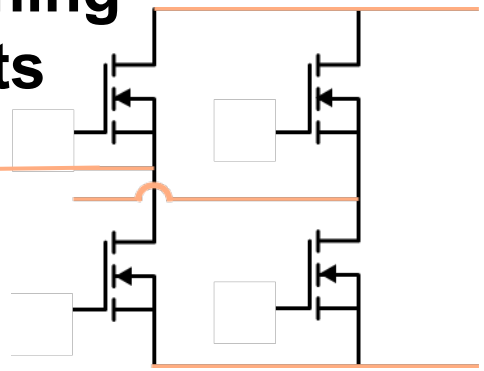
Magnetic materials

Conductors

Electronics

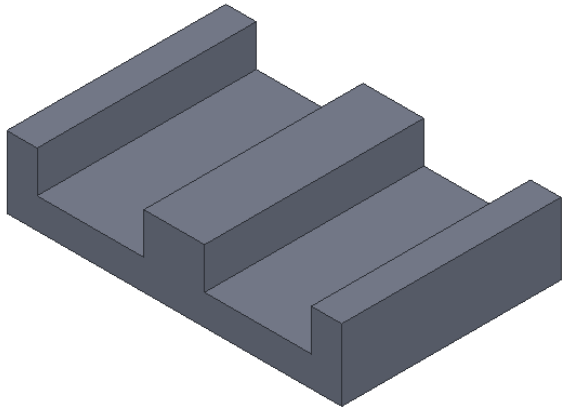
Switching circuits

Inductors and transformers

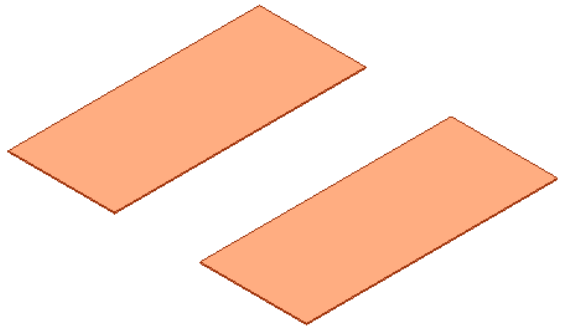


- System/Topology selection
- "Electrical domain"

Can We Explore Something More Fundamental?



Magnetic materials



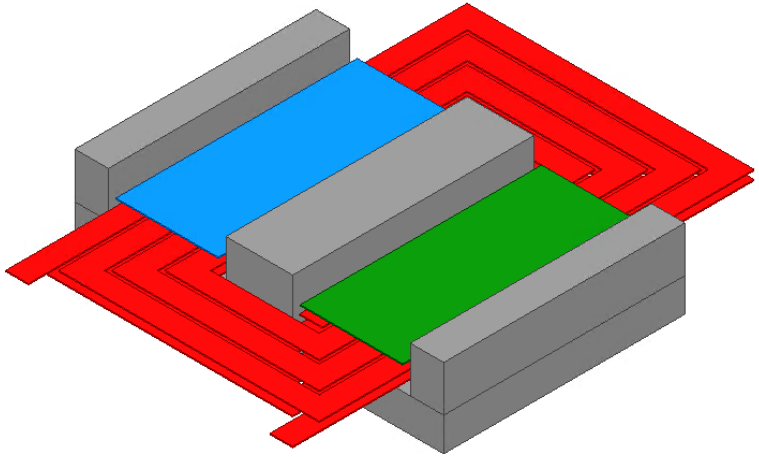
Conductors

Electronics

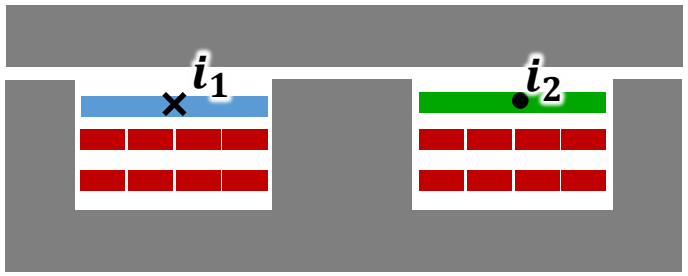
Can we create something different by treating these elements more fundamentally?

A Fractional-Turn Transformer Using a New Kind of Structure

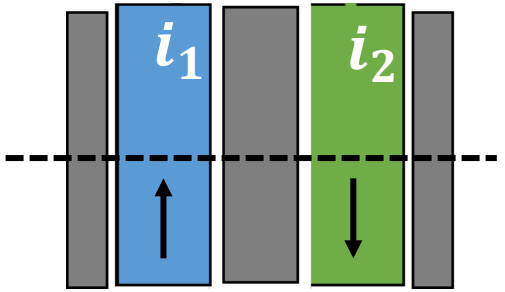
Orthographic View



Side View



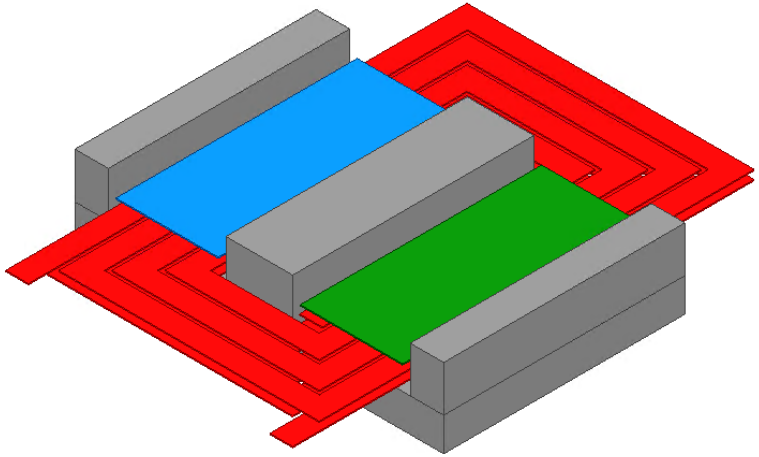
Top View



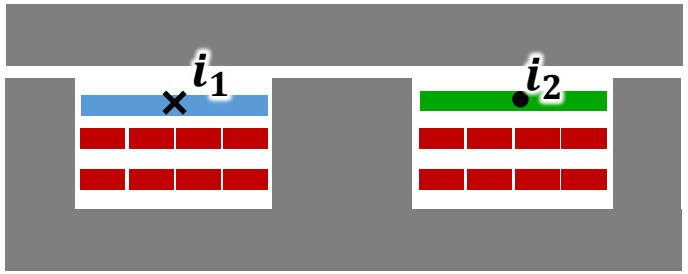
Assume Physical Symmetry About Center of the Core

Assume symmetry

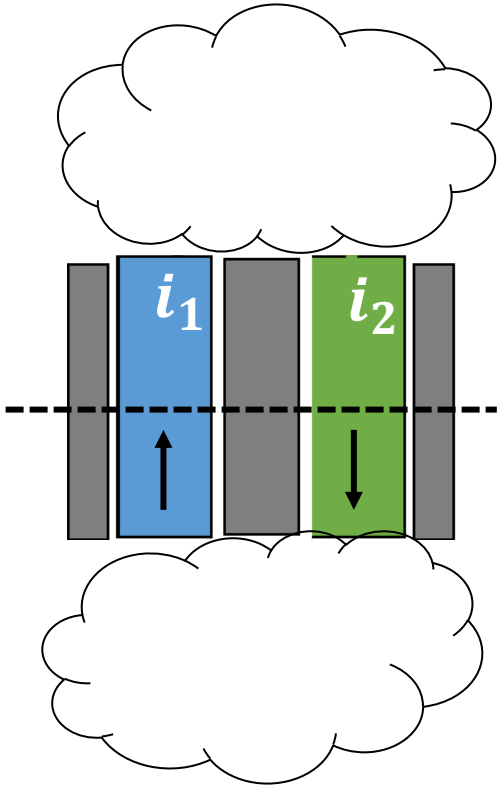
Orthographic View



Side View



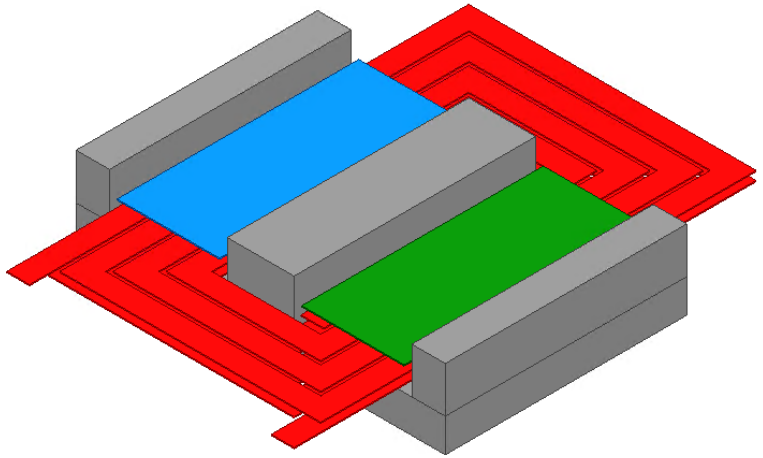
Top View



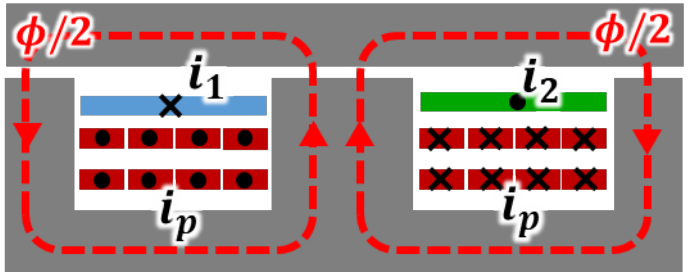
Excite the Primary Winding, Flux Flows Symmetrically

Assume symmetry

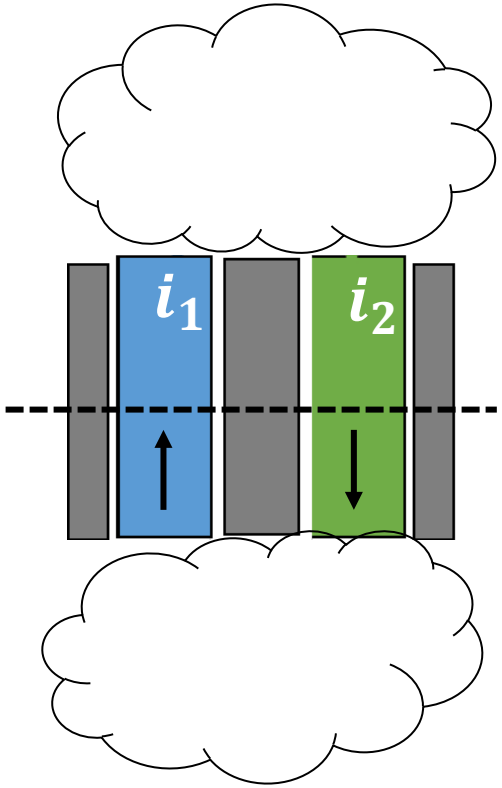
Orthographic View



Side View



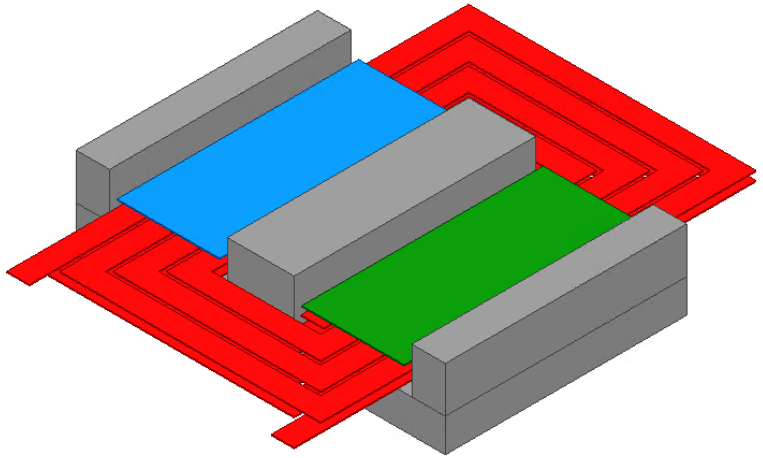
Top View



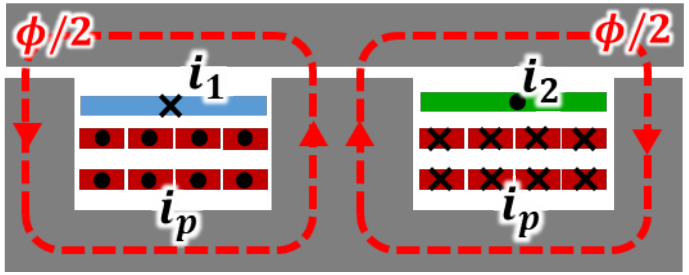
Symmetry and Magnetic Core Enforce Equal Currents

Assume symmetry

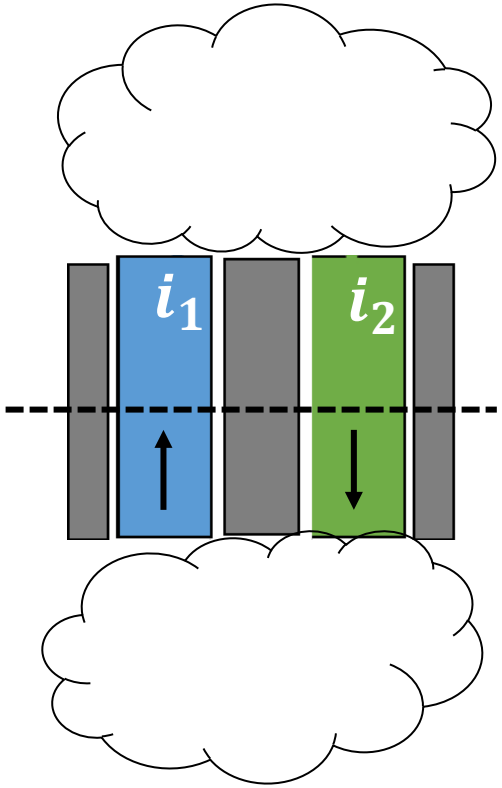
Orthographic View



Side View



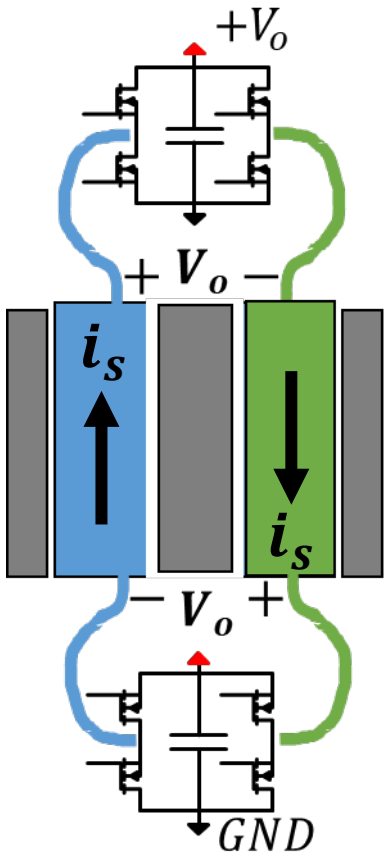
Top View

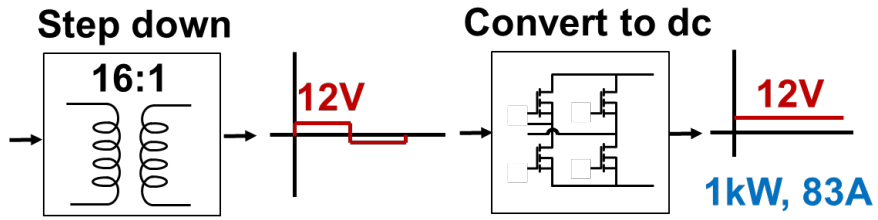


$$\oint H.dl = 8i_p - i_1 = 8i_p - i_2 \quad \Rightarrow \quad i_1 = i_2 \text{ by symmetry}$$

Symmetrically Distribute Two Full Bridge Rectifiers Around the Core

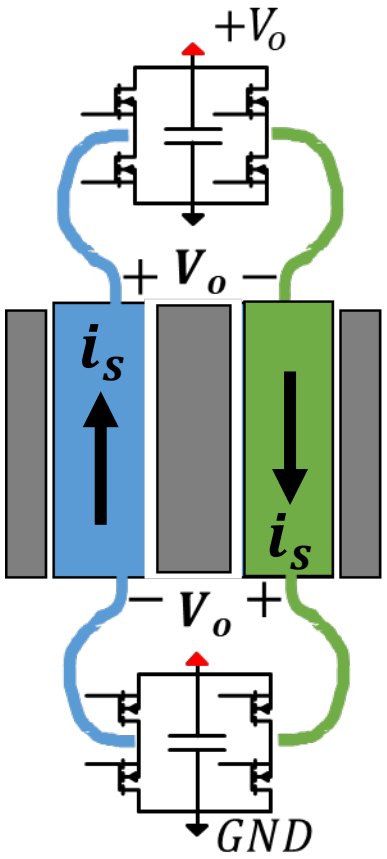
Top View





The Structure Behaves Like a Fractional Turn Transformer

Top View

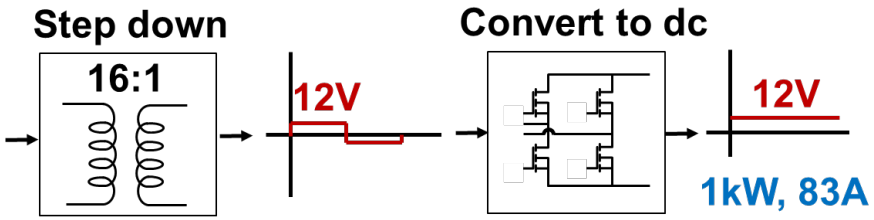


- Free to treat conductors as independent elements
- Connections yield:

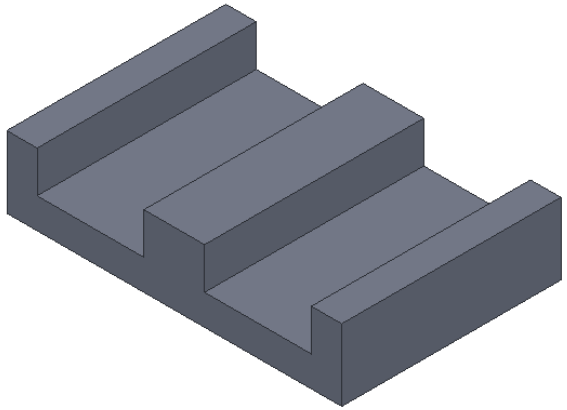
$$2V_o = \frac{V_p}{N_p}$$

$$\frac{V_o}{V_p} = \frac{1/2}{N_p}$$

A fractional turn transformer



The CEMS Concept: A tighter integration of these elements



Magnetic materials

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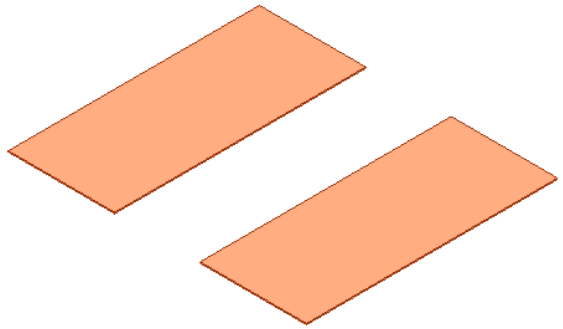


Conductors

+

Electronics

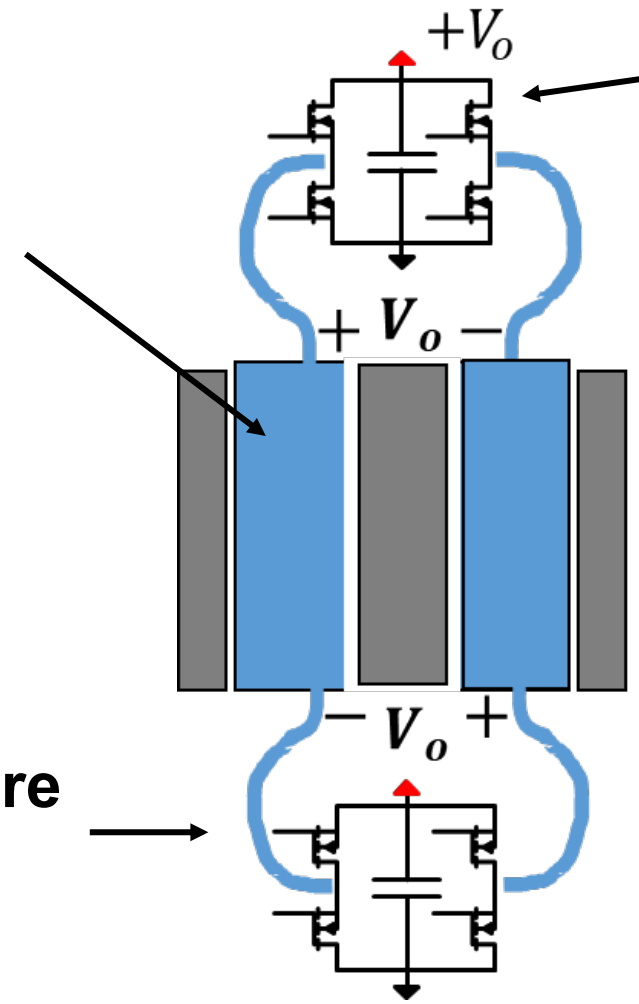
Physical domain + Electrical domain

View and design these as one coupled system

We call this a “Coupled Electronic and Magnetic System” (CEMS)

VIRT: An Example of a Coupled Electronic and Magnetic System

Equivalence of induced currents is ensured by symmetry



Connecting electronics are physically distributed around the core

Electronics can be controlled to modify magnetic properties

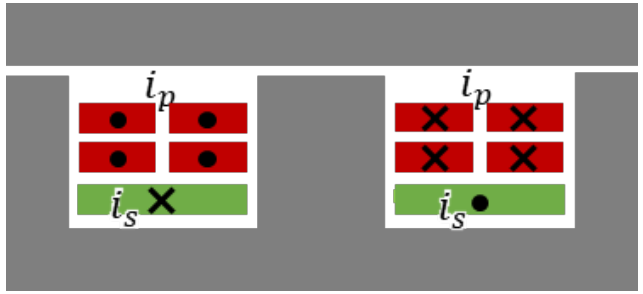
FB/FB:	$N_p: \frac{1}{2}$
FB/HB:	$N_p: \frac{2}{3}$
HB/HB:	$N_p: 1$
HB/0:	$N_p: 2$

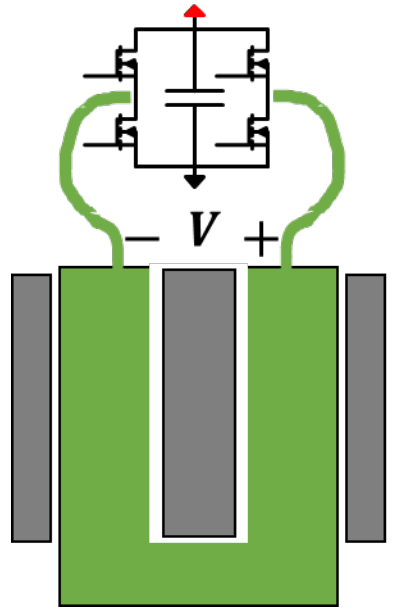
Requires a different modeling framework

M. K. Ranjram, I. Moon and D. J. Perreault, "Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure Enabling Adjustable High Step-Down Conversion Ratios," in *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6509-6525, Aug. 2018, doi: 10.1109/TPEL.2018.2795959.

How Turns Implementation Affects Losses

- **Copper loss** $\propto i^2 R \longrightarrow \propto N^2$
- **Core loss** $\propto \left(\frac{V}{N}\right)^{\beta} \longrightarrow \propto \left(\frac{1}{N}\right)^{3}$





Turns Implementation	Relative Cu loss	Relative Core Loss
32:2	4	1/8
16:1	1	1

How Turns Implementation Affects Losses

- Copper loss $\propto i^2 R \longrightarrow \propto N^2$
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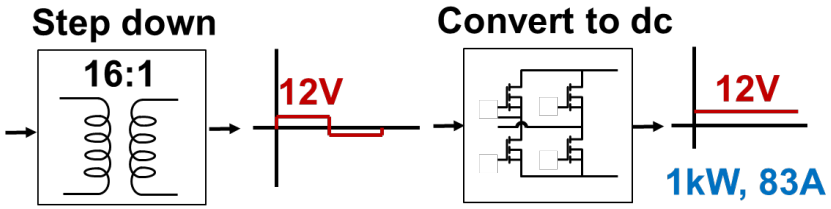
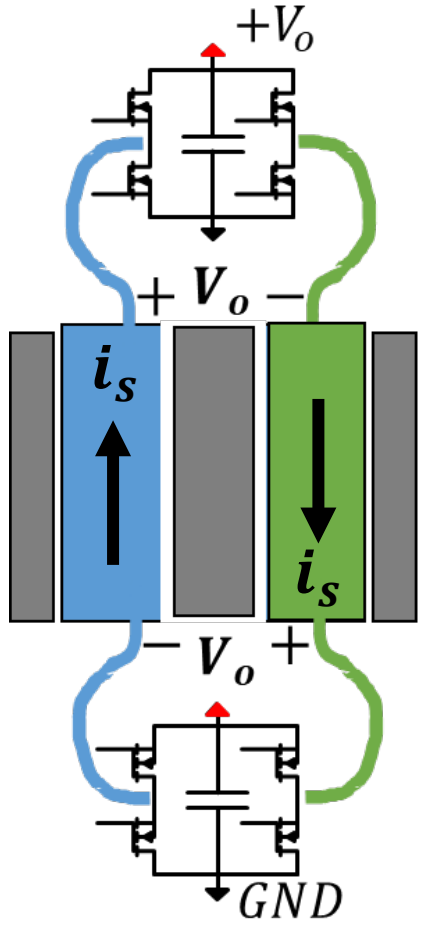
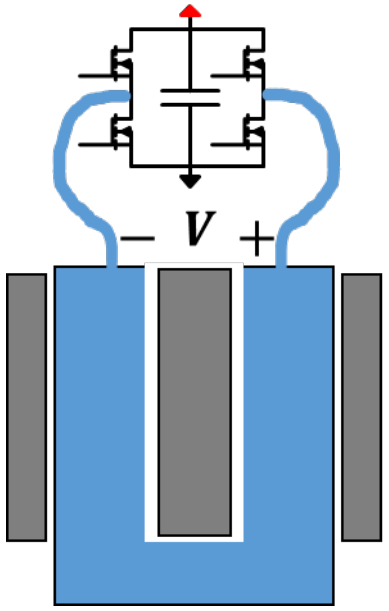


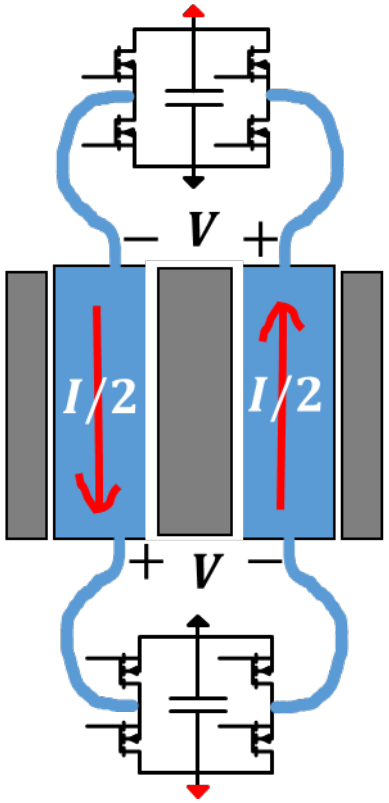


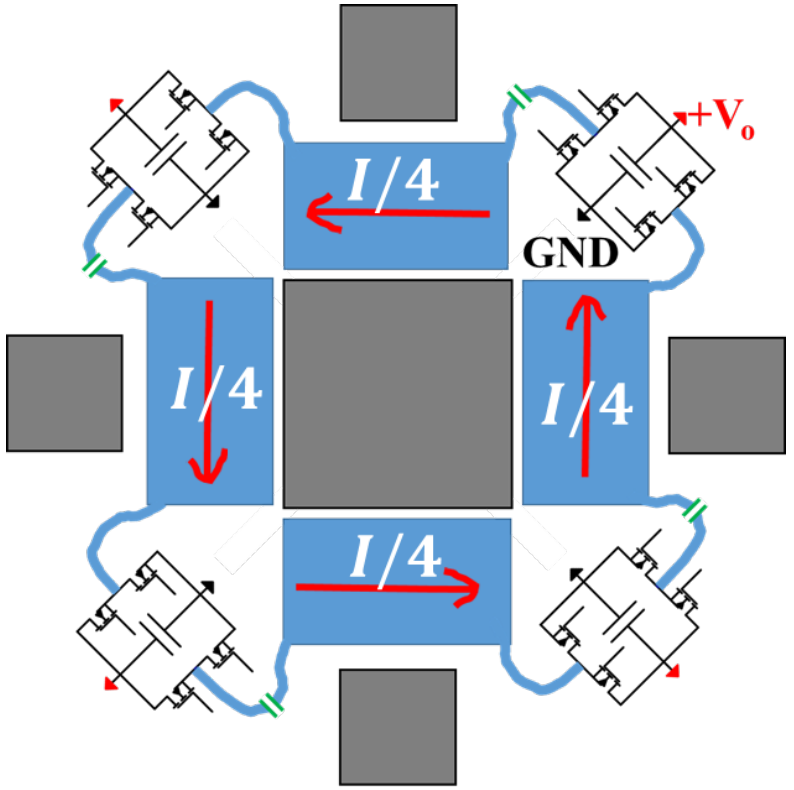
Turns Implementation	Relative Cu loss	Relative Core Loss
32:2	4	1/8
16:1	1	1
8:0.5	¼	8

- Follows the right trend

Correct Trade-off: Exponential Rebalancing



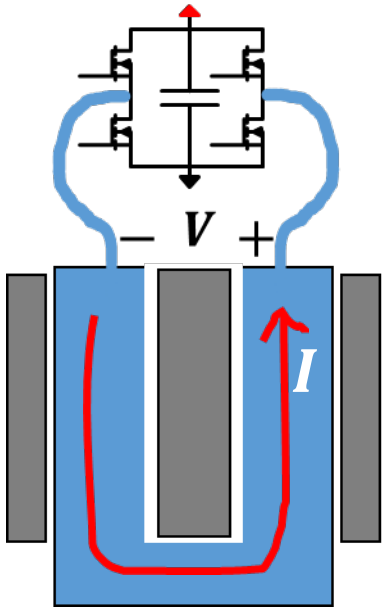




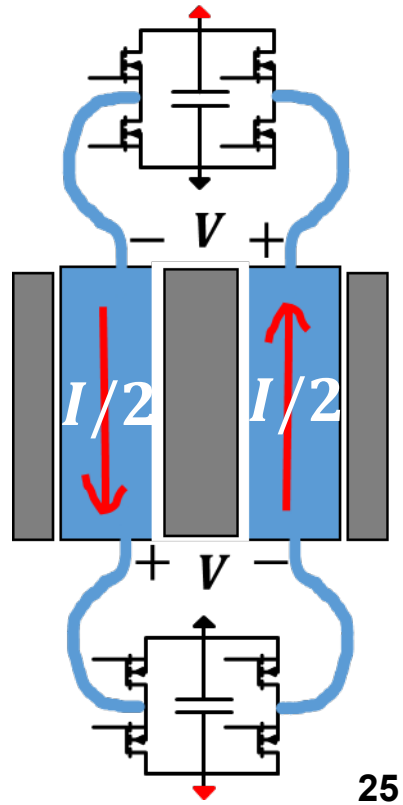
	$2N_p$: 2	N_p:1	Half-turn VIRT N_p: 0.5	Quarter-turn VIRT N_p: 0.25
P_{cu}	**4**	**1**	**~1/4**	**~1/16**
P_{core}	$2^{-\beta}$	1	$\sim 2^{\beta}$	$\sim 2^{2\beta}$

What about the Transistors?

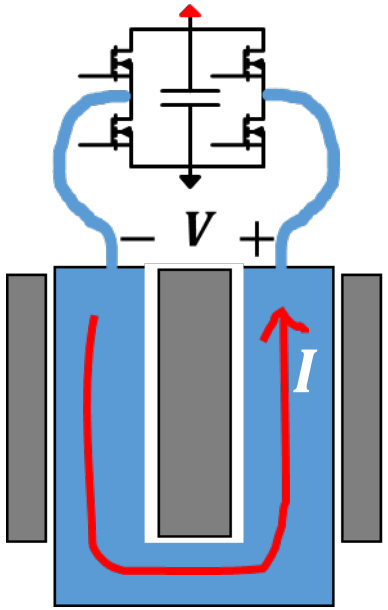
- Twice as many switches, but each carries half the current for the same output power and voltage
- For same transistor area, identical transistor loss
- An advantage at high output currents, easier terminations without direct parallelization.



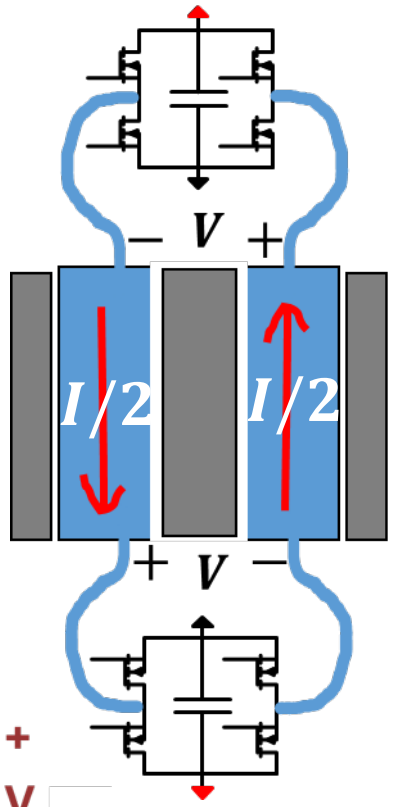
Mode	NON-VIRT	VIRT
FB-FB	$P_{cond} = 2\frac{R_{on}}{2} I_o^2 = R_{on} I_o^2$	$P_{cond} = 4R_{on}\left(\frac{I_o}{2}\right)^2 = R_{on} I_o^2$
HB-HB	$P_{cond} = 2\frac{R_{on}}{2} I_o^2 = R_{on} I_o^2$	$P_{cond} = 4R_{on}\left(\frac{I_o}{2}\right)^2 = R_{on} I_o^2$

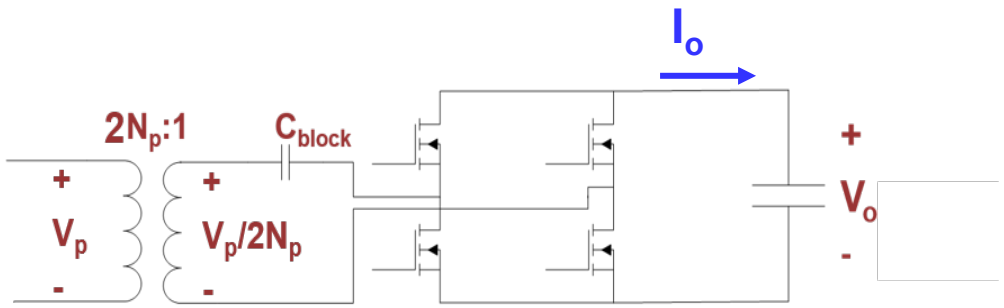


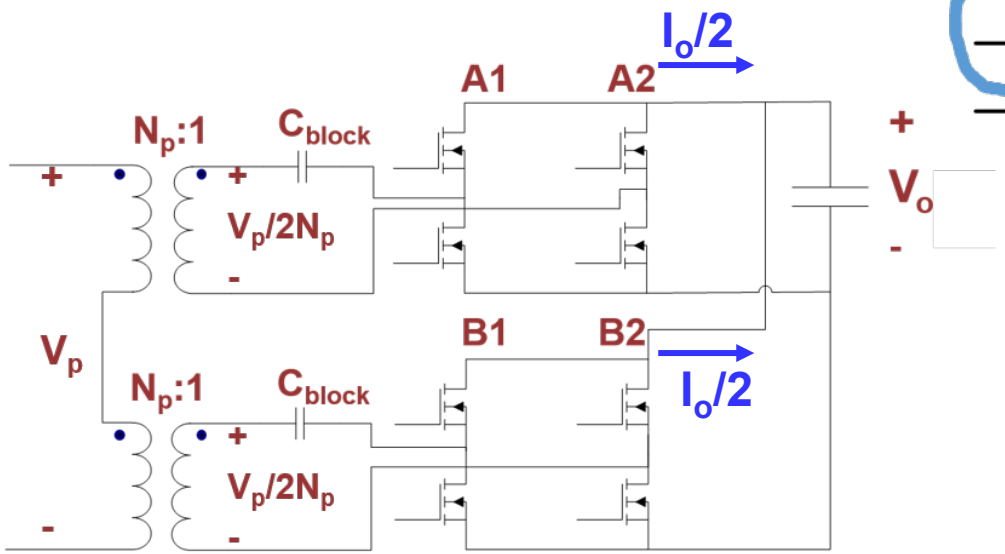
What about the Transistors?



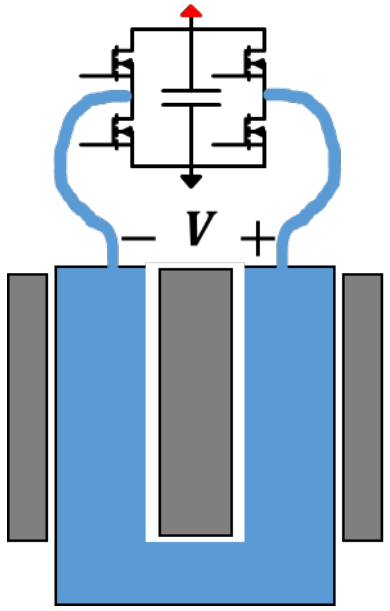
Mode	NON-VIRT	VIRT
FB-FB	$P_{cond} = 2\frac{R_{on}}{2} I_o^2 = R_{on} I_o^2$	$P_{cond} = 4R_{on}\left(\frac{I_o}{2}\right)^2 = R_{on} I_o^2$
HB-HB	$P_{cond} = 2\frac{R_{on}}{2} I_o^2 = R_{on} I_o^2$	$P_{cond} = 4R_{on}\left(\frac{I_o}{2}\right)^2 = R_{on} I_o^2$







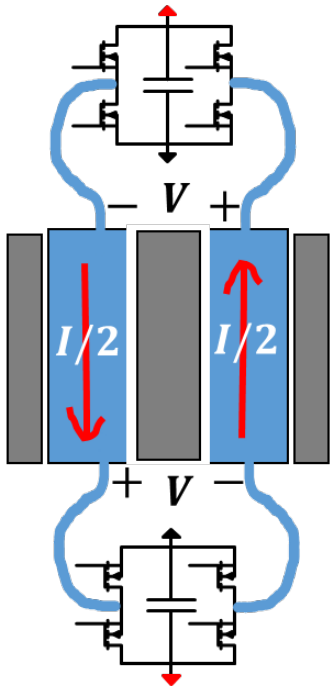
Variability Comparison



FB: $N_p: 1$

HB: $N_p: 2$

Half-turn VIRT



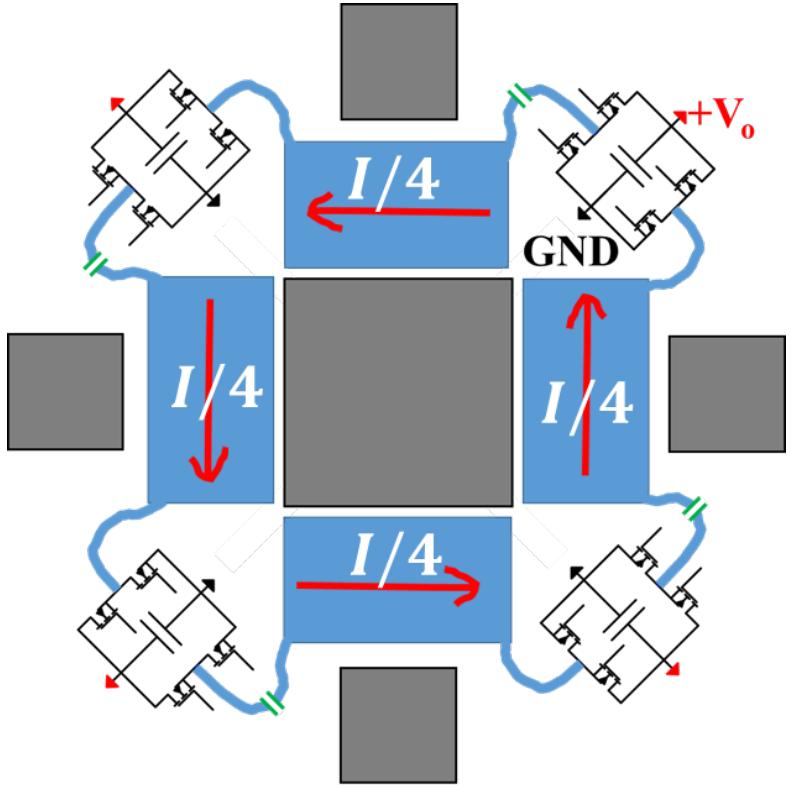
FB/FB: $N_p: \frac{1}{2}$

FB/HB: $N_p: \frac{2}{3}$

HB/HB: $N_p: 1$

HB/0: $N_p: 2$

Quarter-turn VIRT

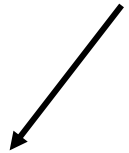


8 possibilities,

$N_p: \frac{1}{4}, \frac{2}{7}, \frac{1}{3}, \frac{2}{5}, \frac{1}{2}, \frac{2}{3}, 1, 2$

Two Key VIRT Features

Variable Inverter/Rectifier Transformer



- **Variability** for:
  - Accommodating wide voltage variations

Two Key VIRT Features

Variable Inverter/Rectifier Transformer

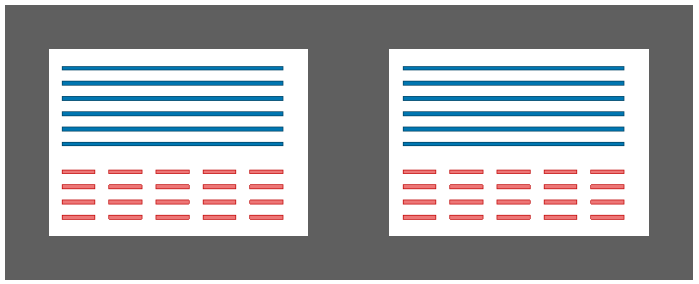
- **Variability** for:
  - Accommodating wide voltage variations
- **Fractional turns** for:
  - High current carrying capability
  - Reducing the number of primary turns in high step-down transformers (adv. for planar magnetics)

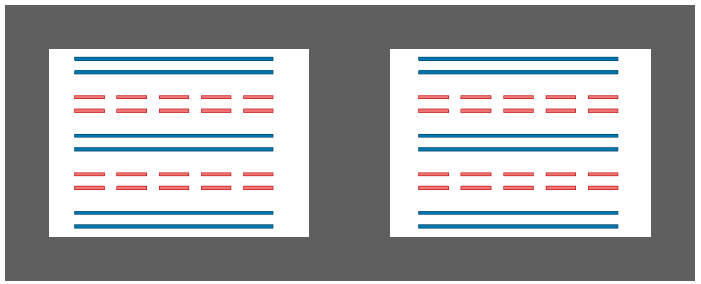
What About Winding Techniques?

- Today's active areas of research
  - High frequency switching (MHz+)
  - New magnetic materials
  - Planar magnetics
  - Novel winding techniques

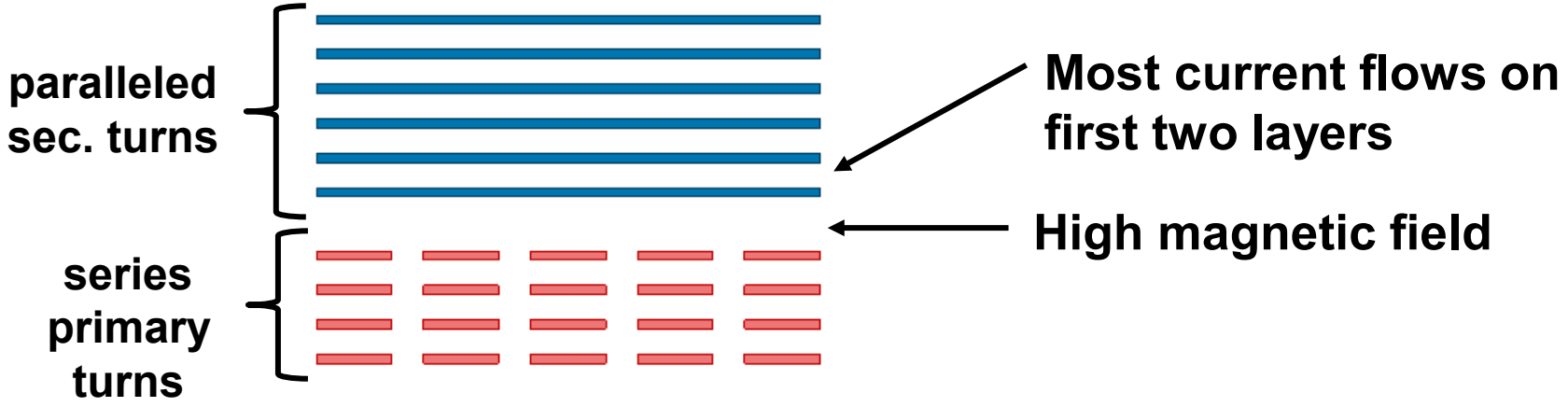
- The magnetic component's ability to carry current is strongly dependent on how it's wound, especially at high frequencies.

Copper Loss Reduction by Parallelizing Windings With Interleaving

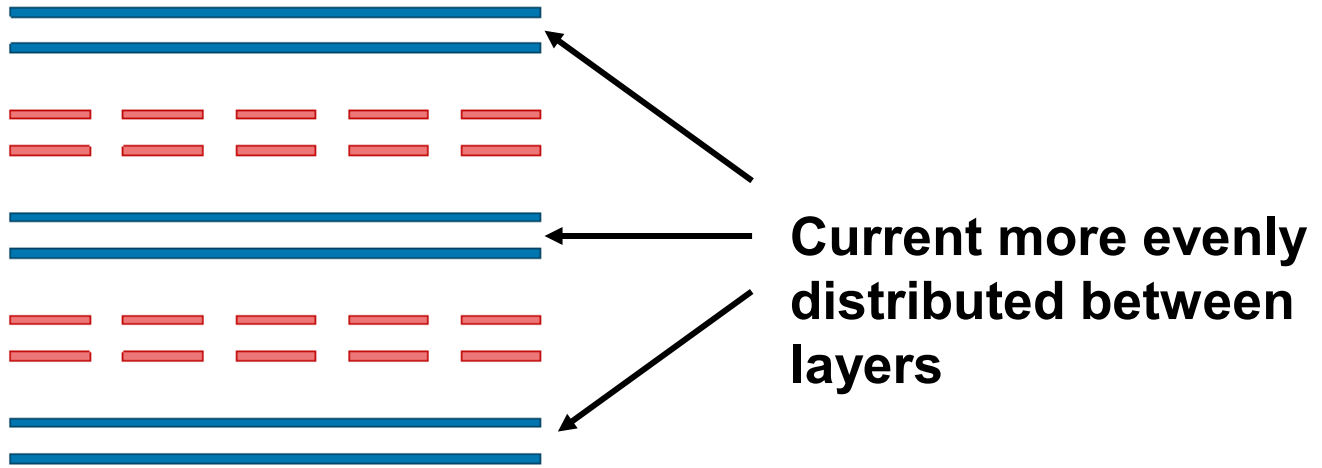




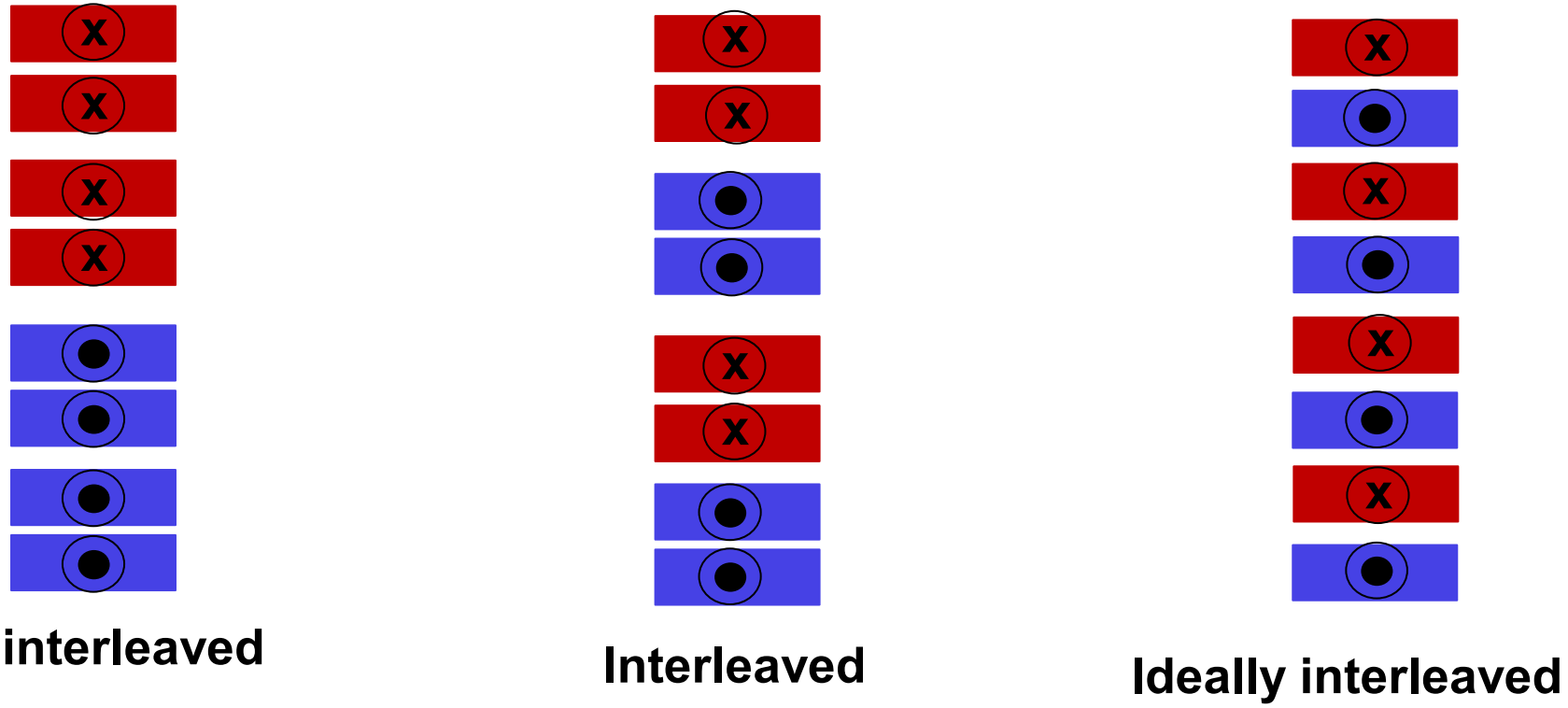
Non-interleaved



Interleaved



Resistance vs. Capacitance Trade-off of Interleaving



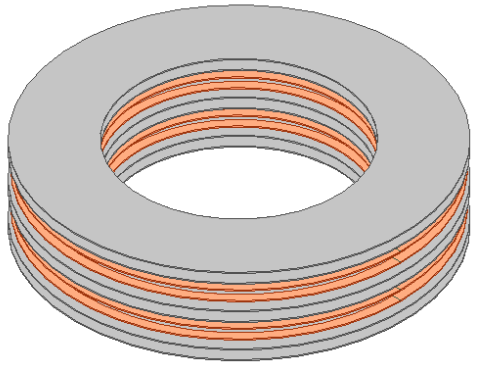
ac resistance → lower

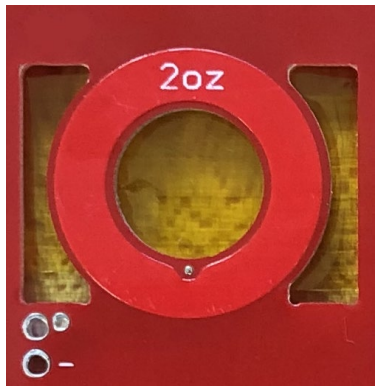
capacitance → higher

termination loss → Much higher

With Realistic Terminations, Loss is 2.5x Higher Than Expected

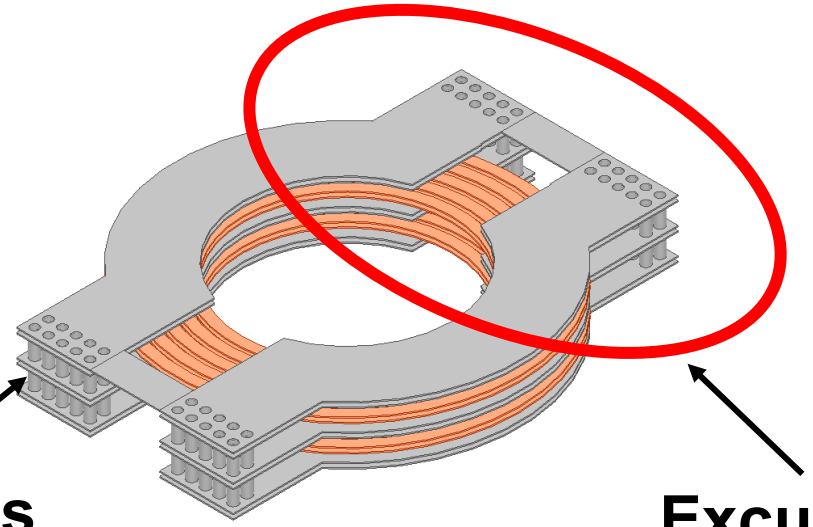
Ideal, perfectly terminated





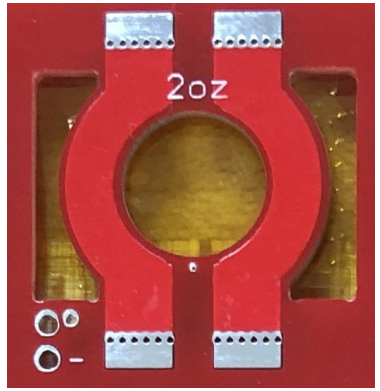
0.29Ω

Practically terminated



Via losses

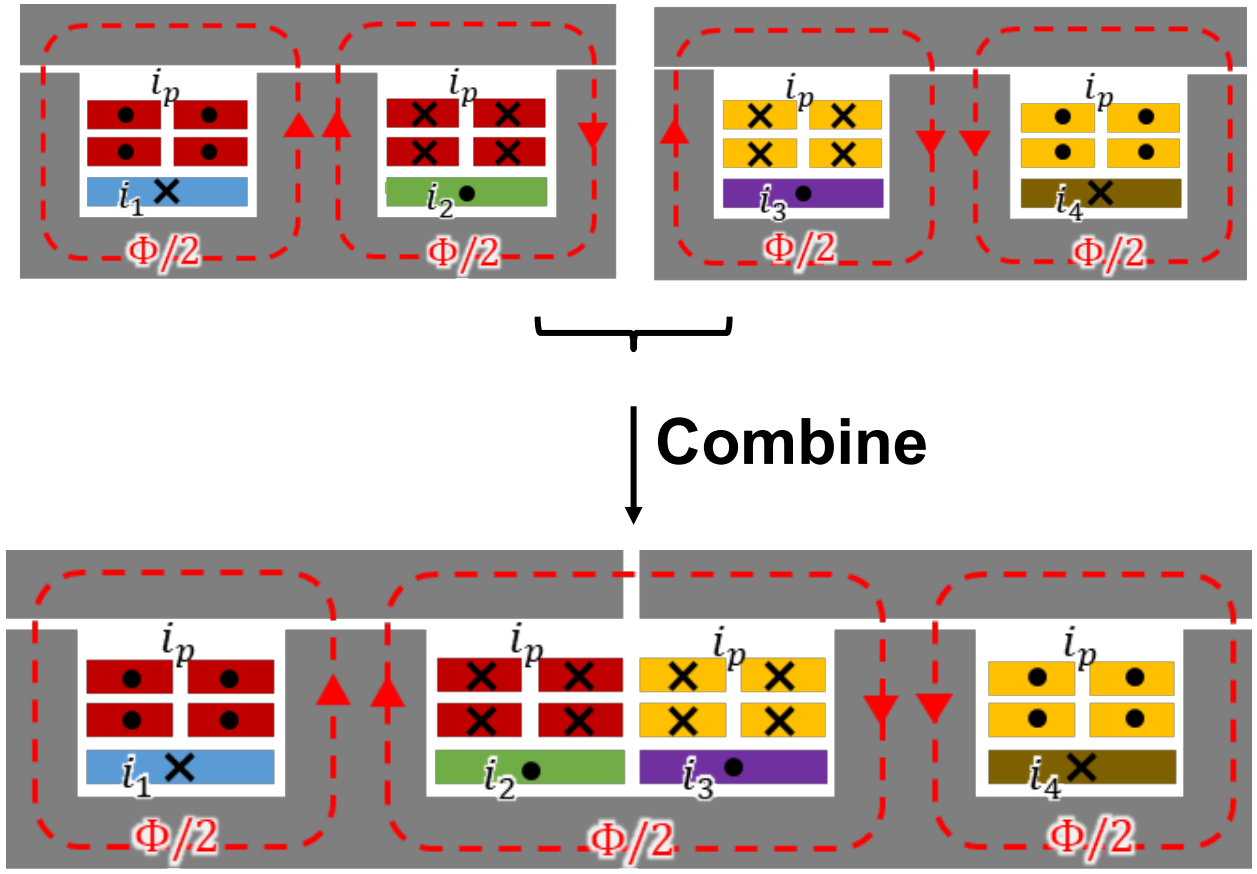
Excursion penalties



0.73Ω

High Current Planar Magnetics

- If we want to carry high current in a planar magnetic, complex vertical stack-ups are problematic
- A better choice: transformer parallelization

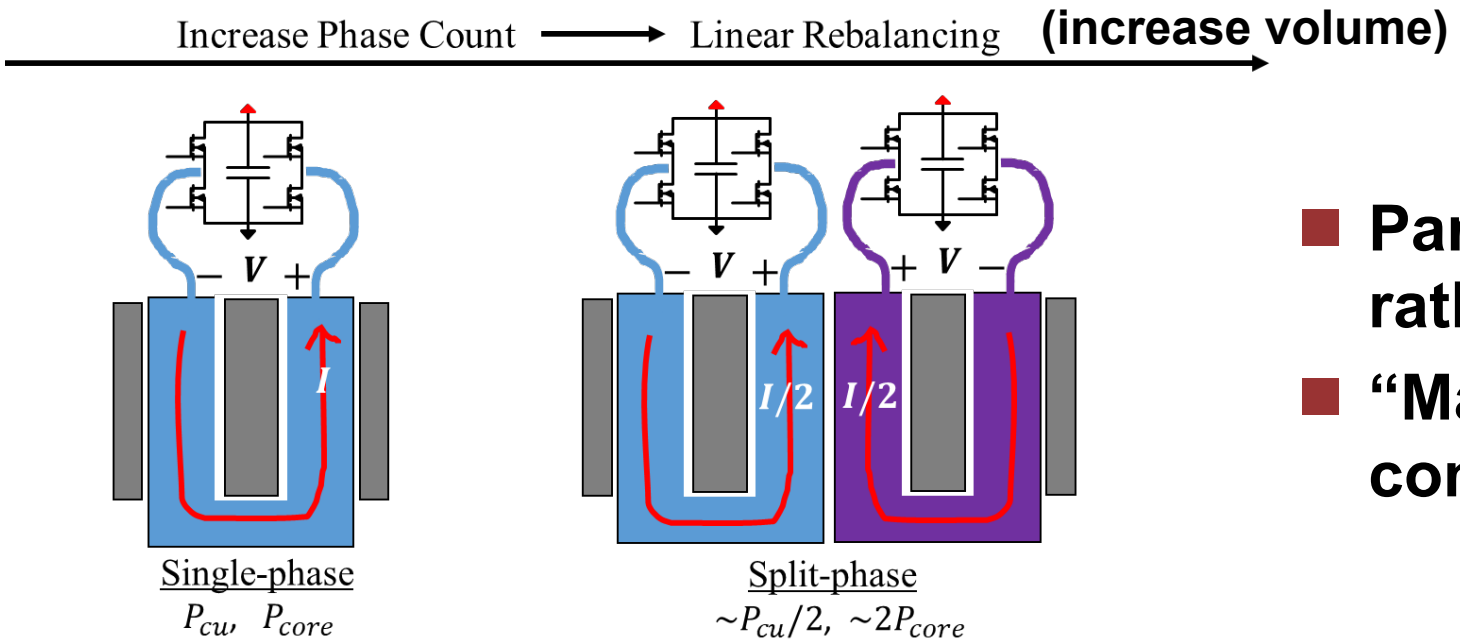


Wound such that equal and opposite flux flows on outer legs

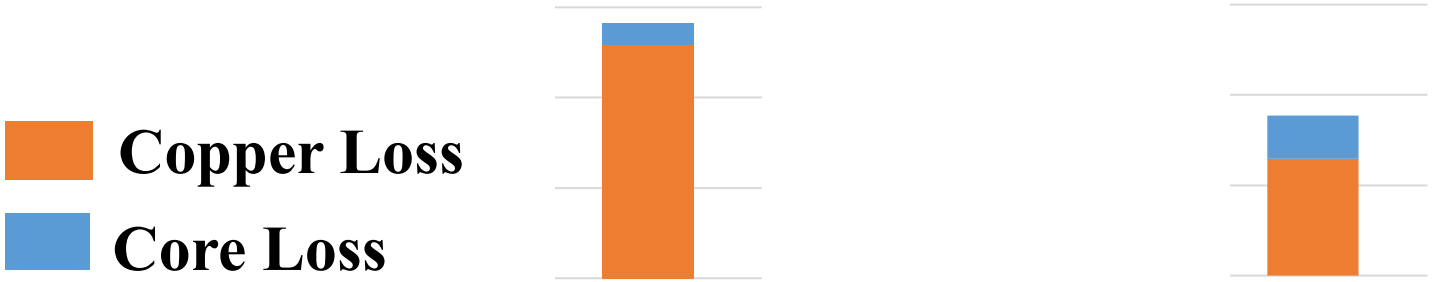
Combine cores for volume reduction

High Current Planar Magnetics

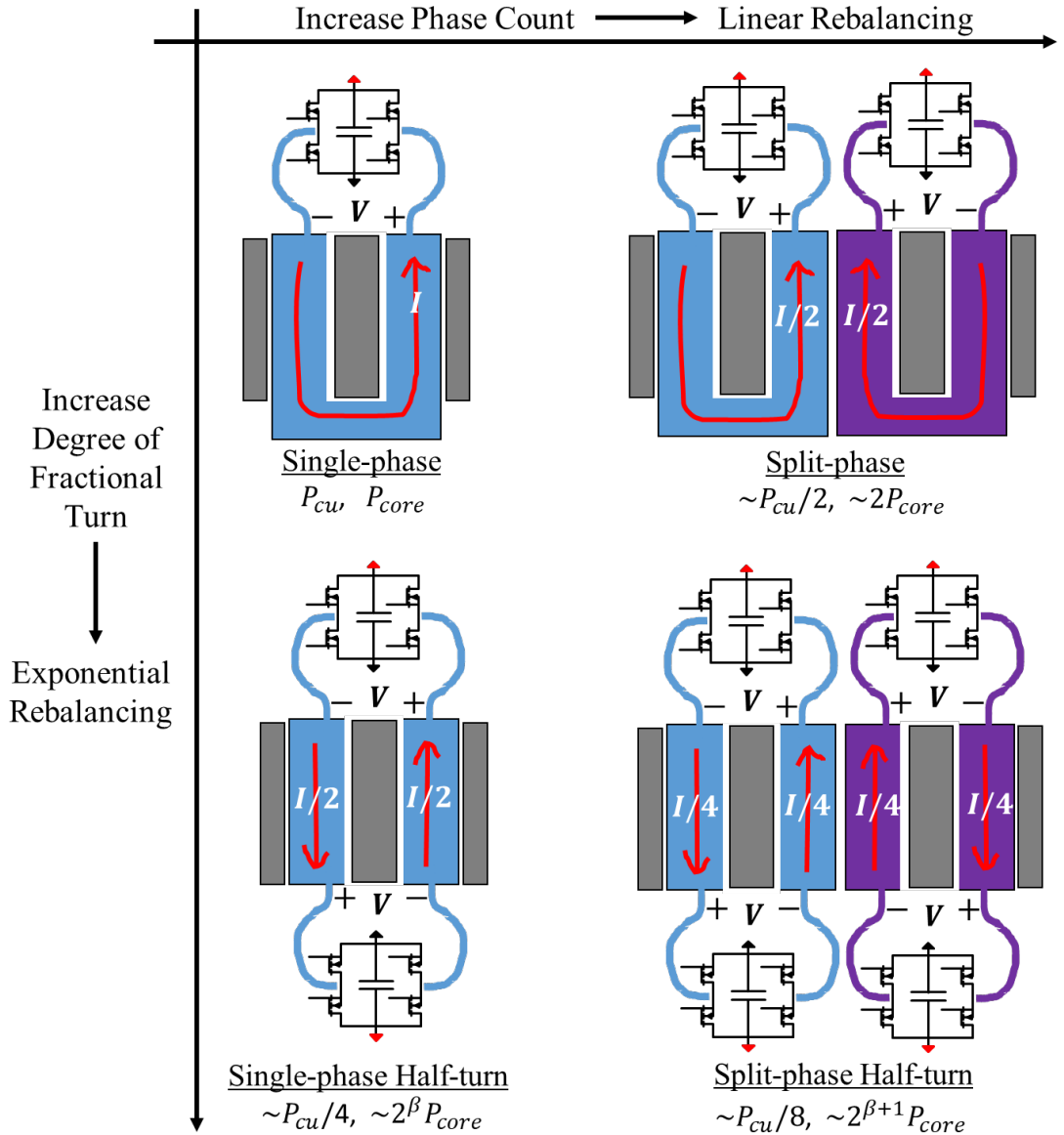
- If we want to carry high current in a planar magnetic, complex vertical stack-ups are problematic
- A better choice:



- Parallel "horizontally" rather than "vertically"
- "Matrix transformer" concept applies here



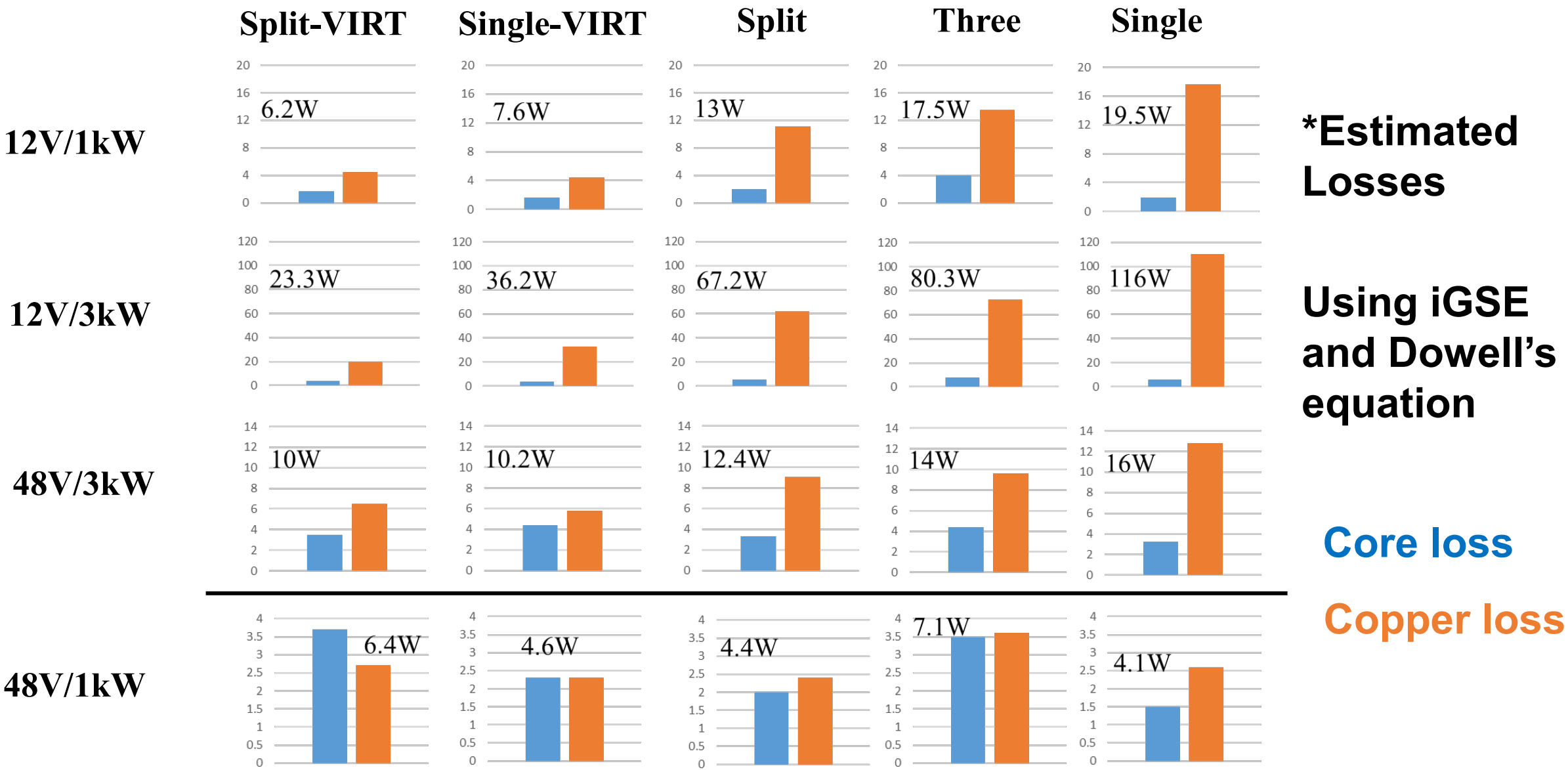
“Gear Shifting” Transformer Core and Copper Loss



SPHTV

M. K. Ranjram and D. J. Perreault, "Leveraging Multi-Phase and Fractional-Turn Integrated Planar Transformers for Miniaturization in Data Center Applications," *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, 2020, pp. 1-8, doi: 10.1109/COMPEL49091.2020.9265752.

Transformer loss “Gear Shifting” Is Beneficial



***Estimated Losses**

Using iGSE and Dowell’s equation

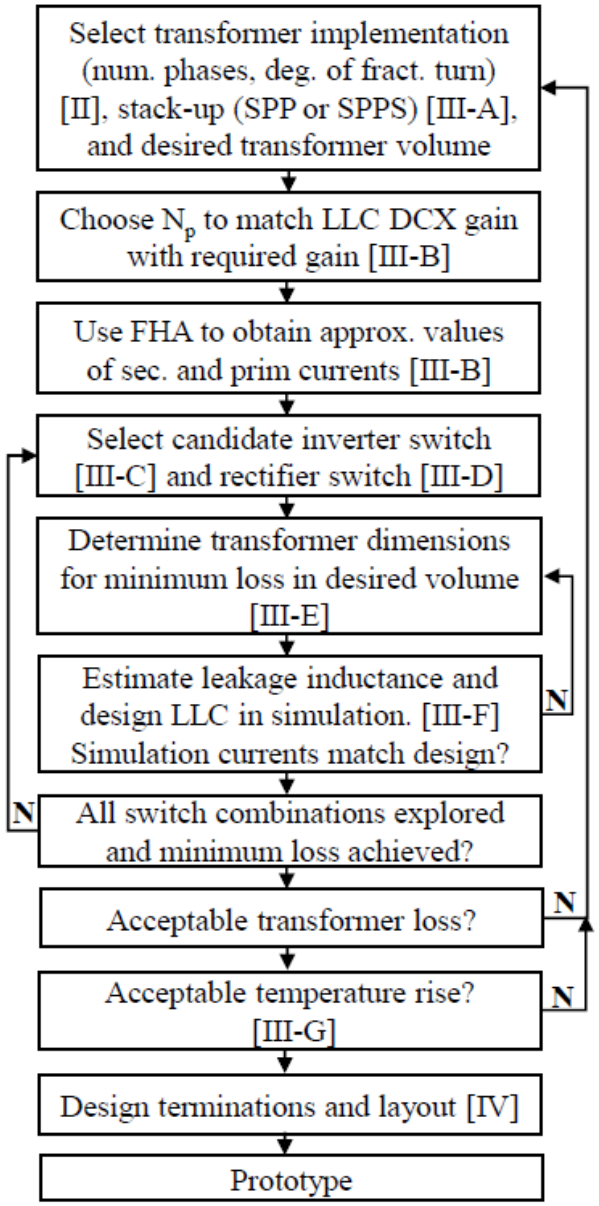
Core loss

Copper loss

K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters,” in *Proc. IEEE Workshop Comput. Power Electron,*2002, pp. 36–41.

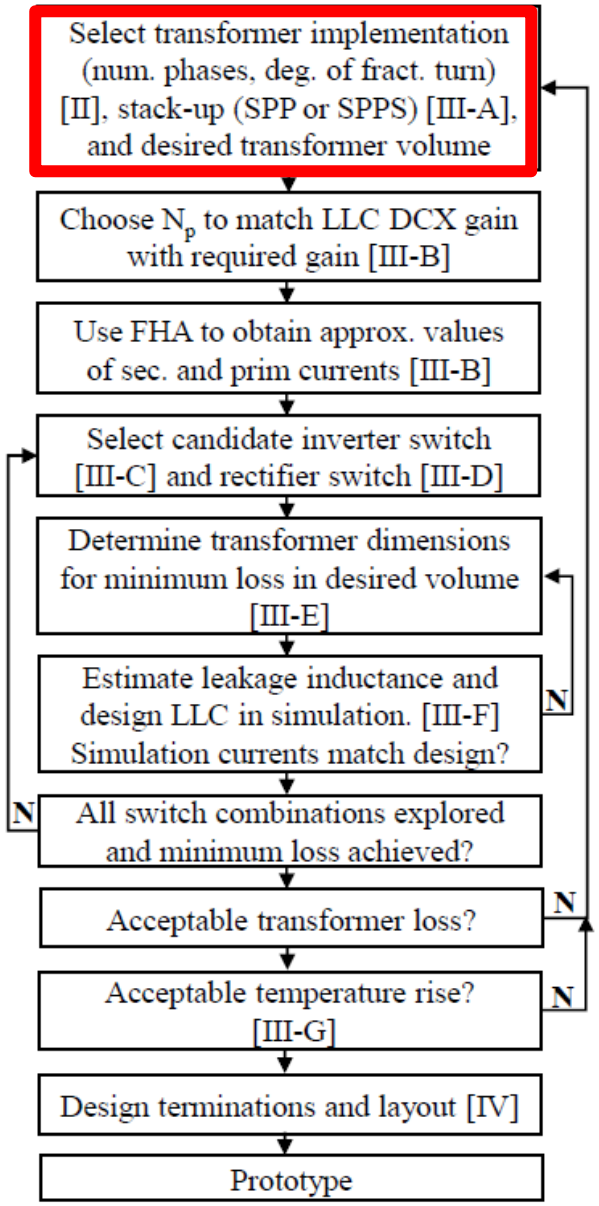
P. L. Dowell, “Effects of eddy currents in transformer windings,” in *Proc. Inst. Elect. Engineers*, vol. 113, no. 8, pp. 1387–1394, 1966

Building a High Performance SPHTV Prototype

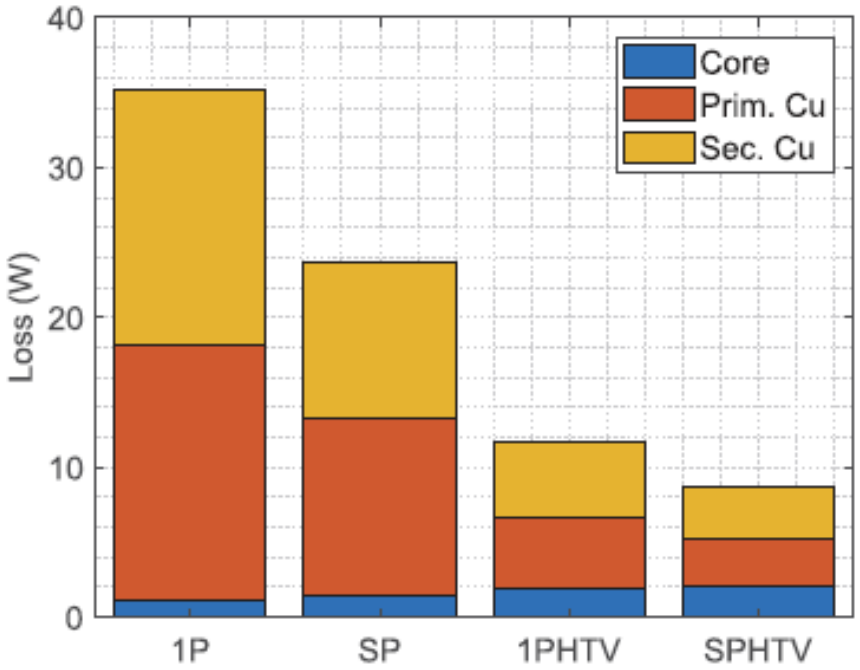


- **Propose iterative design procedure, including designing with good termination practices**

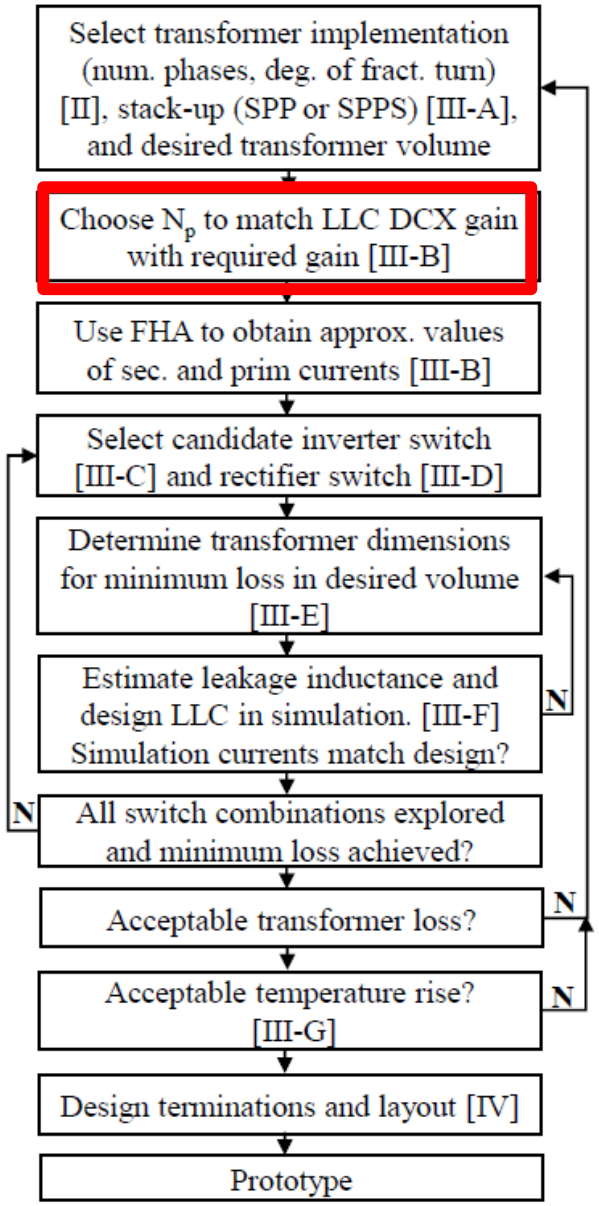
Building a High Performance SPHTV Prototype



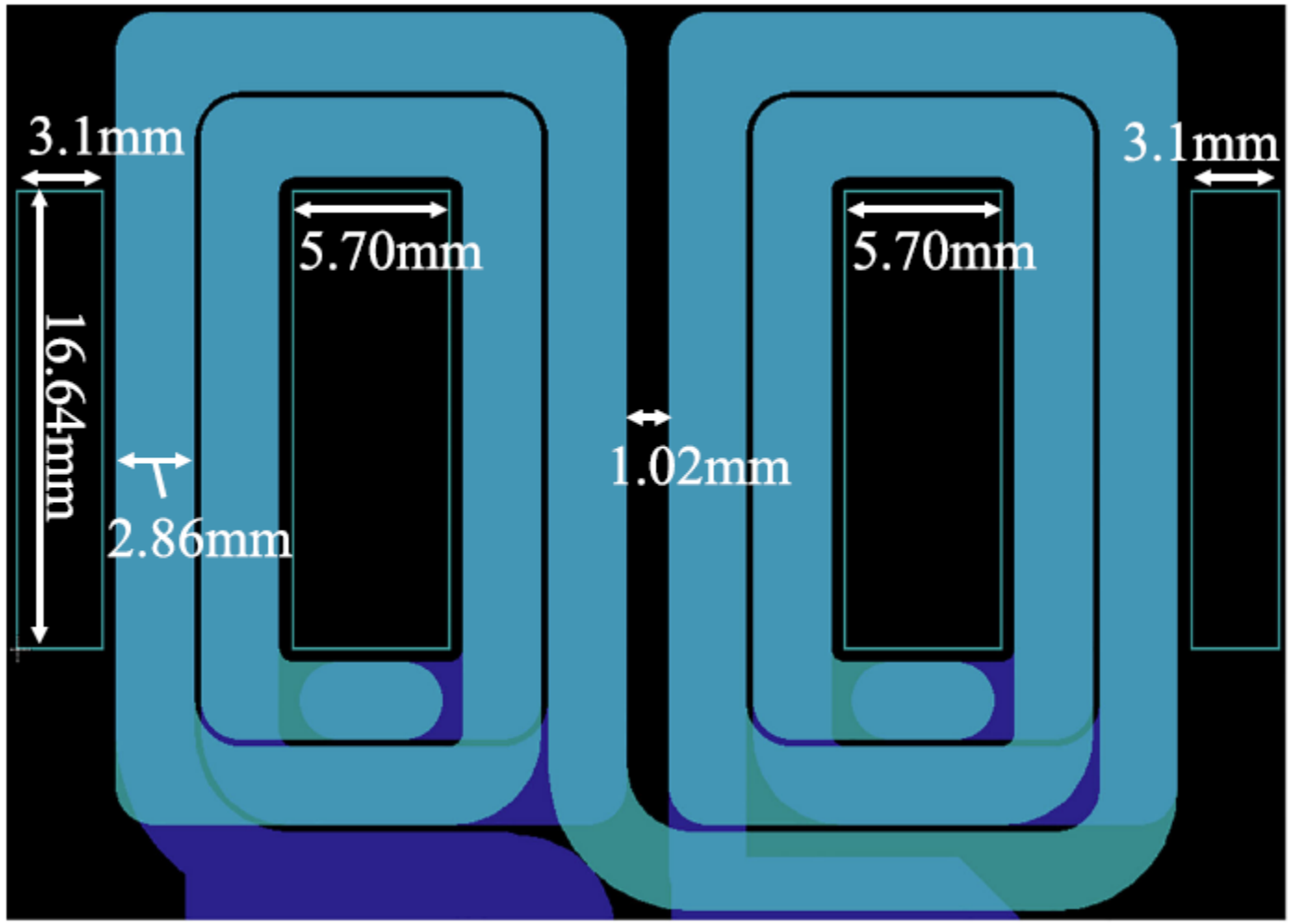
- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
  - SPPS achievable, but implementation is more complex



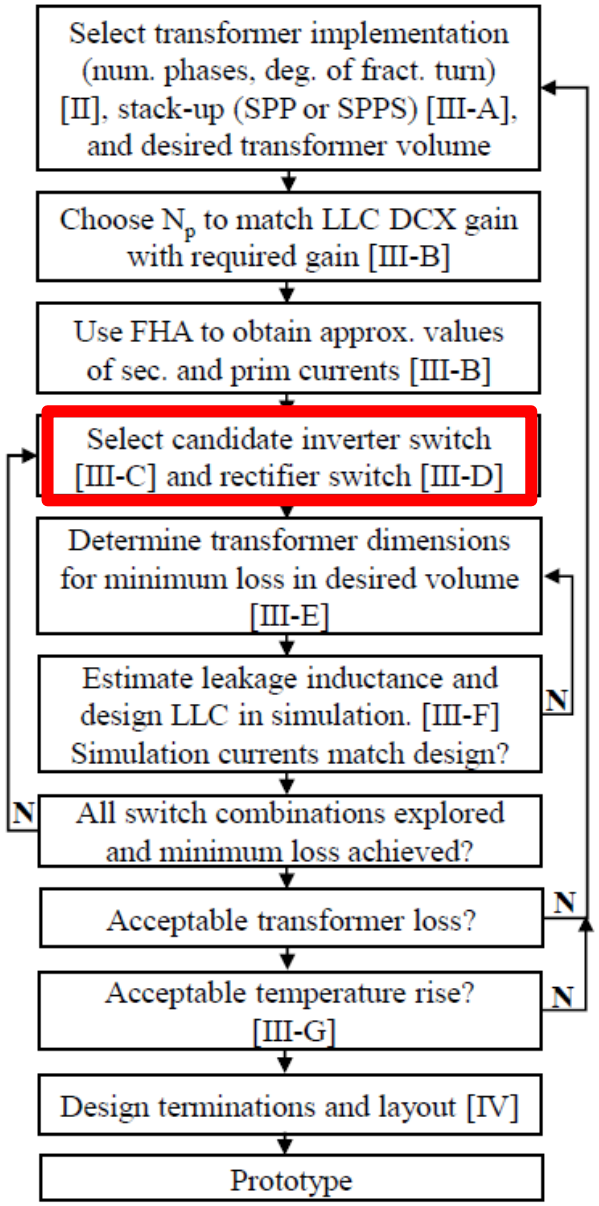
Building a High Performance SPHTV Prototype



- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns

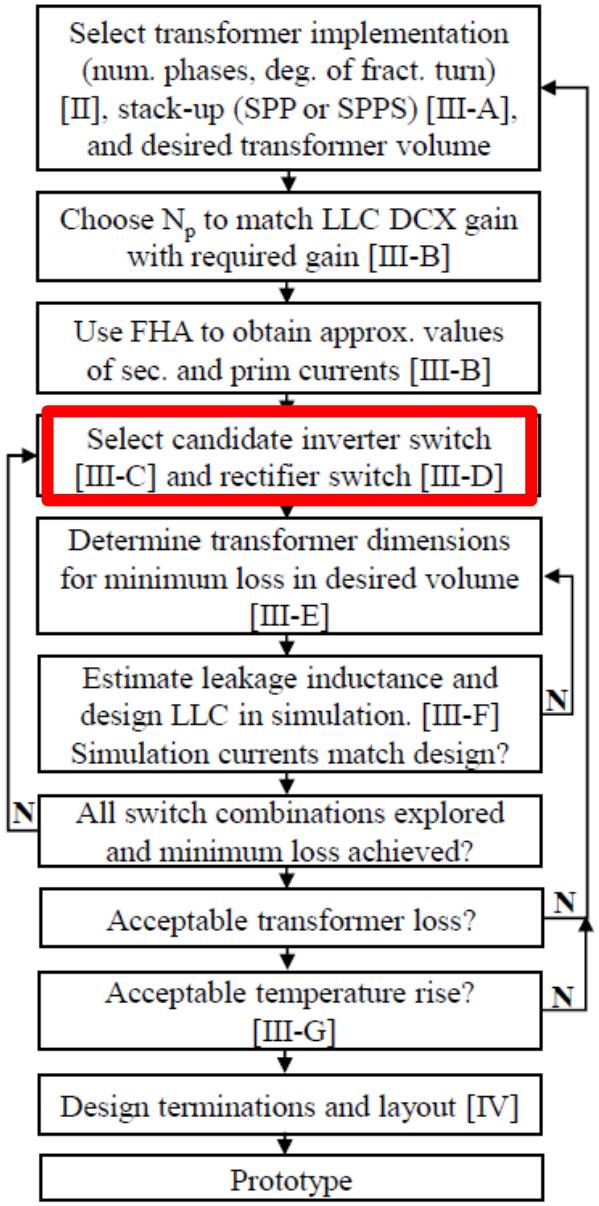


Building a High Performance SPHTV Prototype



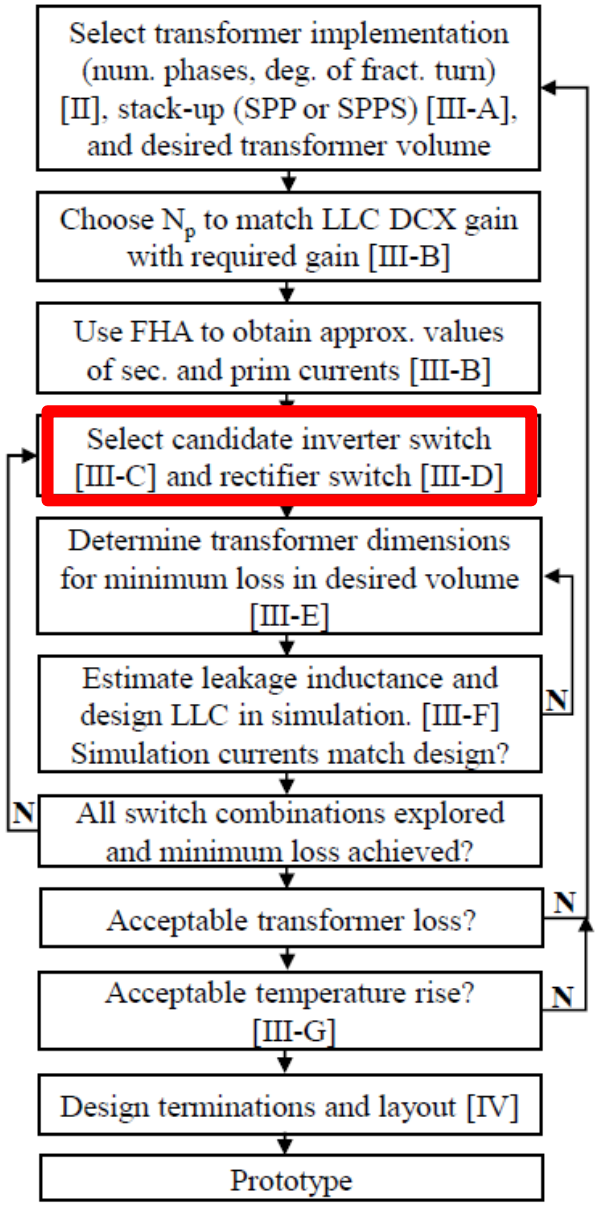
- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: Choose best $R_{on} * C_{oss}$ figure-of-merit, being mindful of:
  - GaN dynamic on-resistance
  - GaN C_{oss} losses
  - GS66516T 650V

Building a High Performance SPHTV Prototype



- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: Choose best $R_{on} * C_{oss}$ figure-of-merit, being mindful of:
  - GaN dynamic on-resistance
  - GaN C_{oss} losses
  - GS66516T 650V
- Rectifier: Choose best $R_{on} * Q_g$ FOM
  - C_{oss} less important due to high sec. currents
  - Silicon, 25V IQE006NE2LM5

Building a High Performance SPHTV Prototype



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- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: GS66516T
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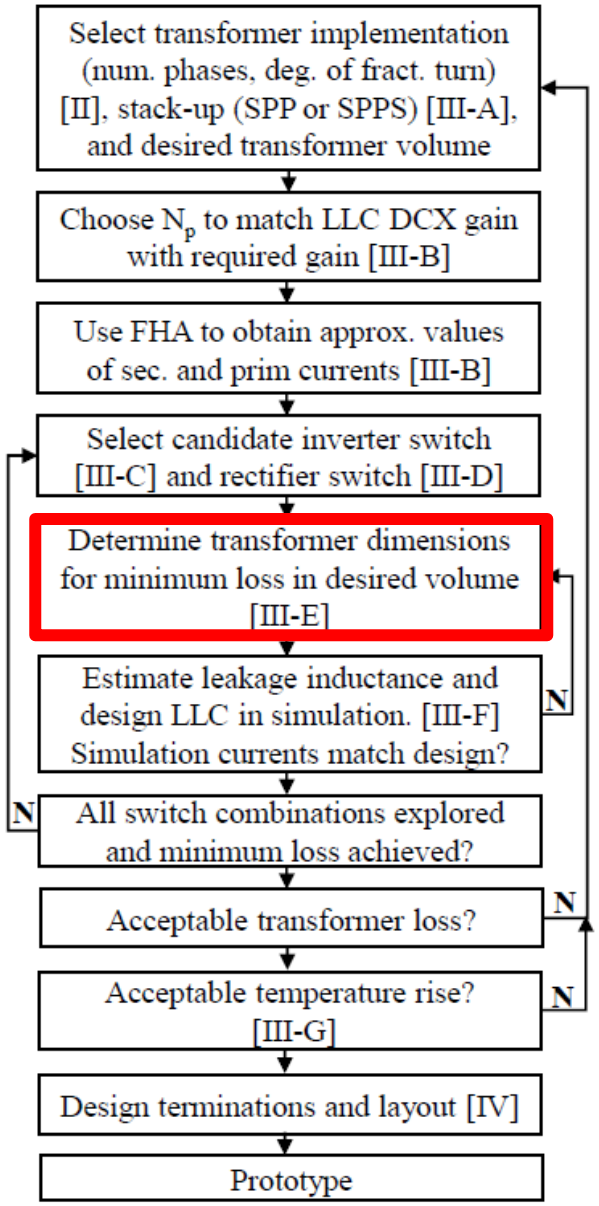
Building a High Performance SPHTV Prototype



- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: GS66516T
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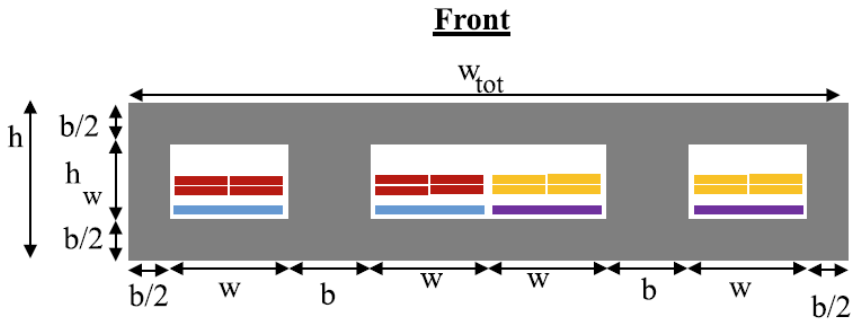
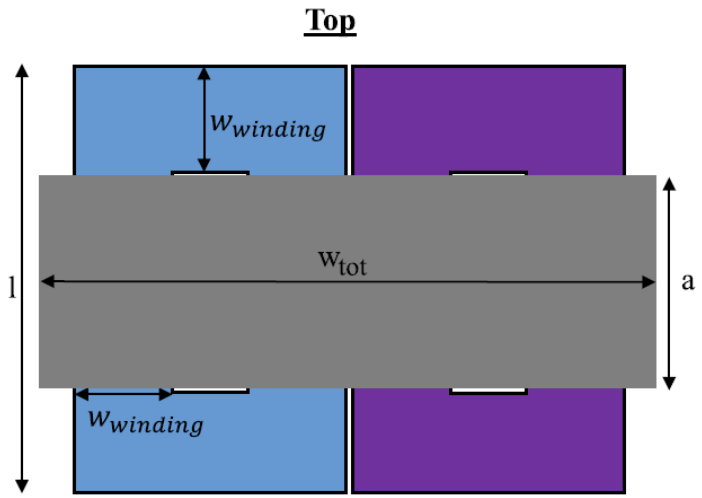
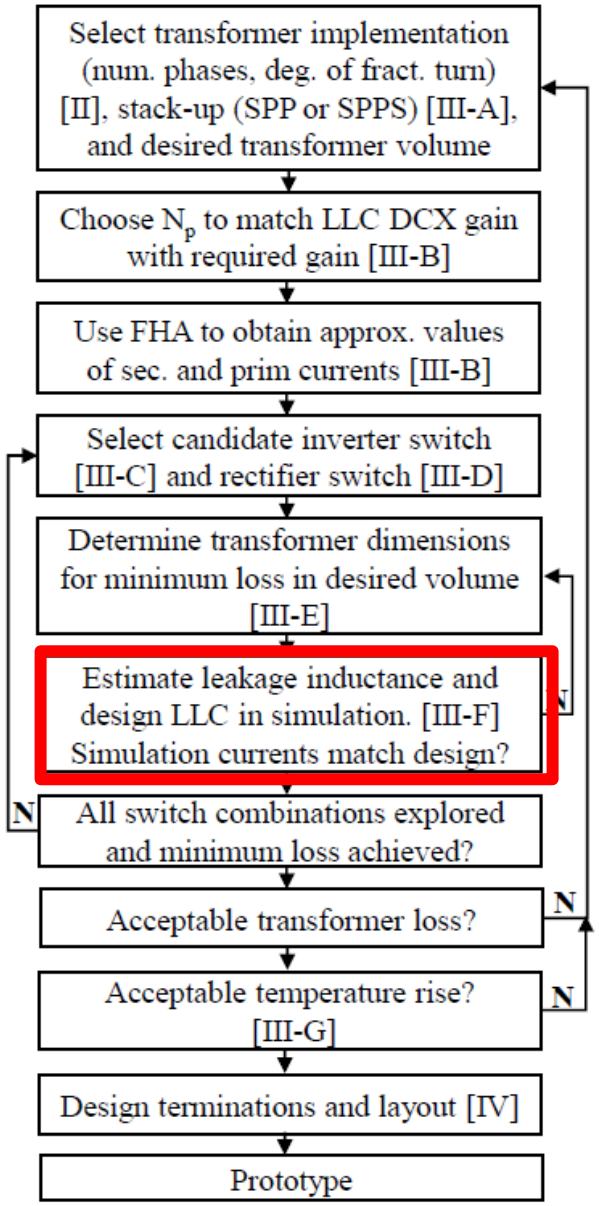




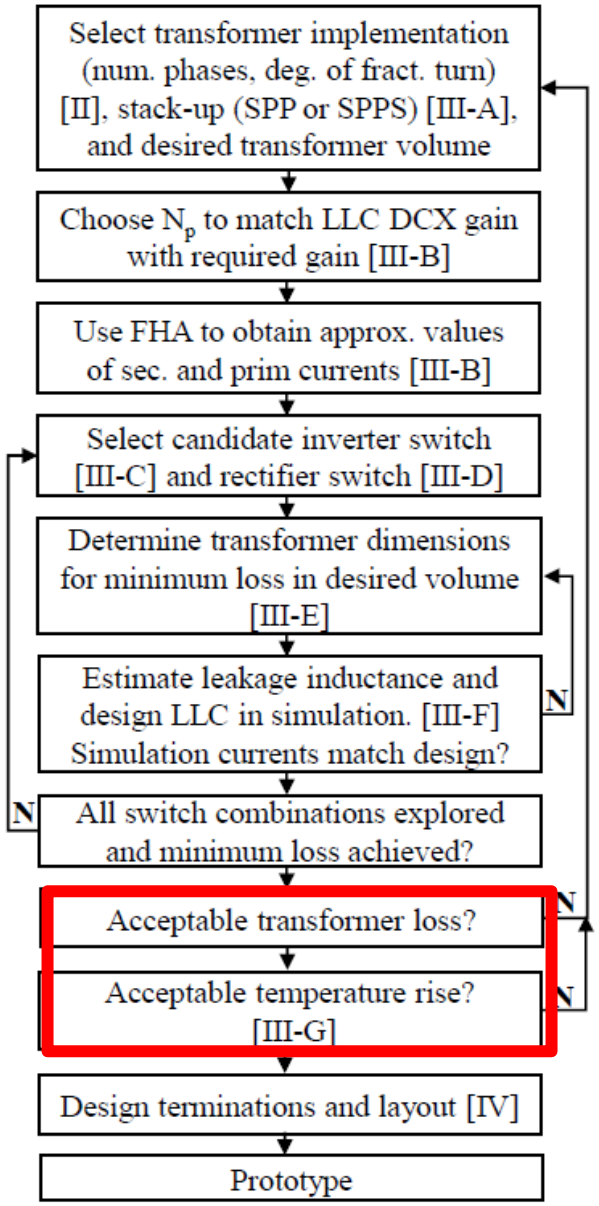
Building a High Performance SPHTV Prototype



- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: GS66516T
- Rectifier: IQE006NE2LM5

$$L_{\mathrm{lk}} \approx \frac{2\mu_o N_p^2}{(w)(\mathrm{MPL})}\left(s_{\mathrm{SP}} + \frac{s_{\mathrm{PP}}}{4}\right)$$

Building a High Performance SPHTV Prototype



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- Inverter: GS66516T
- Rectifier: IQE006NE2LM5

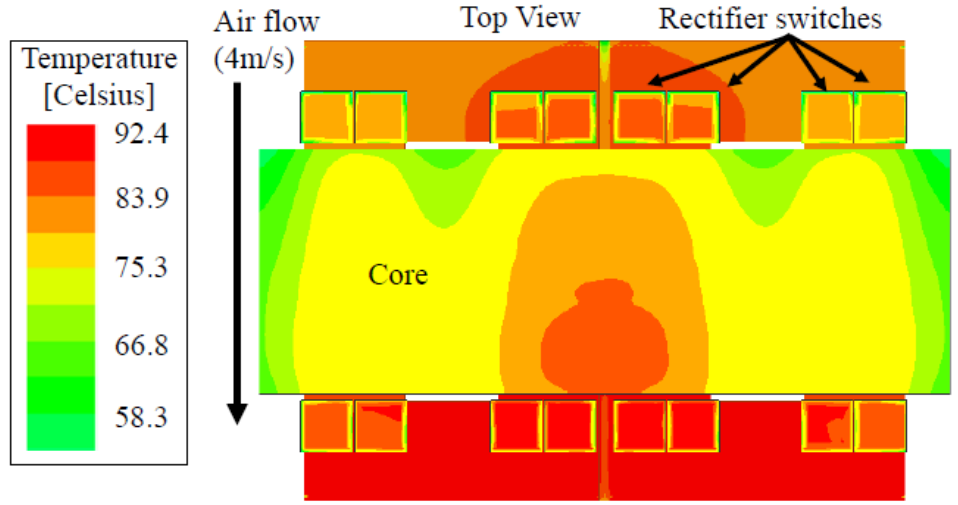
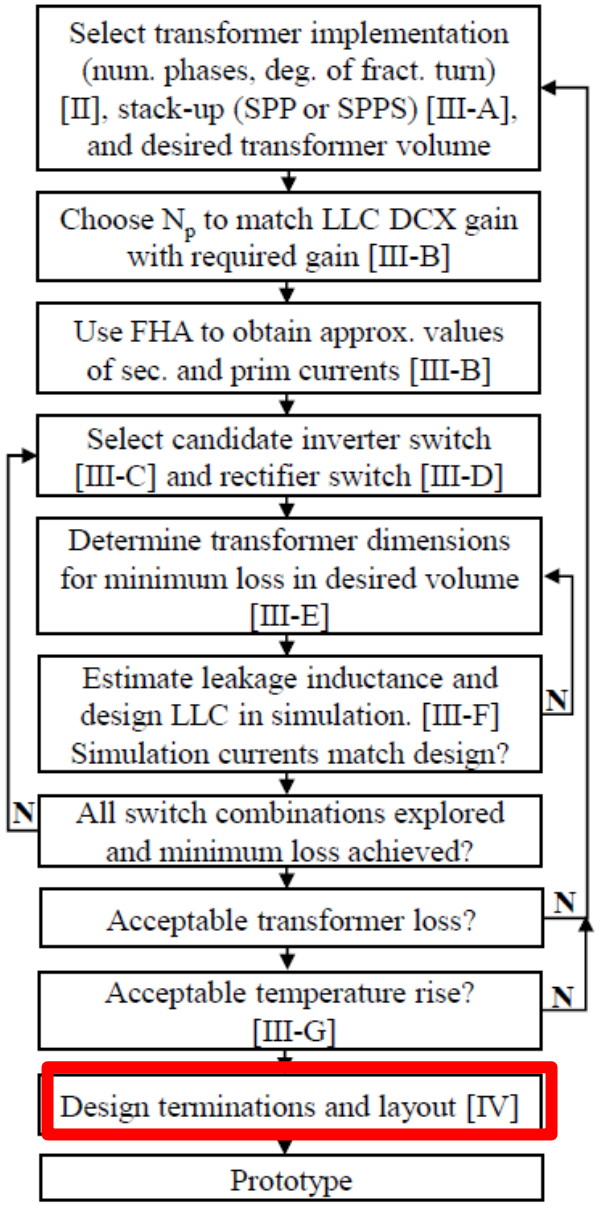
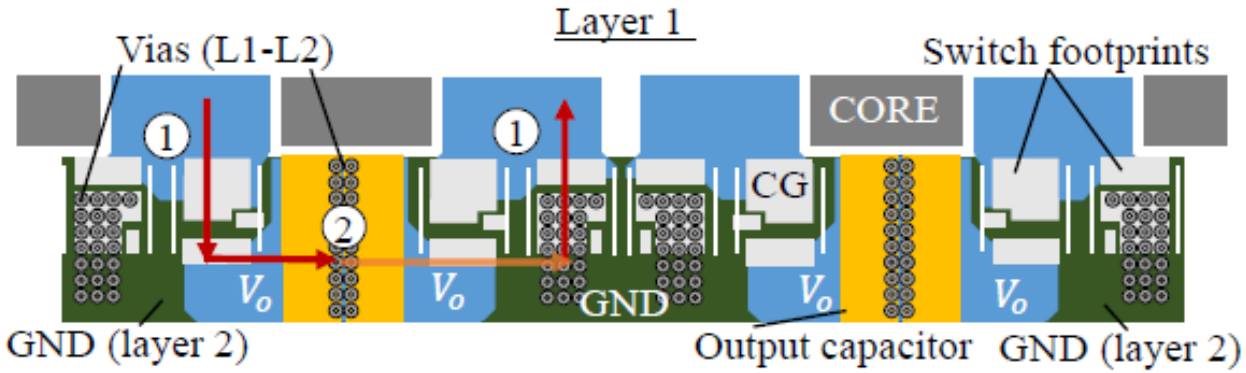


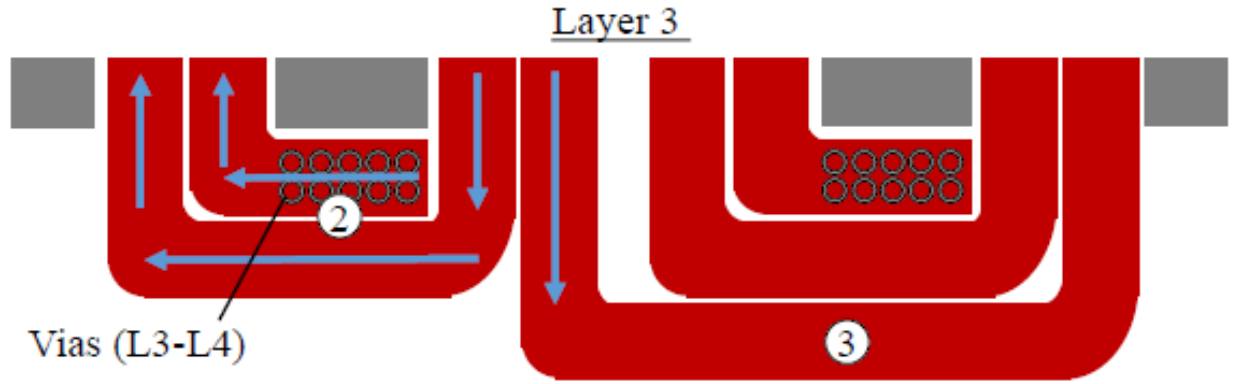
Fig. 7: ANSYS Icepak thermal simulation of the transformer.

Building a High Performance SPHTV Prototype

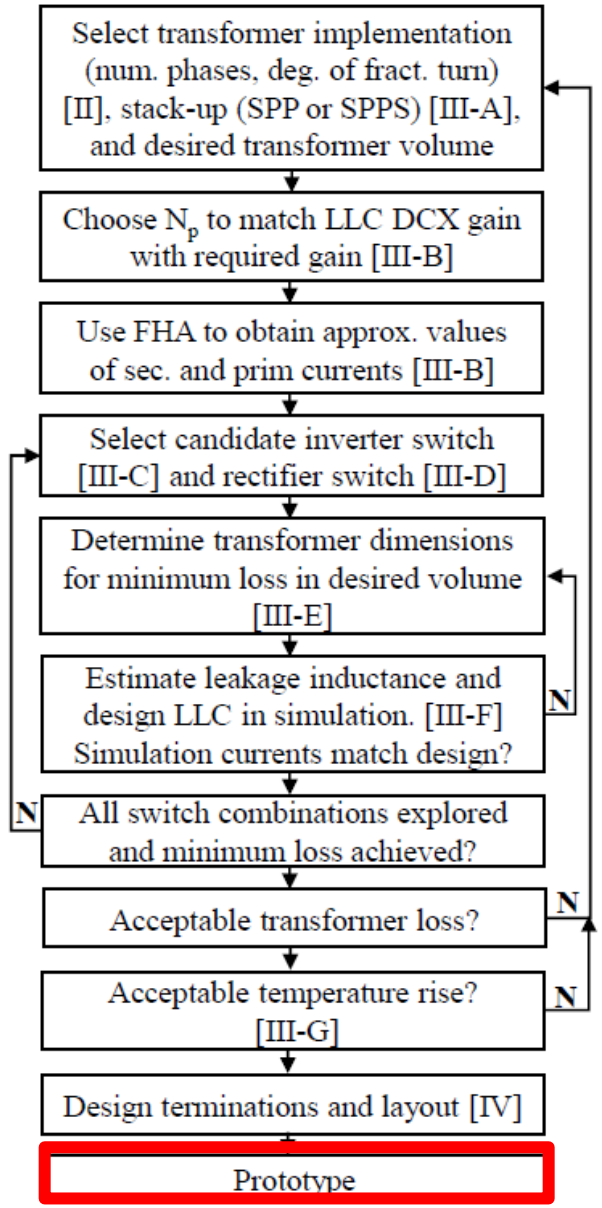


- SPHTV, SPP stack up, 3/2/3 oz copper, 12.5 cc
- 380 to 12V ⇒ 8:0.5 ⇒ 4 + 4 primary turns
- Inverter: GS66516T
- Rectifier: IQE006NE2LM5





Building a High Performance SPHTV Prototype



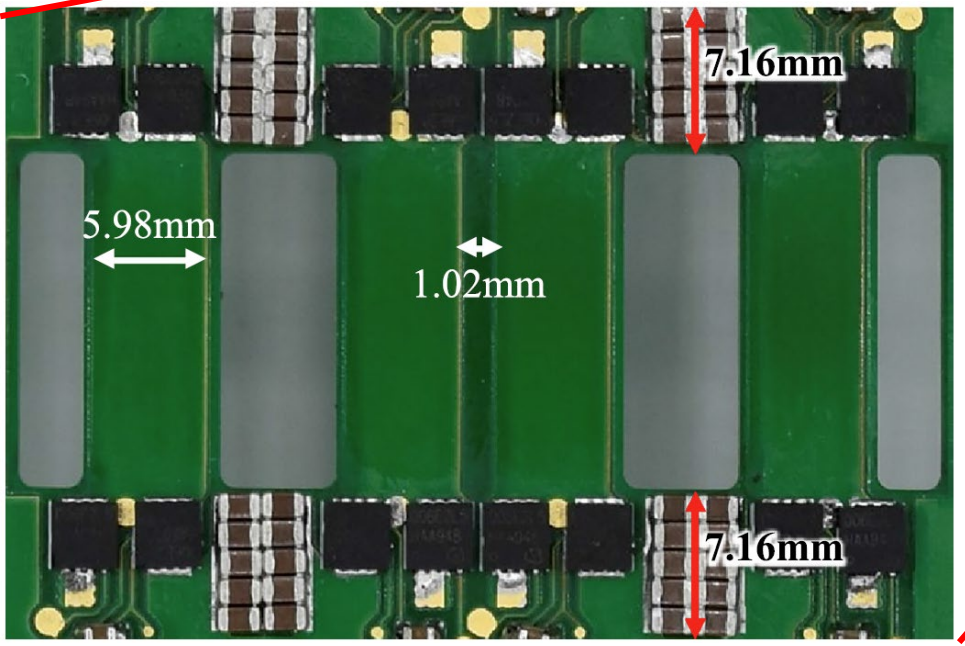
Planar Transformer	
Stack-up	Four layers; L1/L2/L3/L4 = 3/2/2/3 oz.
Winding arrangement	S/_/P/P (second layer unused)
N_p	Four turns; two turns each on L3 and L4, connected in series
Secondary winding	Four half-turns on L1
Layer spacing (approx. from manufacturer)	L1-L2: 0.22mm; L2-L3: 1mm; L3-L4: 0.22mm
Board height (h_{PCB})	1.68 mm
Core material	Hitachi Metals ML91S
Core-to-trace spacing	0.508mm
Trace-to-trace spacing	0.254mm
Core dimensions	a=16.13mm; b=5.16mm; w=7.53mm; h_w=4mm
Core height	9.23 mm
Transformer box volume	14.2 cm^3

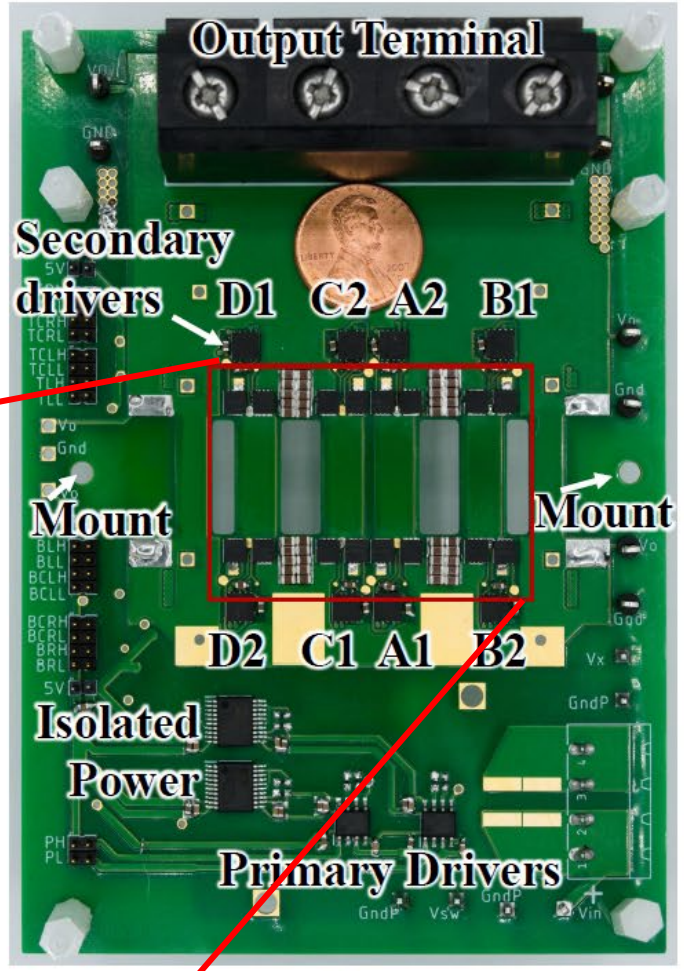
Inverter	
Inverter switches	GS66516T
Gate drivers	SI8271
Isolated power	ADUM5010
Rectifier	
Rectifier switches	IQE006NE2LM5 and IQE006NE2LM5CG
Gate drivers	LM5113QDPRRQ1
Output capacitors	$C_o \approx 144\mu$F; 40x C2012X7S1E106K125AC; 5 pcs. per half-bridge. 10μF nominal, de-rated to $\approx$3.6μF ea. at 12Vdc, 100°C [33]
LLC	
Resonant capacitor	47.22nF; 1x 47nF/630V/1812/C0G + 0.22nF/2kV/C0G
Resonant inductor	520 nH; derived from transformer leakage
Magnetizing inductor	15.3 μH; g_1= 0.127mm, g_2=0.318mm
Other	
Controller	TMS320F28379D
Cooling	Nidec FAN-0100L4, 40mm Axial Fan, 40x40x28mm, 8500RPM

SPHTV Prototype

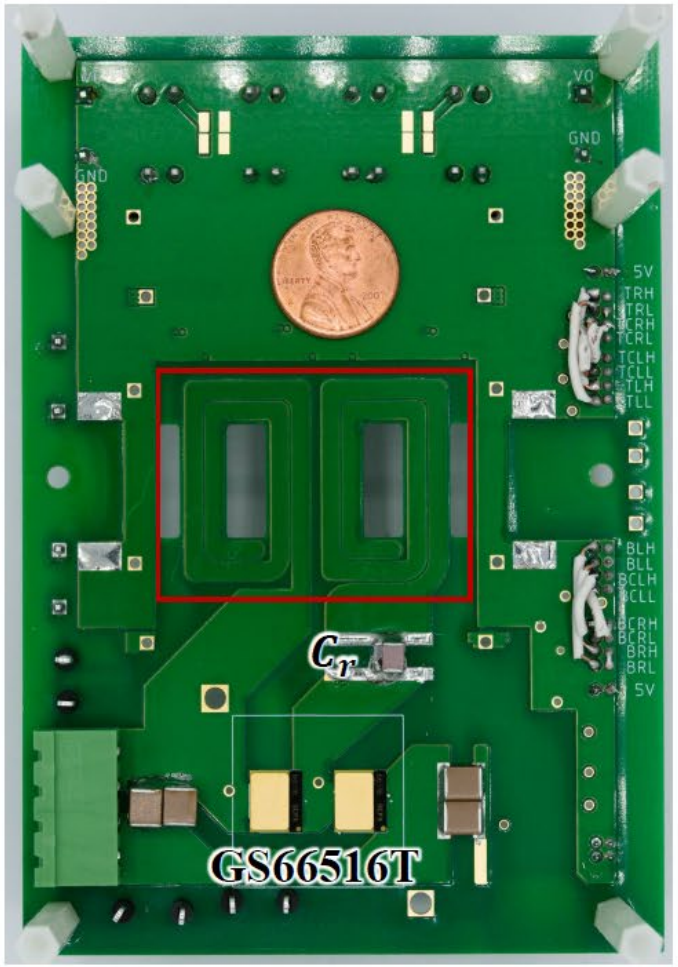
Custom core from Hitachi Metals

(a)





(c)



(d)

- 4 layer, non-interleaved SPP, 3/2/3oz

Losses and Thermal Performance Well Predicted

Losses fit expectation

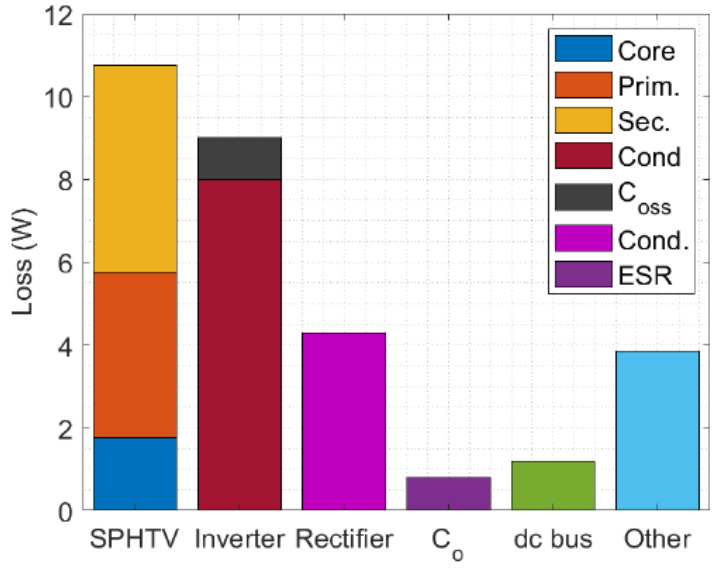


Fig. 12: Estimated loss breakdown at full load, not including hotel power (2.7W) and fan power (1.44W).

Thermal performance

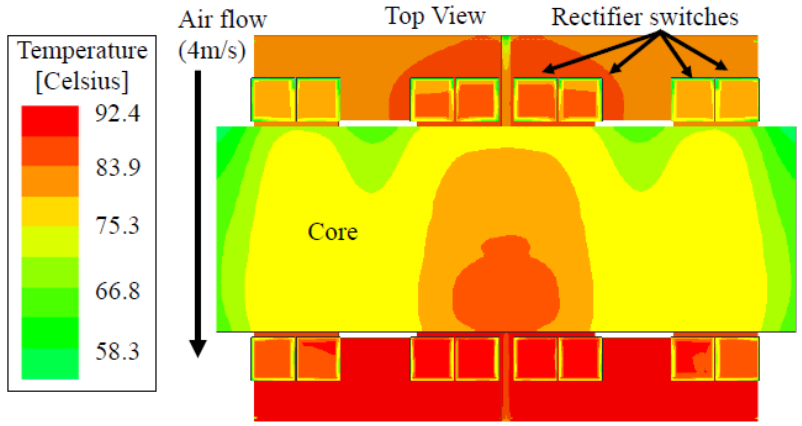


Fig. 7: ANSYS Icepak thermal simulation of the transformer.

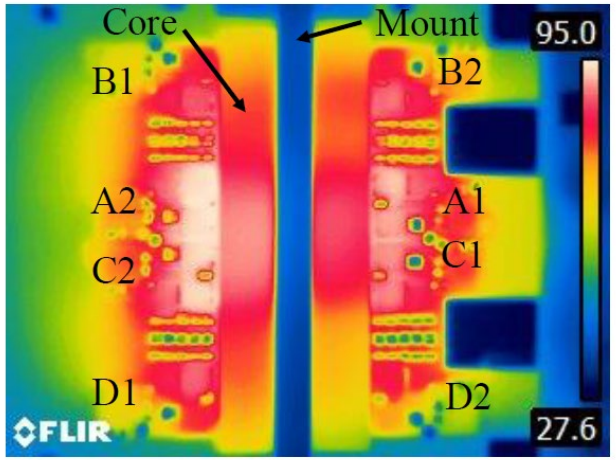
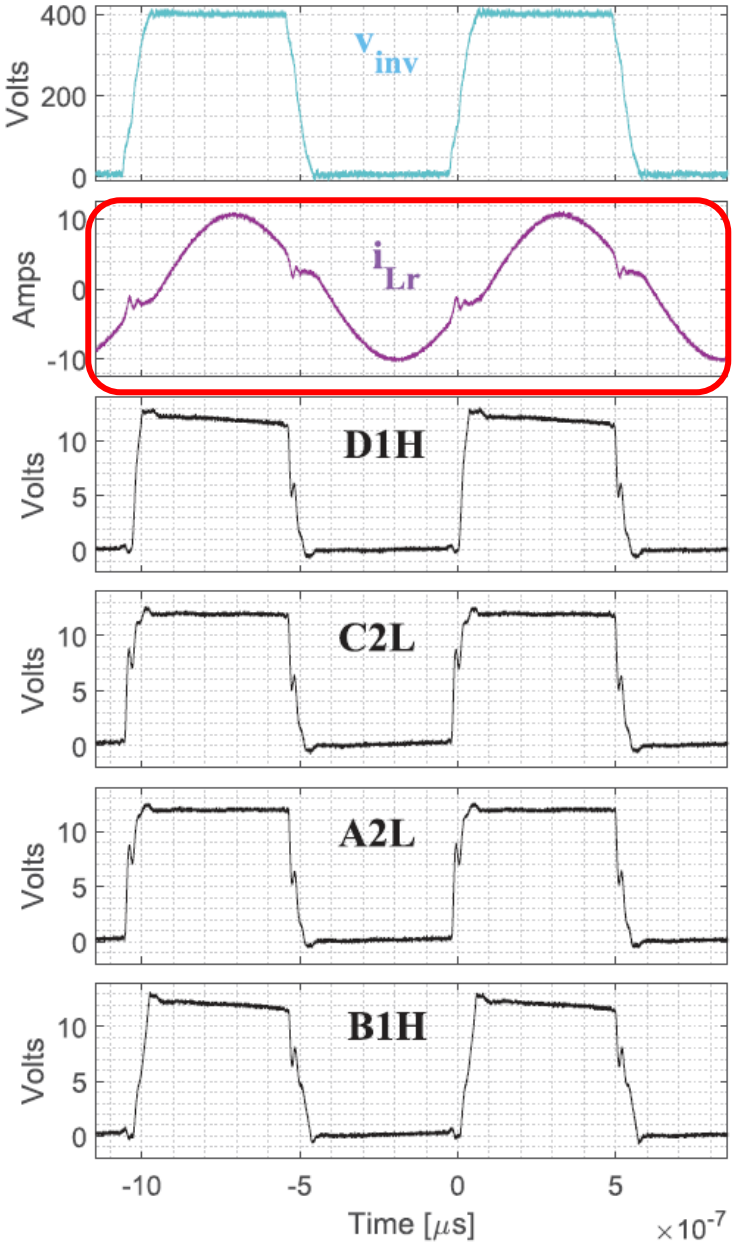


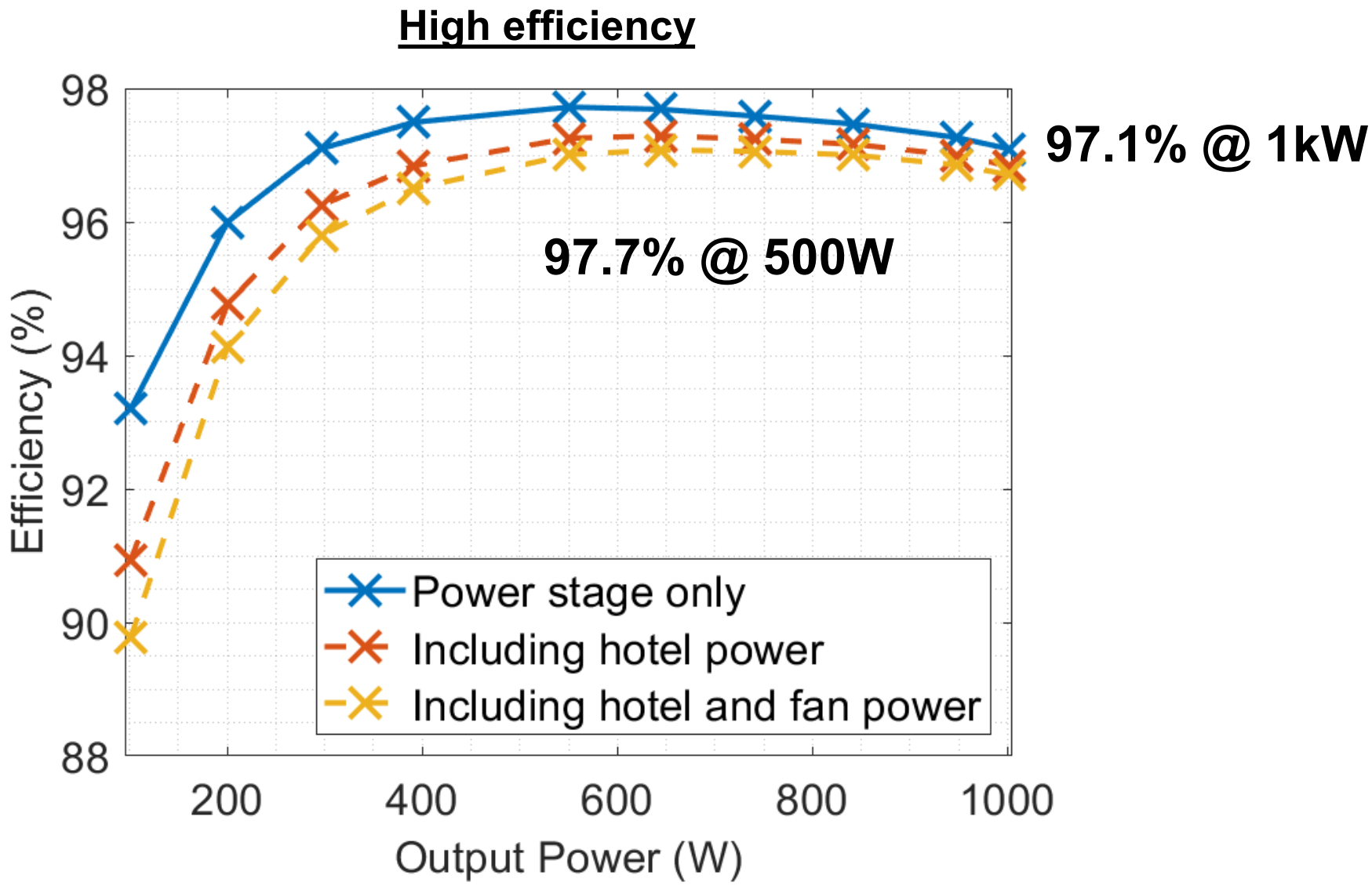
Fig. 11: Thermal image of secondary-side under full-load (obtained after 15 minutes of continuous operation, 22°C room temperature). The fan is located to the right of the PCB.

Example Operating Waveforms

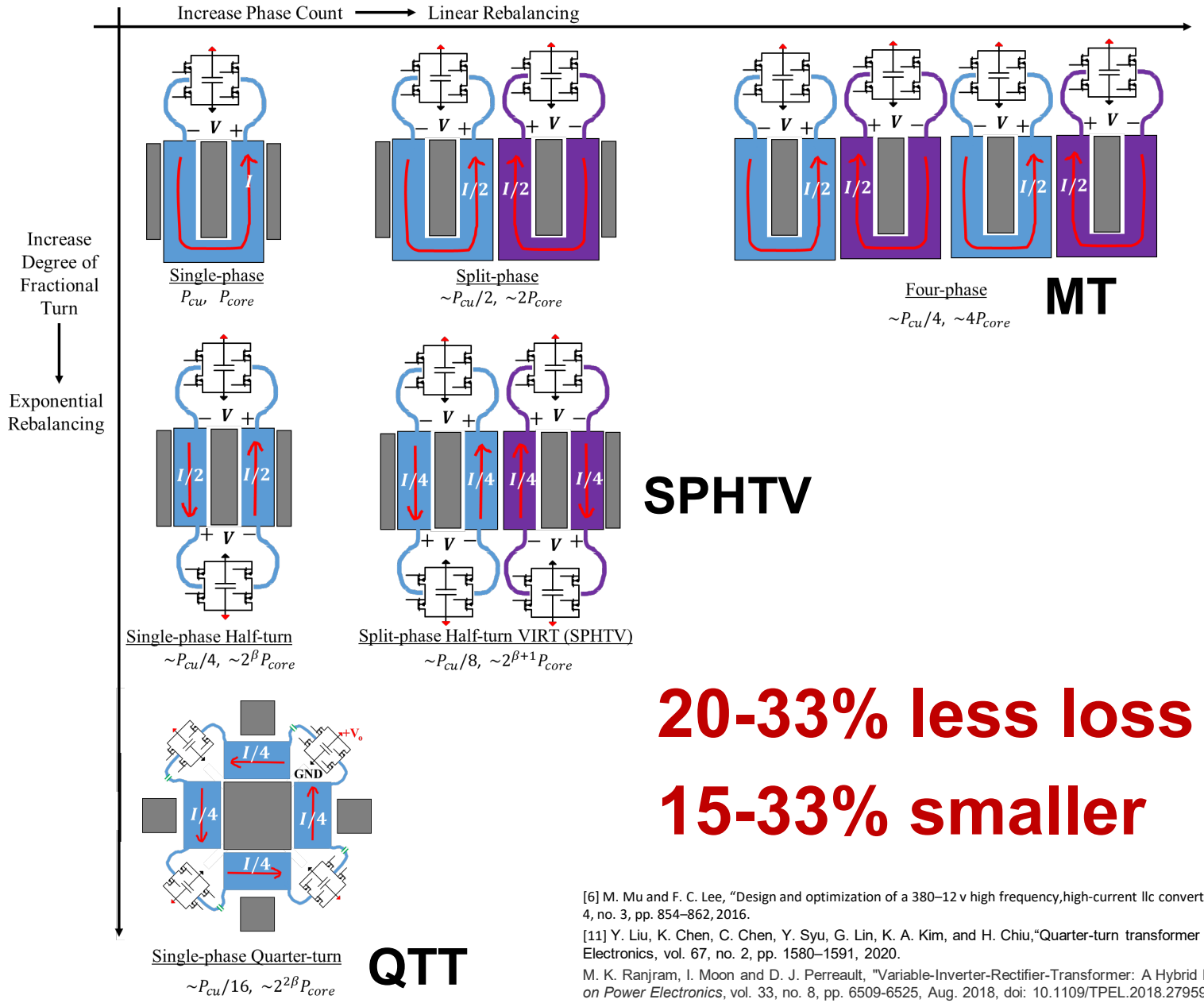


- Inverter ZVS achieved
- All half-bridges are operated identically, experience slightly different deadtime transitions owing to local decoupling loops
- Near-resonant current in primary tank

Prototype is Extremely Efficient



SPHTV: Much Lower Loss and Much Smaller than Best Alternatives



380-12V, 1kW

	This work	MT [6]	QTT [11]
Stack-up	S/_/P/P	S/P/P/S	S/G/P/P/G/S[a]
Peak power stage efficiency	97.7%	-	97.0%
Peak efficiency including hotel power	97.3%	97.1%	-
Full load loss (power stage only) [W]	29.9	34.4	41
Transformer loss at full load [W]	10.8	16.3	13.2
Transformer footprint [mm^2]	1536	2200	2500
Height [mm]	9.23	7.3	8.9
Transformer box volume [cm^3]	14.2	16.1	22.3

[a] 'G' is a secondary layer tied directly to secondary ground

20-33% less loss

15-33% smaller

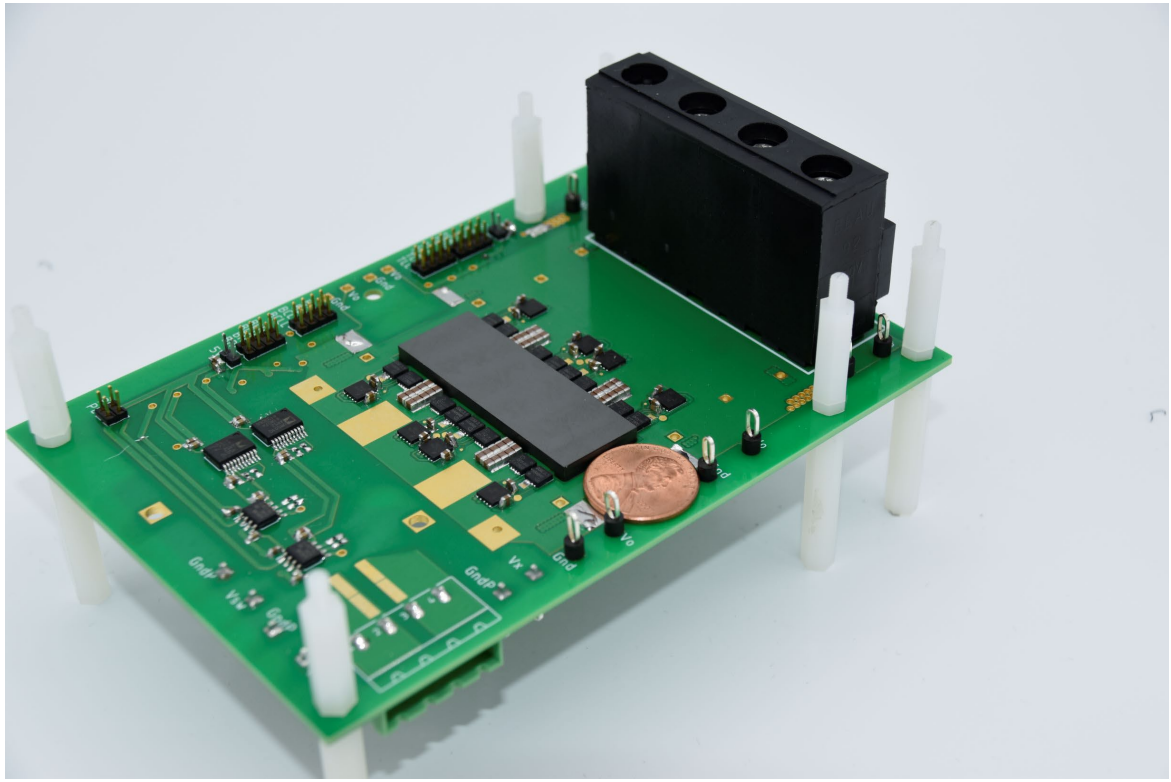
[6] M. Mu and F. C. Lee, "Design and optimization of a 380–12 v high frequency,high-current llc converter with gan devices and planar matrix transformers," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 854–862, 2016.

[11] Y. Liu, K. Chen, C. Chen, Y. Syu, G. Lin, K. A. Kim, and H. Chiu,"Quarter-turn transformer design and optimization for high power density 1-mhz llc resonant converter," IEEE Transactions on Industrial Electronics, vol. 67, no. 2, pp. 1580–1591, 2020.

M. K. Ranjram, I. Moon and D. J. Perreault, "Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure Enabling Adjustable High Step-Down Conversion Ratios," in *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6509-6525, Aug. 2018, doi: 10.1109/TPEL.2018.2795959.

Summary of the Half-Turn VIRT

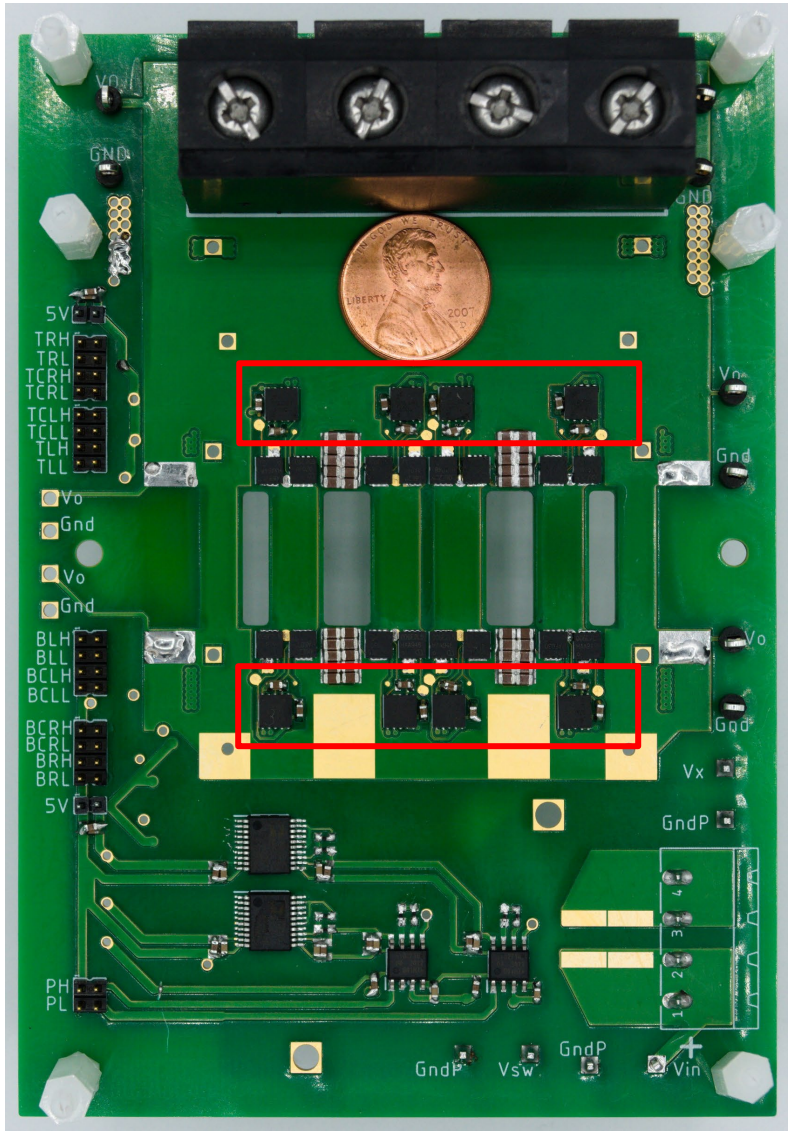
- Coupled Electronic and Magnetic System (CEMS) paradigm enables the VIRT concept
- Fractional and variable turns ratios unachievable in conventional design
- Used to build much smaller and much more efficient datacenter supply



Additional Implementation Details

1. Can reduce the number of secondary gate drivers

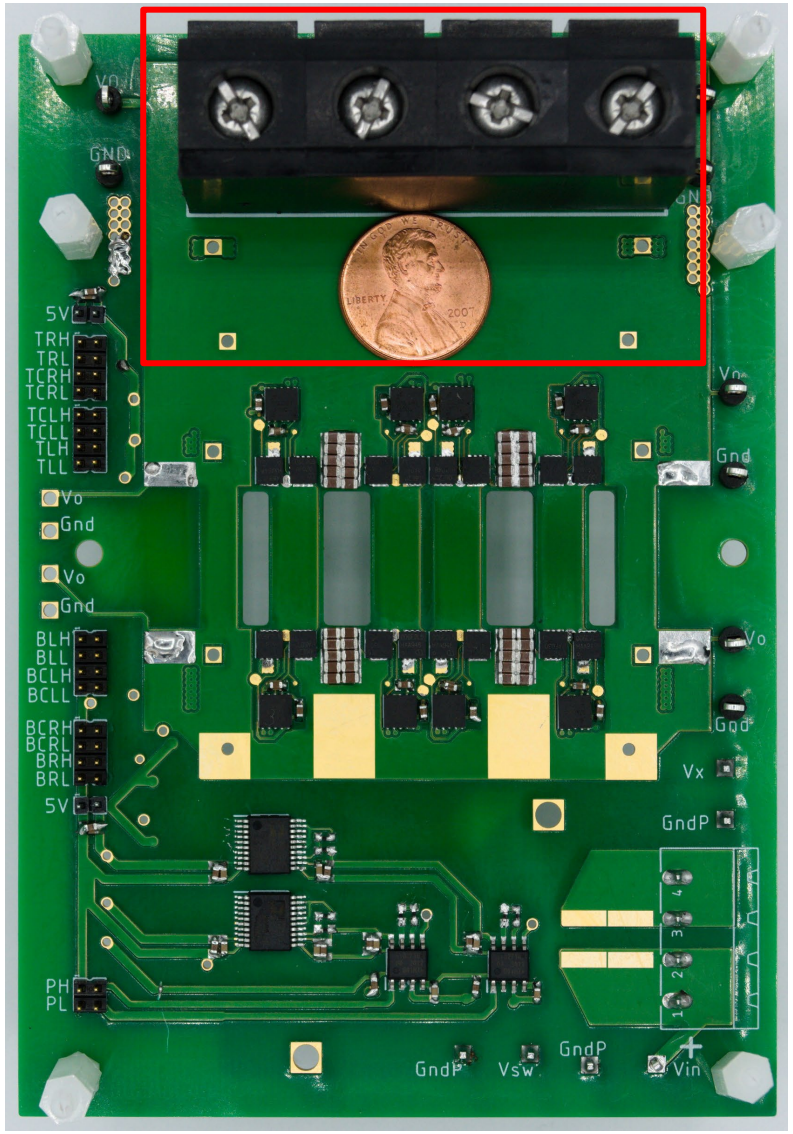
Used for prototype convenience, but same gating signal sent to each switch.



Additional Implementation Details

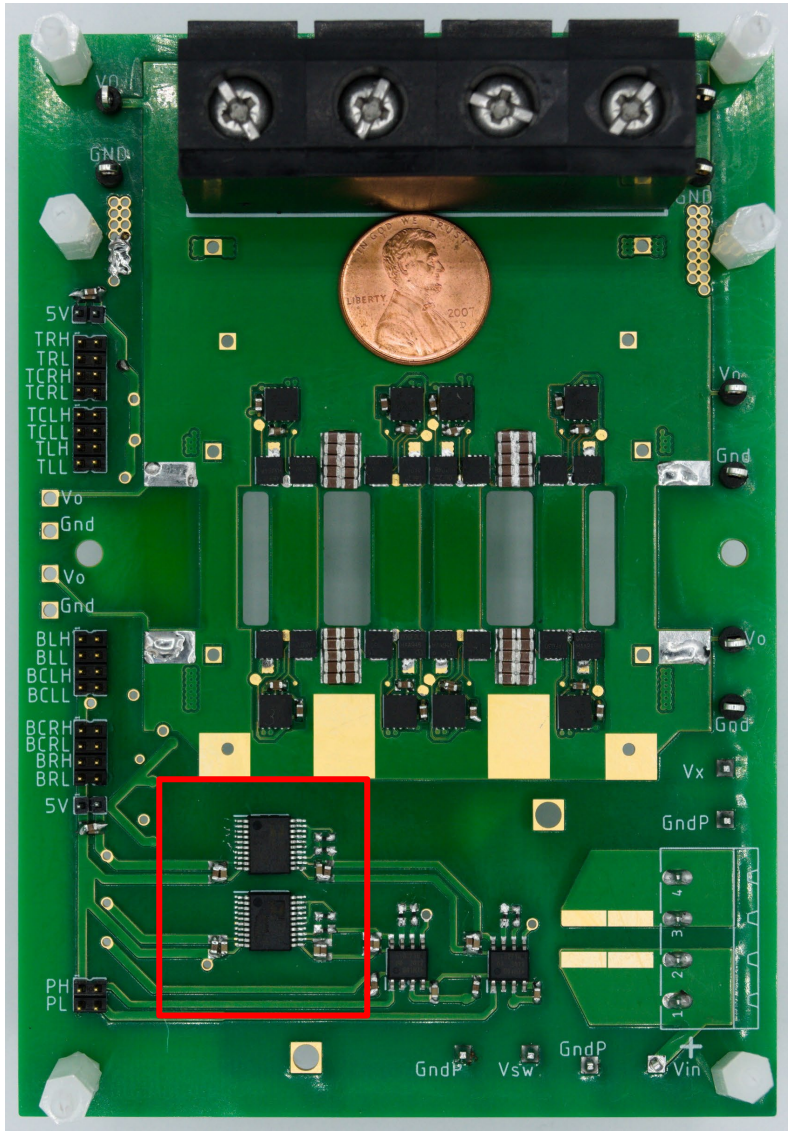
2. **Single dc output terminal used**

In practice, distribute dc output. Room also included in prototype for additional heat-sinking, but proved unnecessary.



Additional Implementation Details

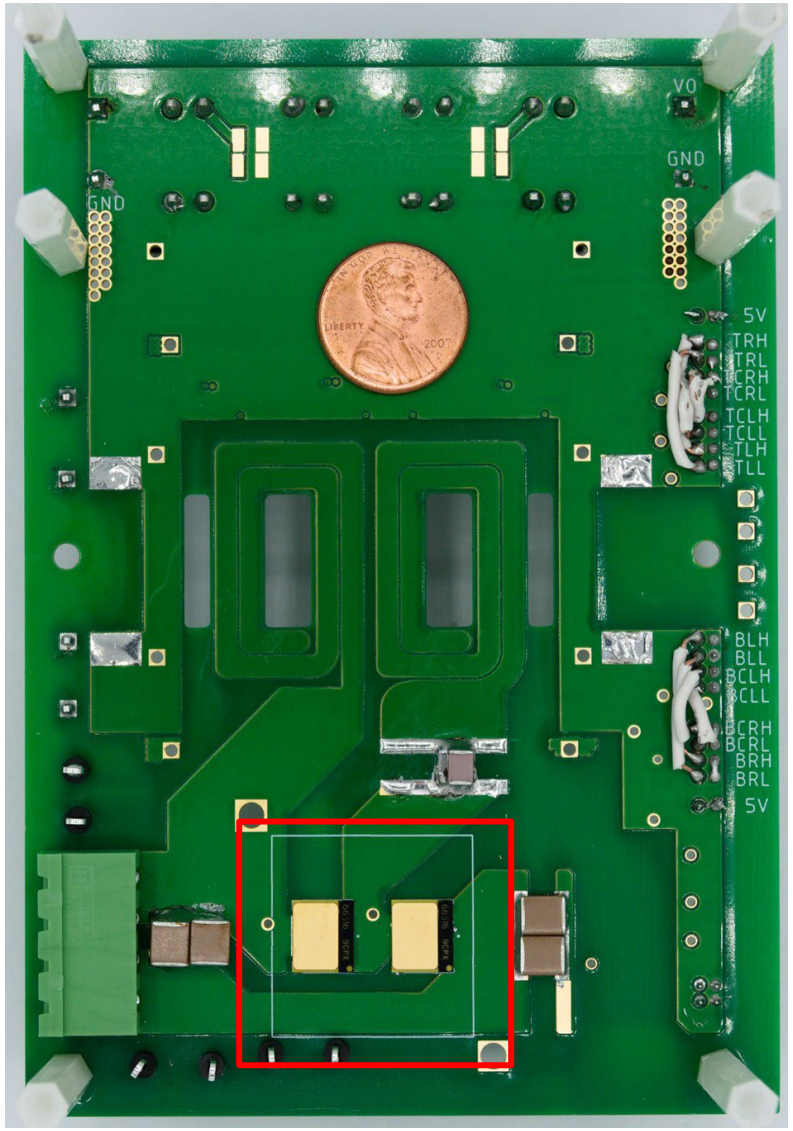
3. Isolated power supplies to power inverter from the secondary-referred hotel power. Loss (~0.45W) included in efficiency estimate



Additional Implementation Details

4. **Space conservatively included for inverter heat sink.**

Footprint can be dramatically reduced.



Additional Implementation Details

5. Acrylic core mount used for convenience to fix gap lengths during prototyping.

In practice, these would be made permanent when mounting to board.