SiC Power Device Reliability Presented at APEC 2019

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March 20, 2019

SiC Commercial Market

- Revenue > $250M worldwide in 2017
- Available market ~ $5B in 2022
- Trillions of fielded device hours to date
- Commercially released Schottky diodes, MOSFETs, and power modules
- Thousands of customers servicing many major markets
- Broad product portfolio
  - Voltage and current ratings
  - Package types
  - Die sizes

Advantages of SiC

- Wide bandgap -> high voltage capability: >10 kV
- Low switching losses

SiC Device Reliability: Excellent and Continually Improving

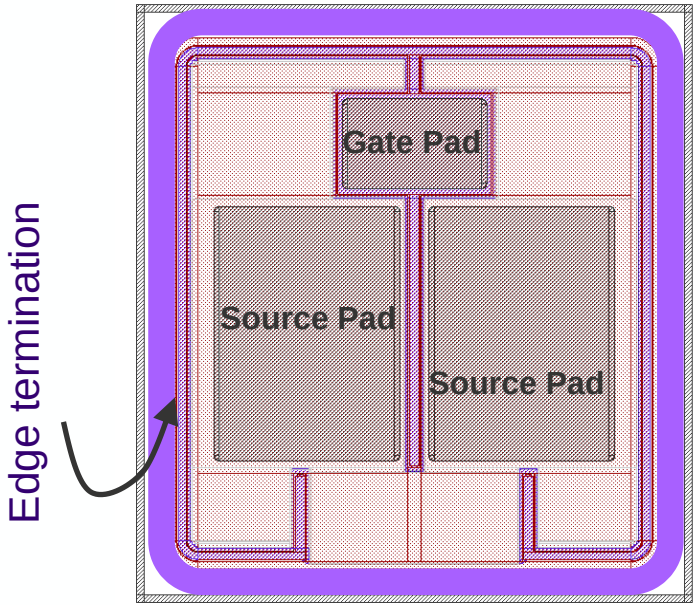
- Substrate quality
- Epitaxial growth
- Wafer processing

SiC Device Reliability Features Needed for Typical Applications

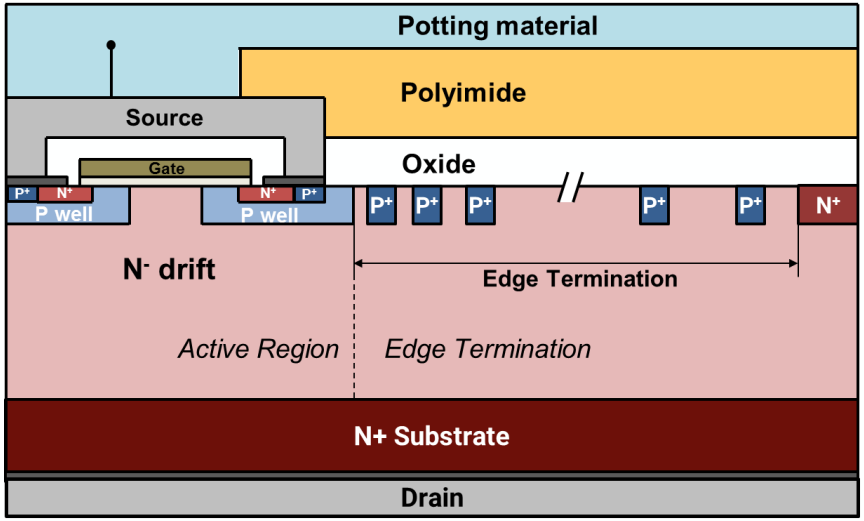
- Blocking voltage
- Gate oxide electric field
- Humid environments
- Threshold voltage stability
- On-resistance stability (3rd quadrant operation)
- Terrestrial neutron irradiation (high altitudes)

Device salient features and potential failure mechanisms

SiC MOSFET Salient Features / Critical Components



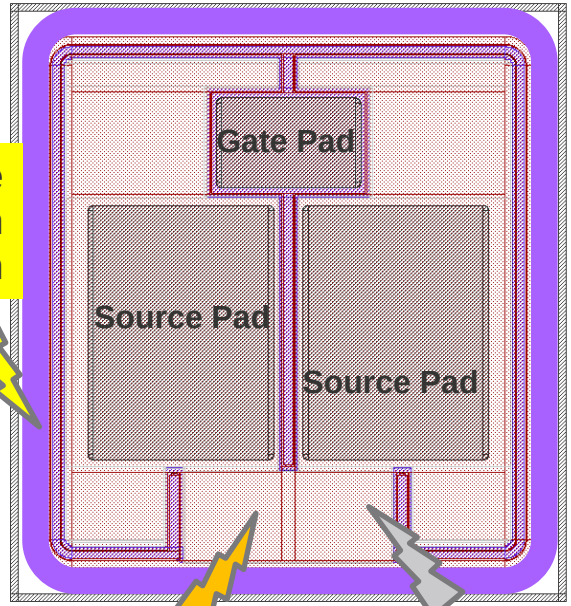
Drain is the backside of the chip



Schematic by E. VanBrunt et al., ECSCRM 2018

- SiC epitaxial layer: defects, thickness, doping
- MOS channel: Inversion-layer mobility, gate dielectric
- Edge termination
- Implantation / doping
- Ohmic contacts

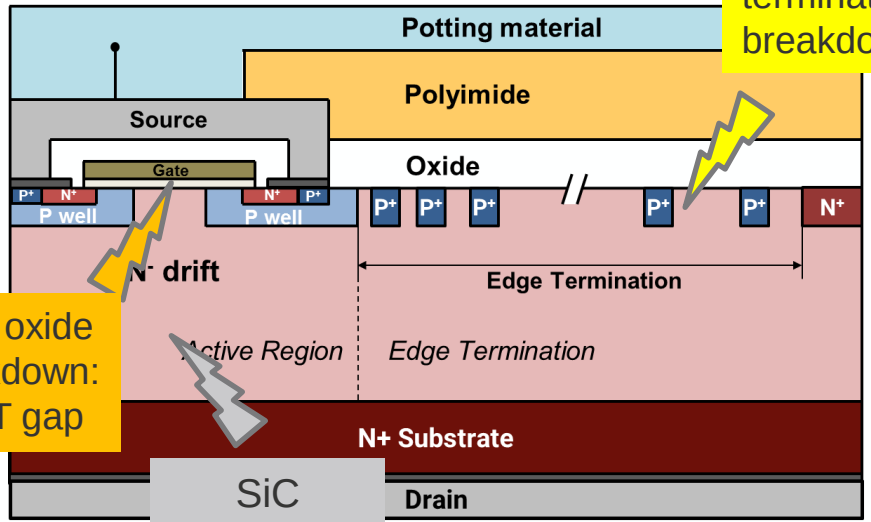
Blocking Voltage Potential Failure Mechanisms



Edge termination breakdown

Gate oxide breakdown

SiC breakdown



Edge termination breakdown

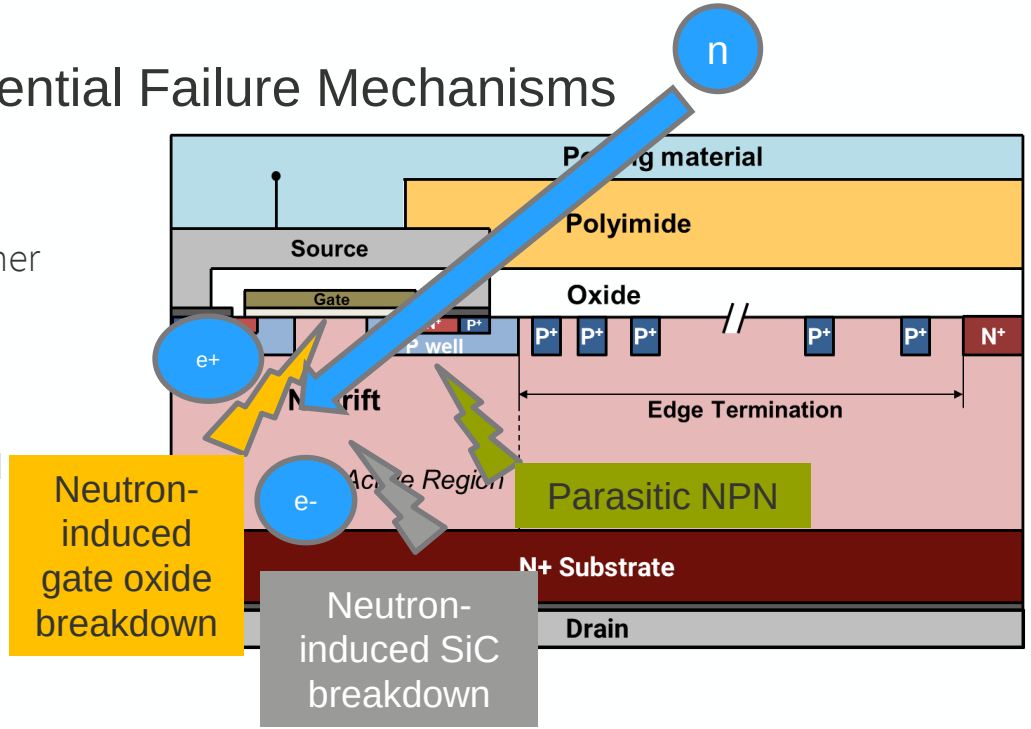
Gate oxide breakdown: JFET gap

SiC breakdown

Reliability stresses: HTRB, ALT-HTRB

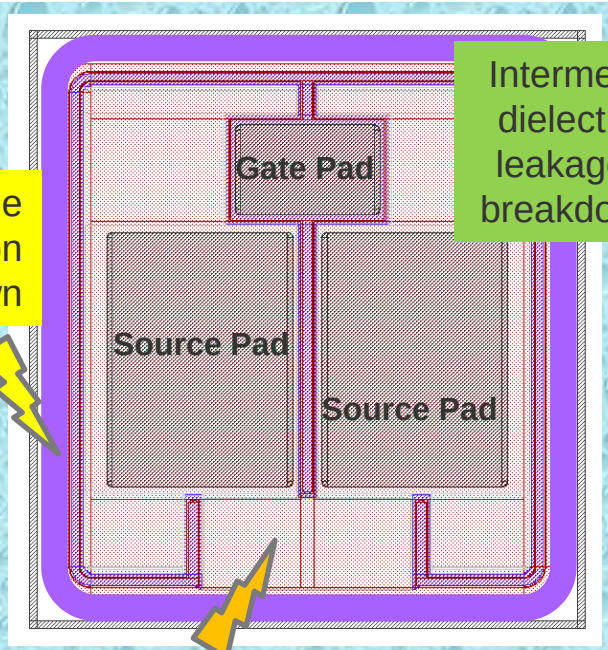
Terrestrial Neutrons Potential Failure Mechanisms

- Neutrons are attenuated by atmospheric gases, so there are more neutrons at higher elevations
- Neutrons collide with lattice atoms ->
  - Atoms recoil and/or
  - Protons and/or neutrons can be emitted
- Charge spikes along these trajectories
- Ionization trails ~ micrometers long: comparable to epilayer thickness
- Current transients
  - Parasitic bipolar turn-on -> burn-out
  - Charge accumulation -> gate oxide failure



Reliability stress: Neutron-irradiated HTRB

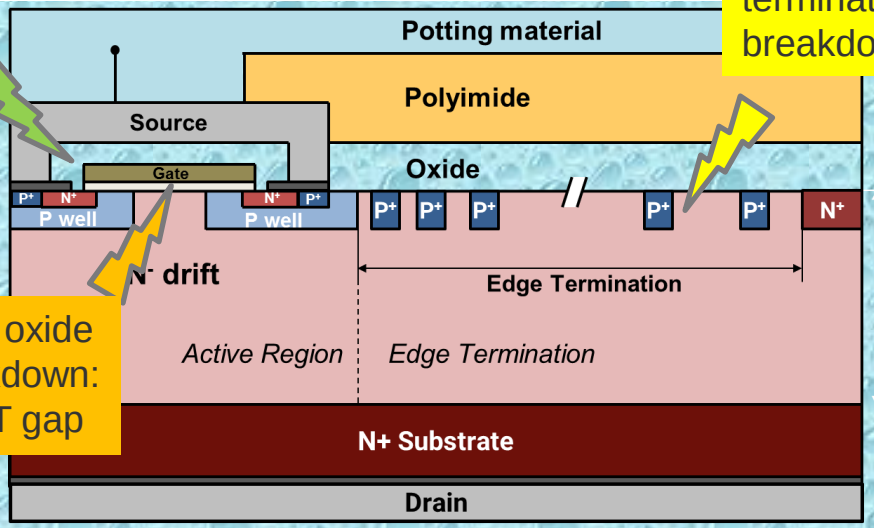
Humidity + Blocking Voltage Potential Failure Mechanisms



Edge termination breakdown

Intermetal dielectric leakage / breakdown

Gate oxide breakdown

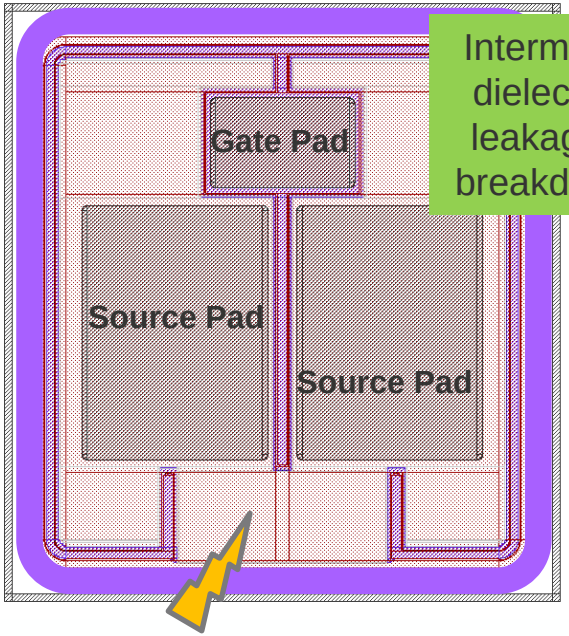


Edge termination breakdown

Gate oxide breakdown: JFET gap

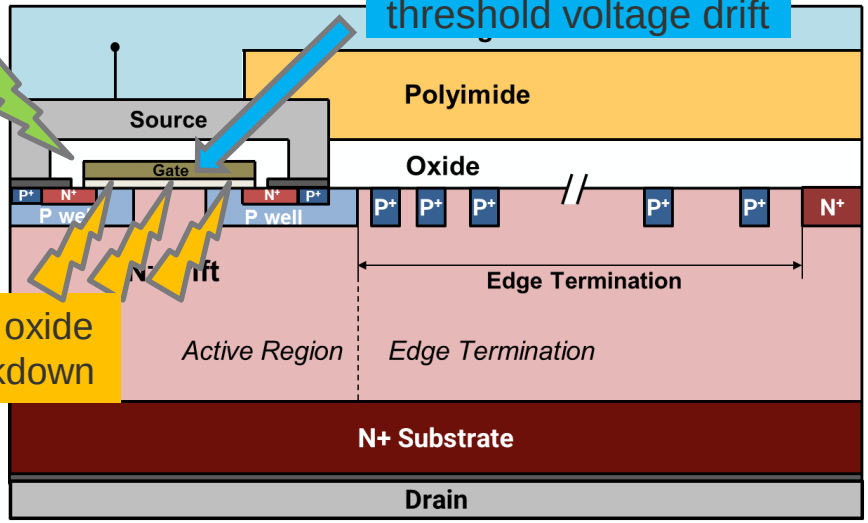
Reliability stress: THB

Gate Voltage Potential Failure Mechanisms



Intermetal dielectric leakage / breakdown

Gate oxide breakdown

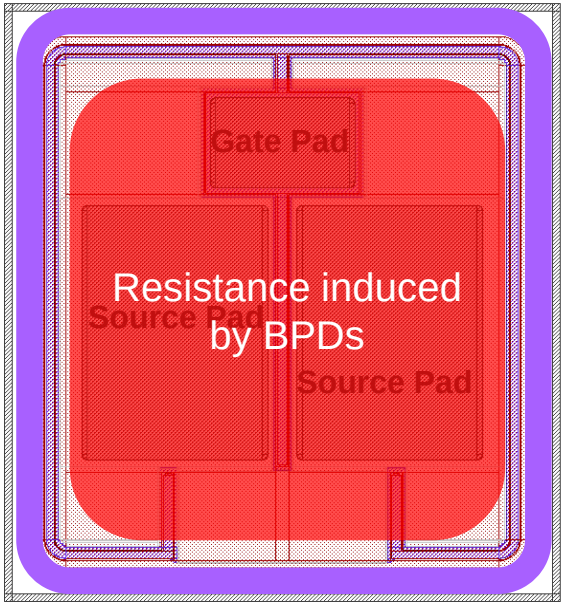


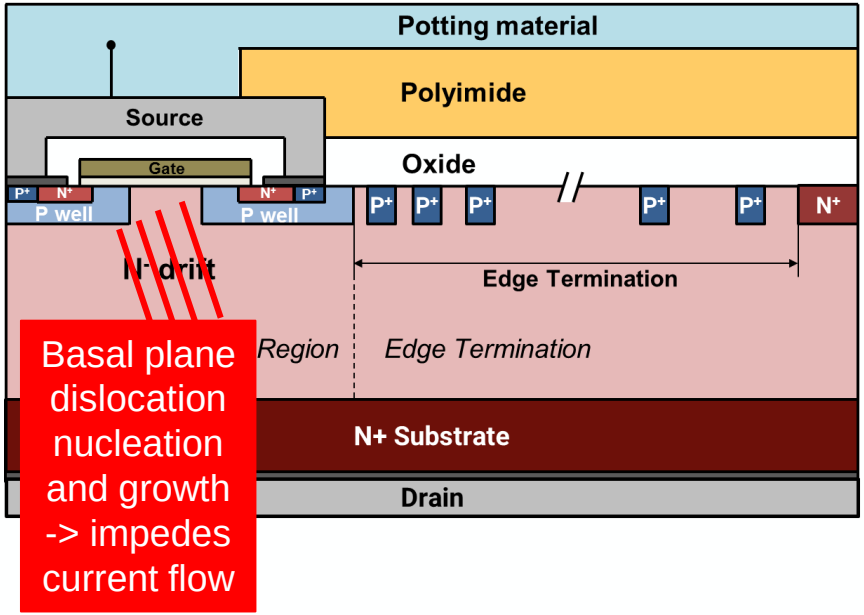
Trapping -> threshold voltage drift

Gate oxide breakdown

Reliability stresses: TDDB, HTGB, HTGS, PBTI, NBTI

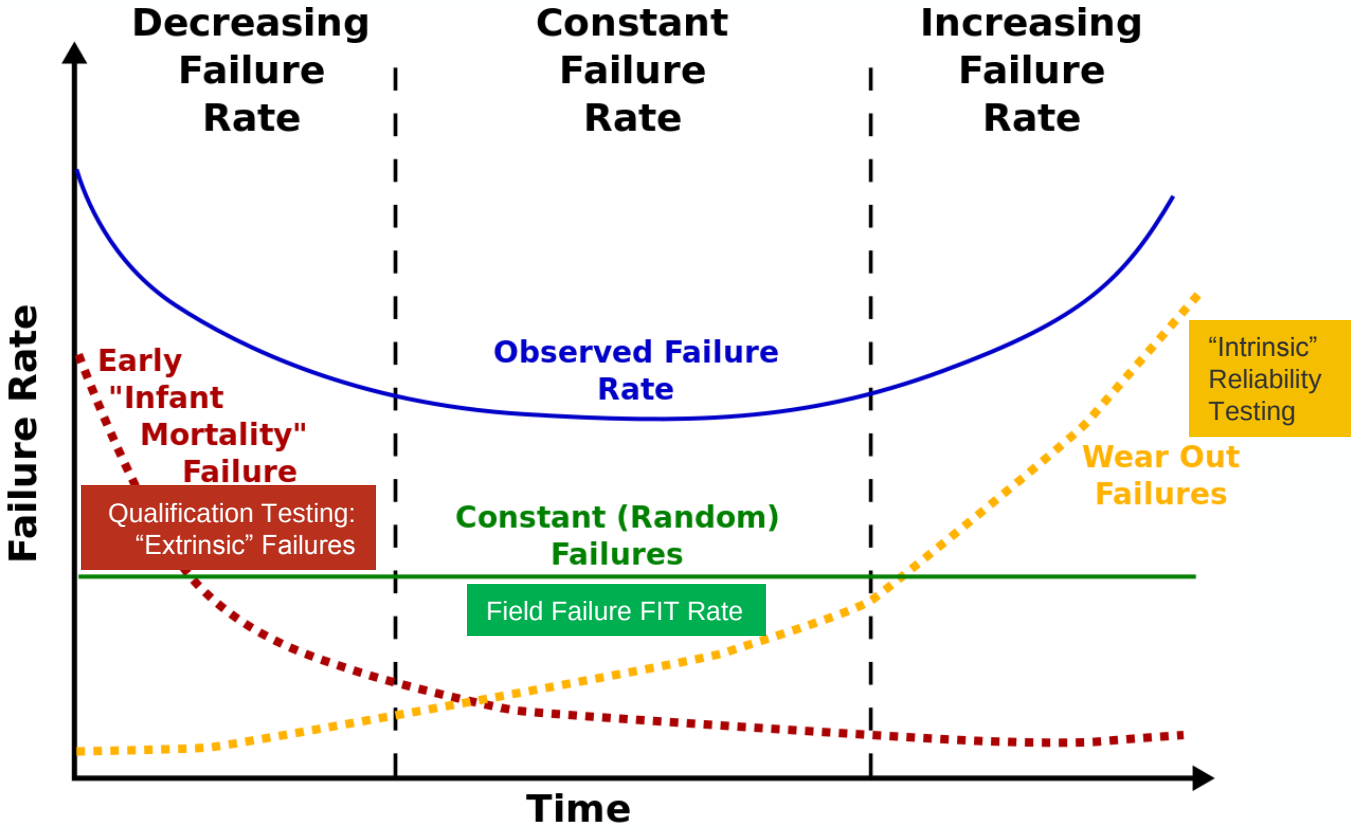
3rd Quadrant Operation Potential Failure Mechanism





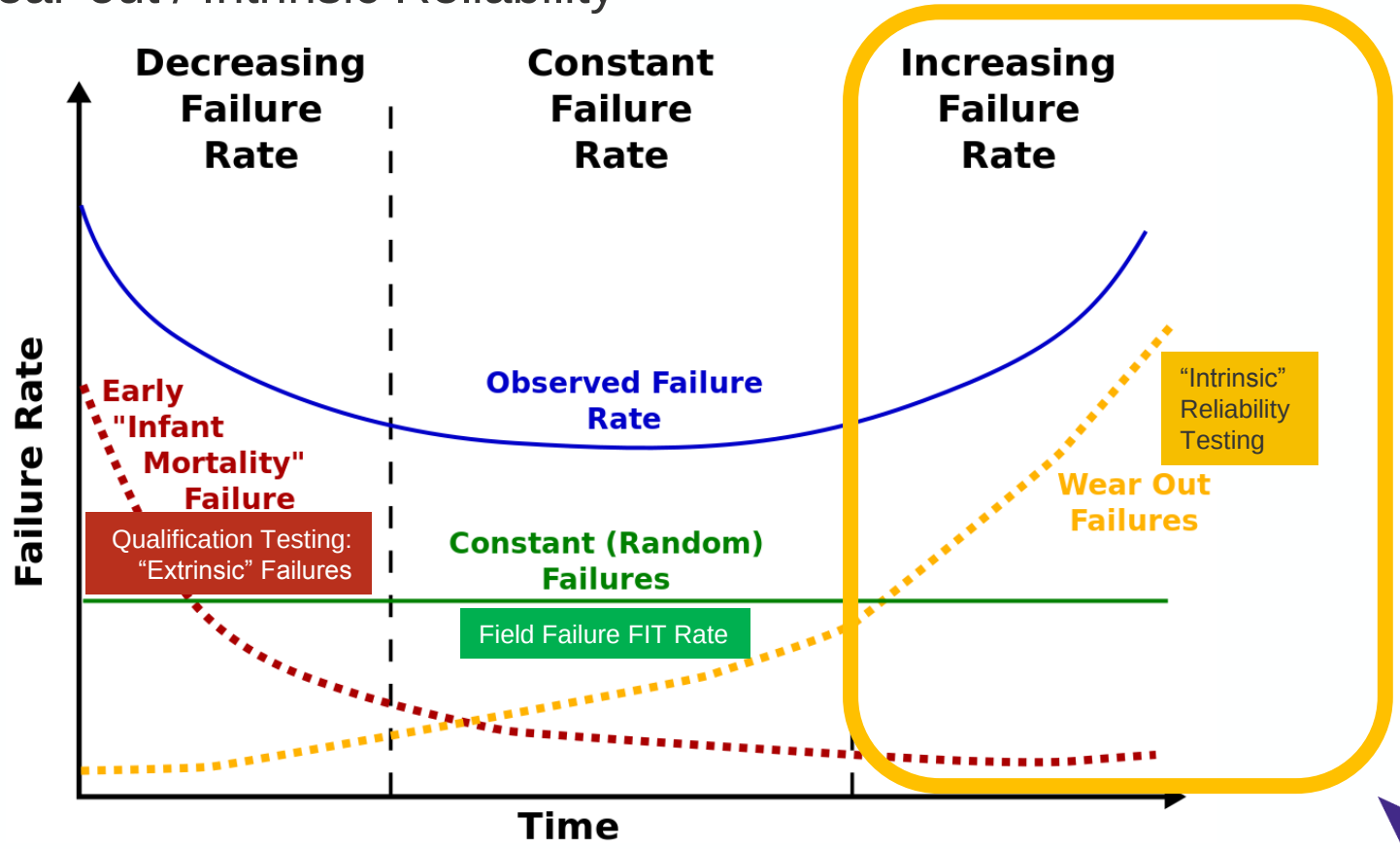
Reliability stress: Body diode HTOL

Reliability Overview – “Bathtub Curve”



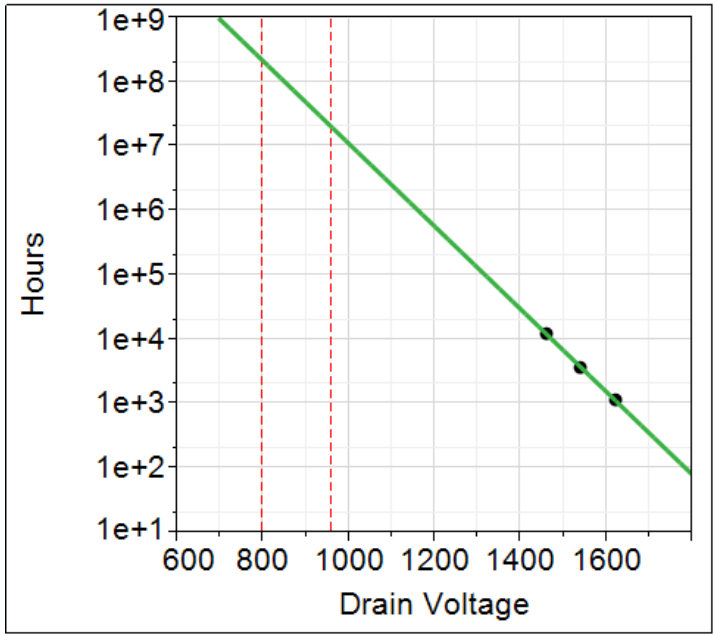
Wear-out mechanisms & intrinsic reliability

Wear-out / Intrinsic Reliability

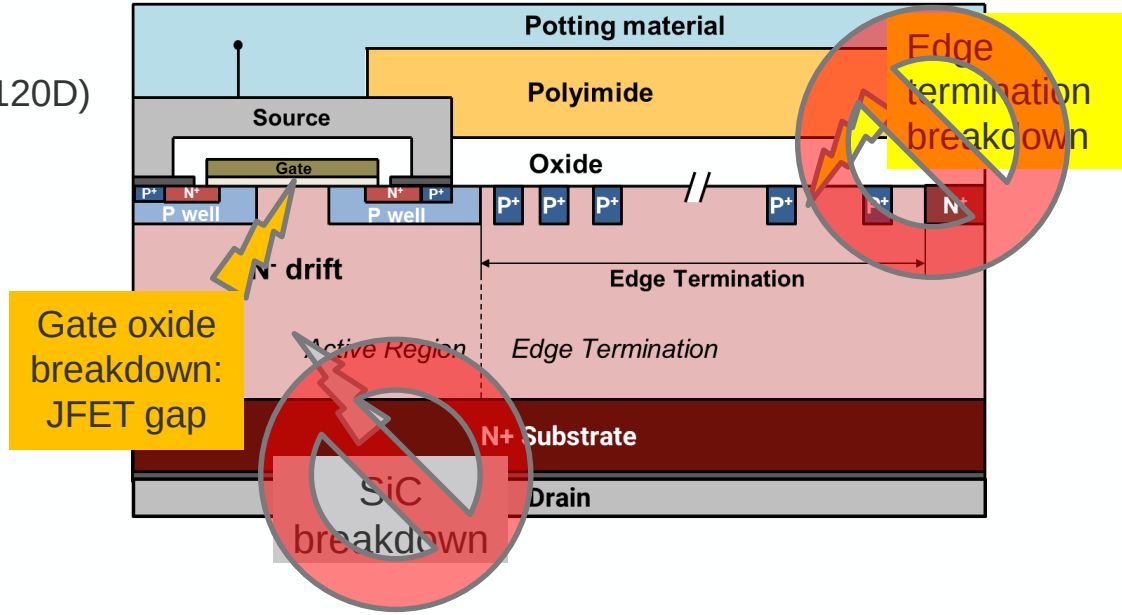


Accelerated life test high temperature reverse bias (ALT-HTRB)

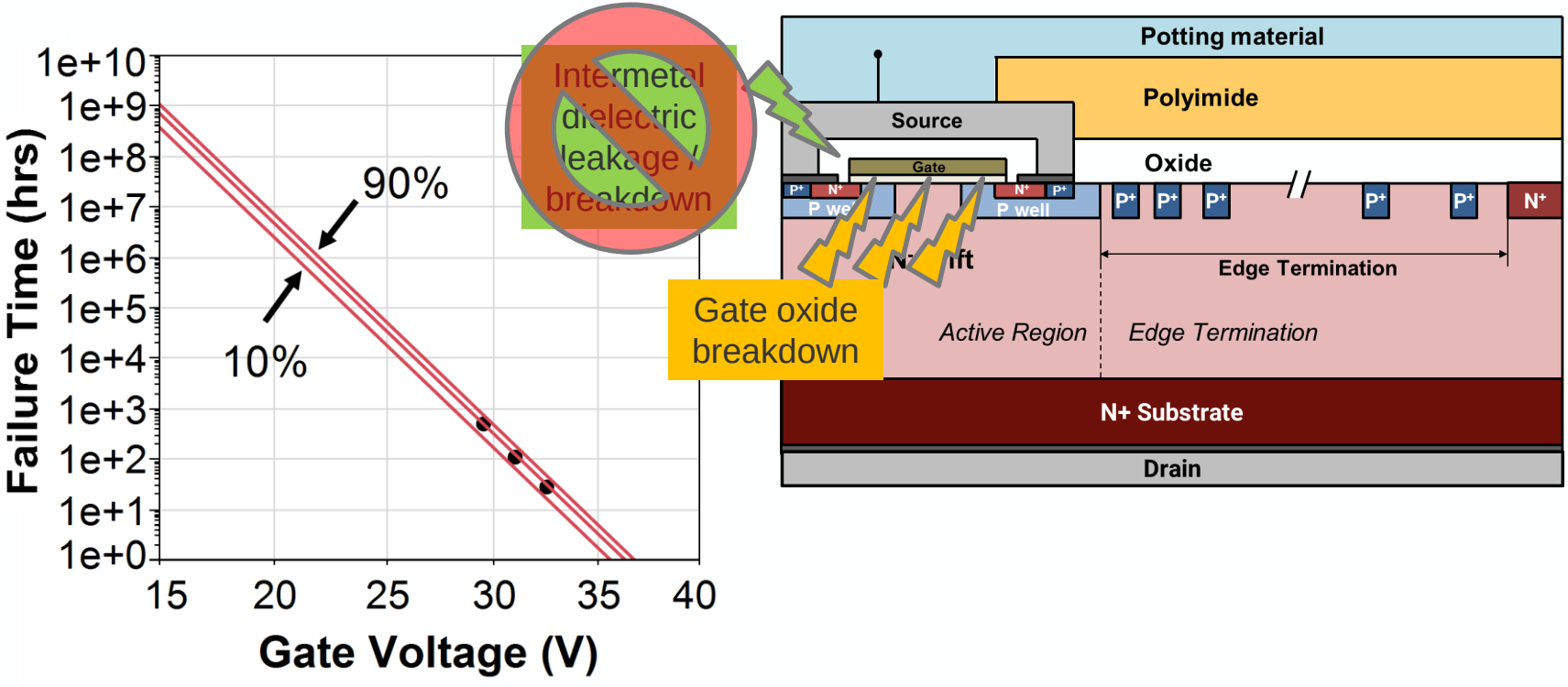
Full production 1200V, 80 mΩ MOSFETs in TO-247-3 packages (Wolfspeed C2M0080120D)



D. Gajewski et al., IIRW, 2016



Time-Dependent Dielectric Breakdown (TDDB)

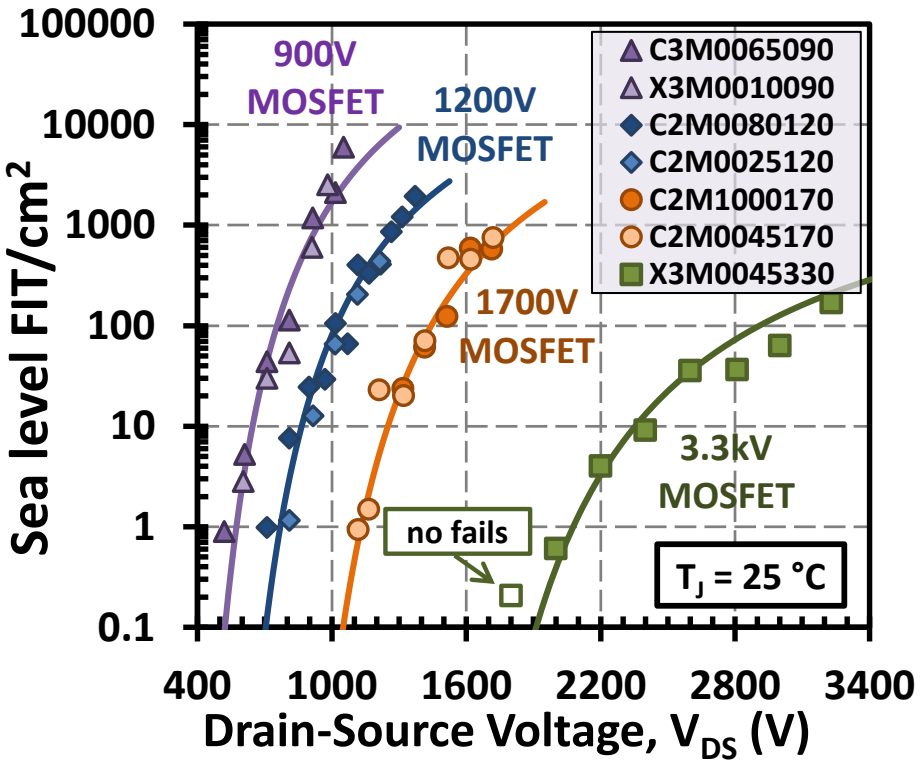


D. Lichtenwalner et al., ECSCRM 2018

Predicts >1E8 hours at 15V and 175C

Terrestrial Neutrons

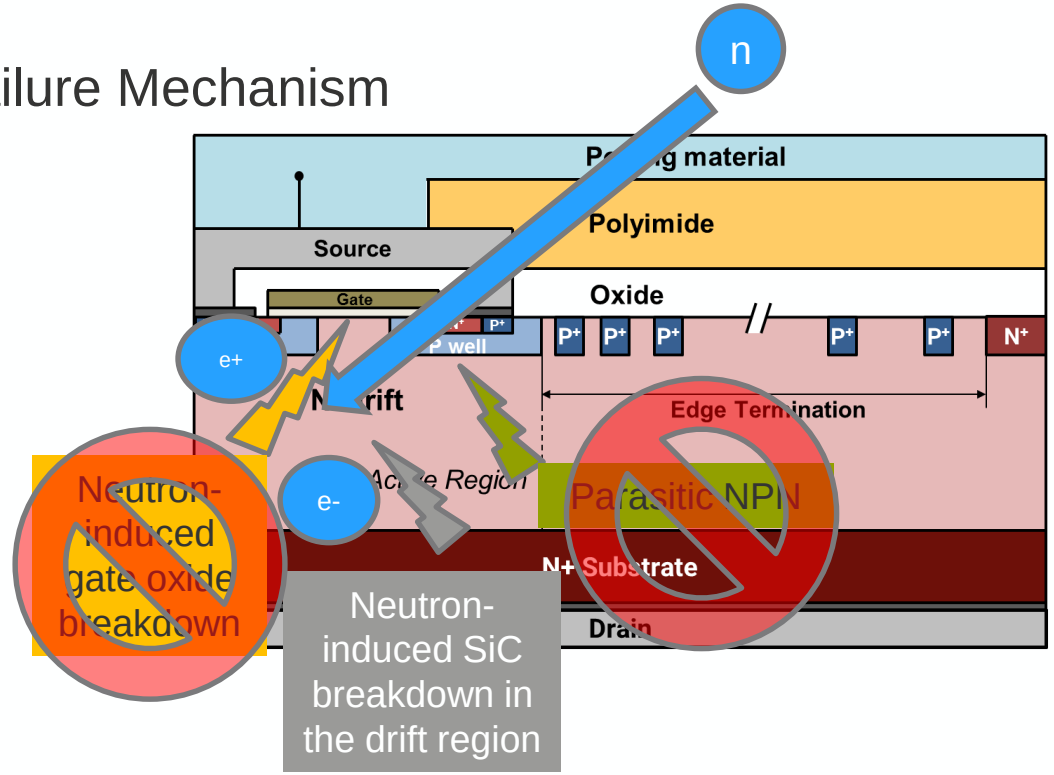
- Wolfspeed SiC MOSFET FIT rates: scaling by active area
- Failure rate increases proportionally with device area
- Failure rate decreases as voltage rating increases
- FIT/cm^2 vs V_{DS} for Wolfspeed MOSFETs
  - 900V 65 mohm
  - 900V 10 mohm
  - 1200V 80 mohm
  - 1200V 25 mohm
  - 1700V 1000 mohm
  - 1700V 45 mohm
  - 3.3kV 45 mohm



D. Lichtenwalner et al., IRPS 2018

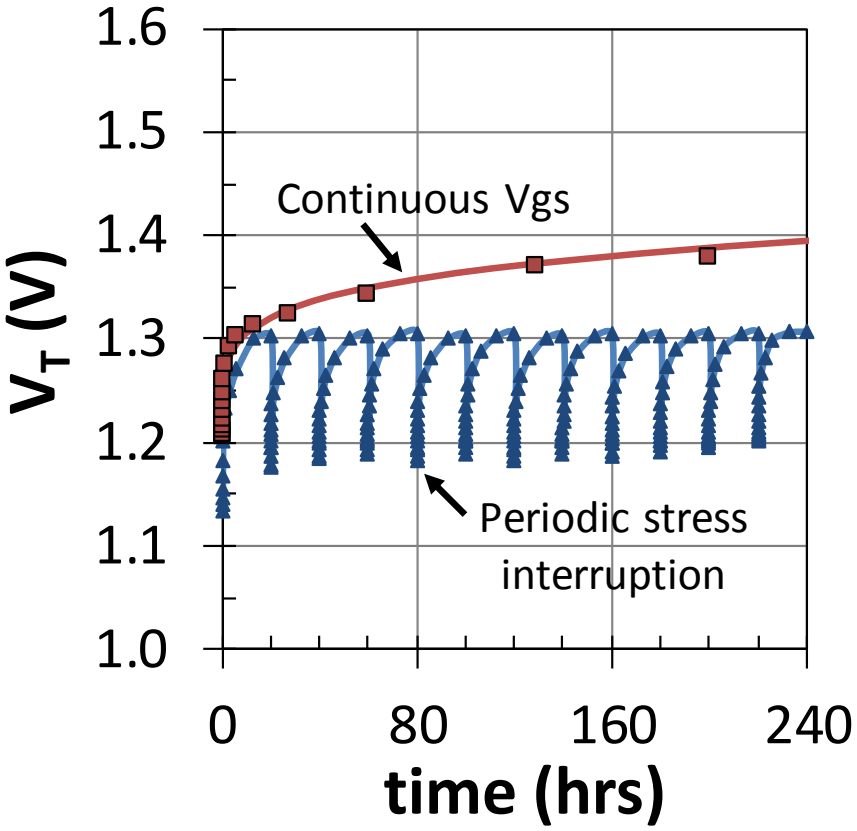
Terrestrial Neutrons Failure Mechanism

- Only drift-related breakdown is observed
- No gate oxide breakdown
- No parasitic NPN turn-on



Threshold Voltage Stability / BTI Relaxation Effects

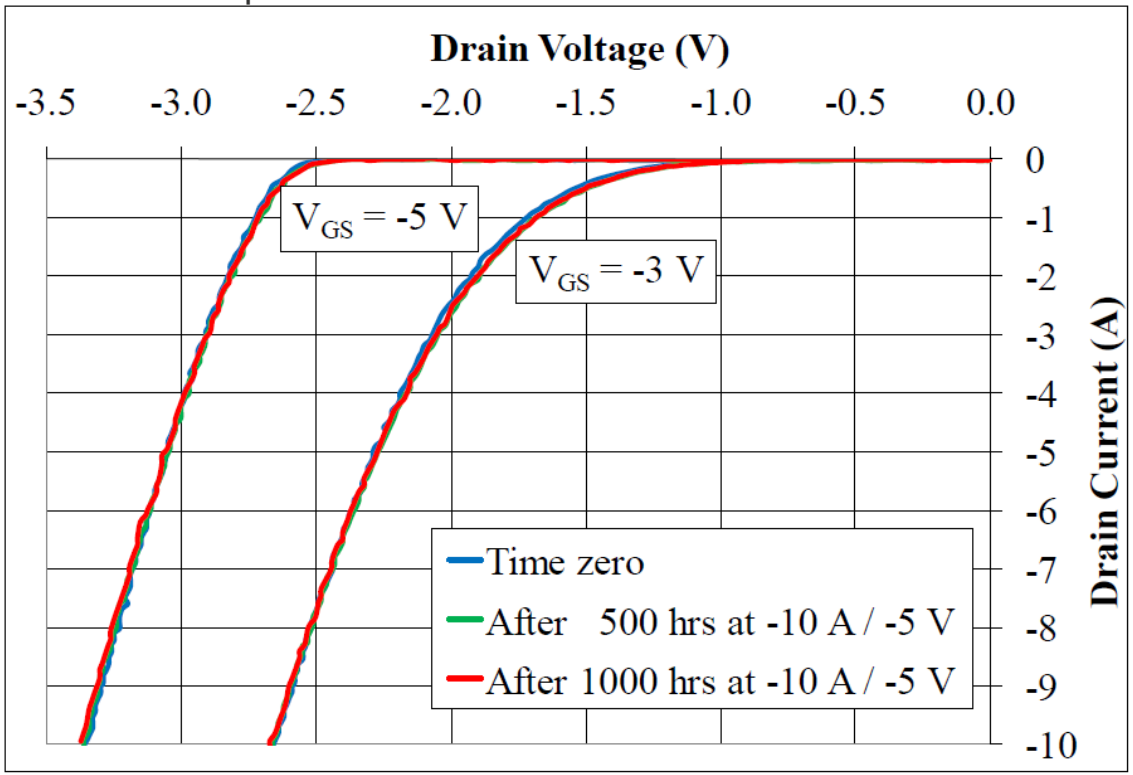
- Threshold voltage drift is accelerated with gate voltage and temperature
- $\Delta V_T(t)$ is less for periodically interrupted gate stress compared to continuous gate stress – relaxation effect
- Interrupted stress more closely represents real switching applications and is therefore more meaningful



Body Diode

- HTOL stress in 3rd quadrant mode
- Body diode and MOSFET VF values measured pre/post stress – negligible parametric drift

Wolfspeed Gen2 1200V 80 mOhm MOSFET



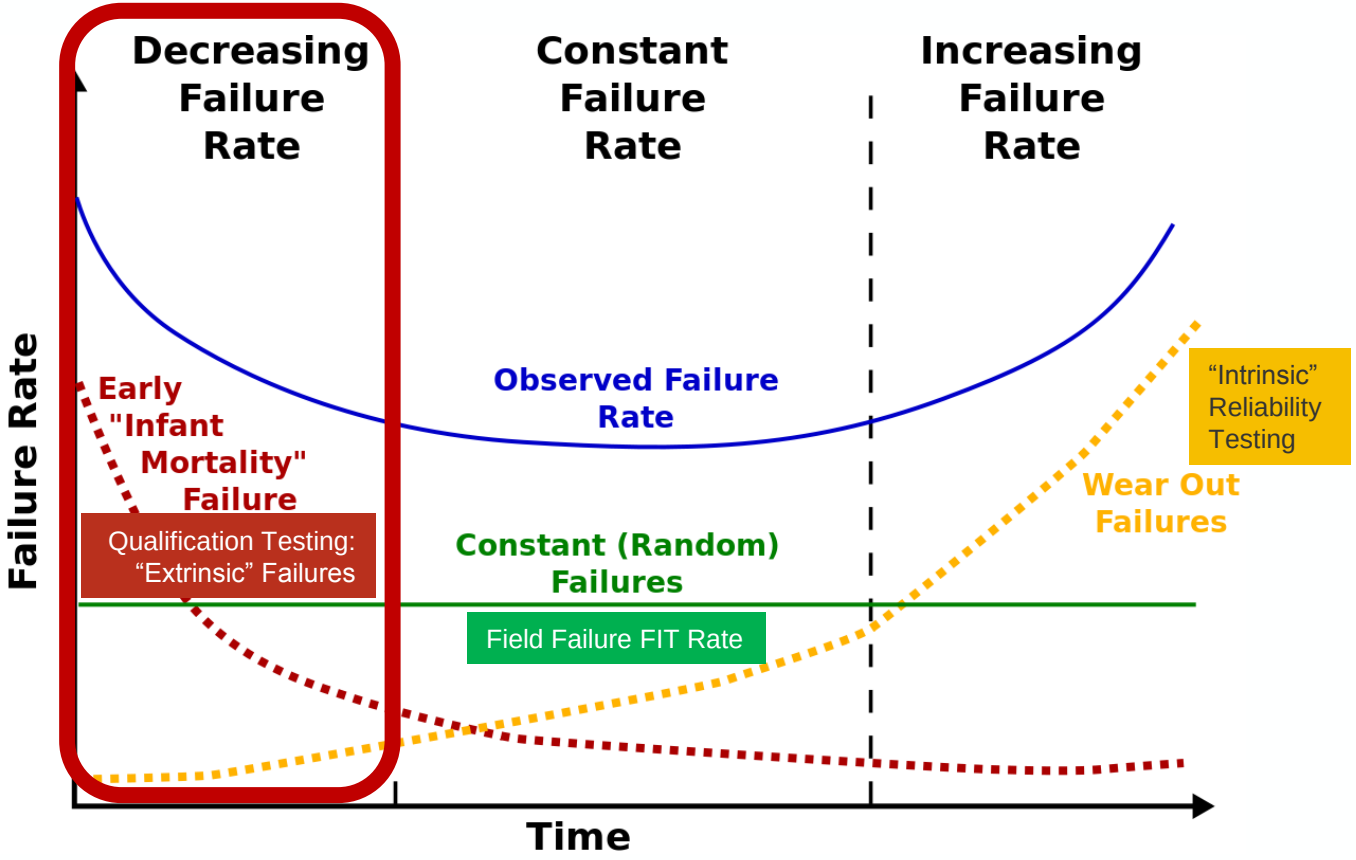
D. Gajewski et al., ICSCRM 2013 / Mat. Sci. Forum v.778-780

THB

- THB is a standard qualification test in all industry standard guidelines, but AEC-Q101 calls out THB stressing only up to 100 V
- In response to showing reliable performance under humid conditions, Wolfspeed has developed the “THB-80” test:
  - 85 °C and 85% RH at 80% of rated blocking voltage
- Recently released Wolfspeed E-Series :
  - Gen3 900 V MOSFETs
  - Gen4 1200 V Schottky diodes
  - Both have passed THB-80 qualification testing for 1000 hours with no visible evidence of corrosion

Product qualification

Product Qualification



Typical Product Qualification

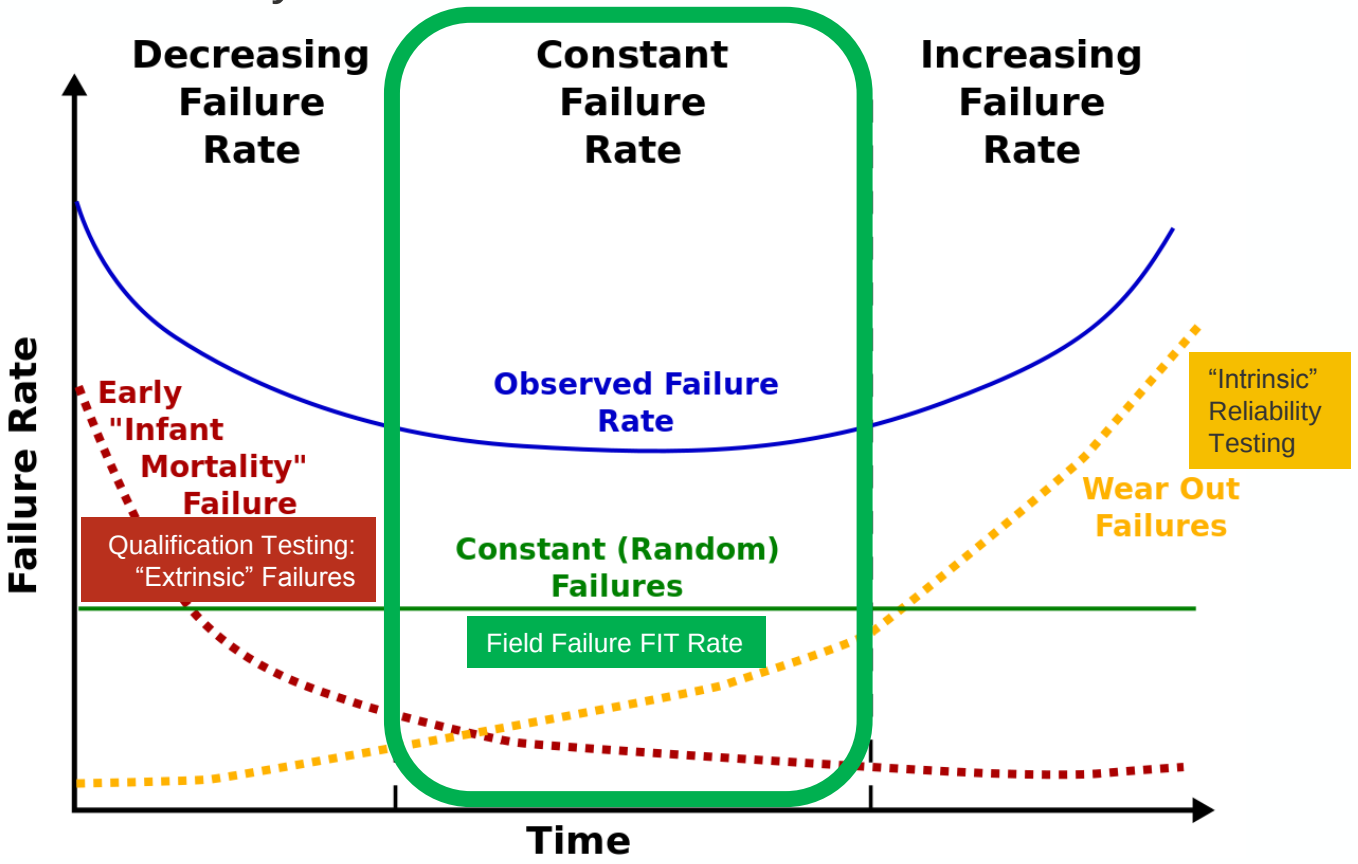
Stress	Abrv	Sample Size Per Lot	# of Lots	Reference (current revision)	Additional Requirements	Accept on # Failed
High Temperature Reverse Bias	HTRB	77	3	MIL-STD-750-1 M1038 Method A	1000 hours at Vmax and Tcmax	0
High Temperature Gate Bias	HTGB	77 each Vgs>0 and Vgs<0	3	JESD22 A-108	1000 hours at VGSmax and VGSmin and Tcmax	0
Temperature Cycling	TC	77	3	JESD22 A-104	1000 cycles Ta_max/Ta_min	0
Unbiased Highly Accelerated Stress Test	UHAST	77	3	JESD22 A-118	96 hours at 130 °C and 85% RH	0
High Humidity High Temp. Reverse Bias	H3TRB	77	3	JESD22 A-101	1000 hours at 85 °C, 85% RH with device reverse biased to 100 V	0
Intermittent Operational Life	IOL	77	3	MIL-STD-750 Method 1037	6000 cycles, 5 minutes on / 5 minutes off, devices powered to ensure DTJ ≥ 100 °C	0
Destructive Physical Analysis	DPA	2	3	AEC-Q101-004 Section 4	Random sample of parts that have successfully completed H3TRB and TC	0

Recent Product Qualifications of Note

- Wolfspeed E-series full 3x77 automotive AEC-Q101 plus THB-80 for EV market
  - Gen3 900V SiC MOSFETs
  - Gen4 1200V SiC Diodes
- Wolfspeed Gen3 1200 V SiC MOSFETs
- Wolfspeed Gen3 3.3 kV and 10 kV SiC MOSFETs
- First all-SiC Wolfspeed 1.2 kV power module
  (Gen2 MOSFET and Gen5 Schottky diode)

Field reliability

Field Reliability



Wolfspeed Power Field Reliability

Technology	Fielded Device Hours (Billions)*	FIT Rate (valid field failures per billion device hours)**
CSDxxx060 Diode	1203	0.1
C2Dxxx120 Diode	511	0.6
C3Dxxx060 Diode	2919	0.06
C4Dxxx120 Diode	708	0.2
C2M MOSFET	63	3.7
C3M MOSFET	11	4.1

- *Calculated today's date minus confirmed ship date minus 90 days (allowing for time to put into service) * 12 hours per day
- **Calculated as: 2 times the number of valid field failures (excludes engineering evaluations, as-received visual defect escapes or issues, as-received test escapes, packaging and assembly quality issues) divided by fielded device hours; includes an additional factor for statistical confidence margin

Conclusion

- SiC power devices have some unique reliability considerations in addition to Si power devices
- SiC failure mechanisms have been identified and testing methods have been developed to characterize them effectively
- Successful product qualifications and field reliability show that the reliability science is paying off, and SiC is ready for large volume manufacturing for high reliability applications

Extra Slides

Wear-out mechanisms & intrinsic reliability

THB

Wear-out mechanisms & intrinsic reliability

Body Diode

Threshold Voltage Stability (PBTI or NBTI)

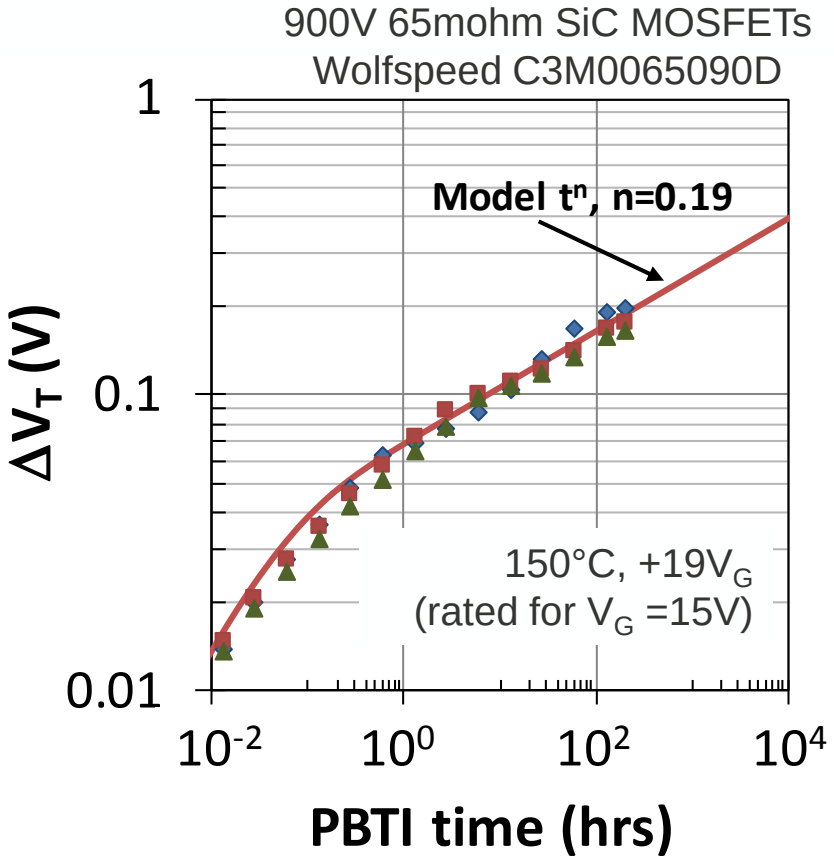
- PBTI (NBTI) = Positive (Negative) Bias Temperature Instability: threshold voltage shift (ΔV_T) with time can change the device on-state and/or blocking characteristics
- ΔV_T relates to interface & oxide traps [1,2] (filling/emptying/creation):
  $\Delta V_T = q*(\Delta N_{ox}+\Delta N_{IT})*[(q*T_{ox})/(K_{ox}*\varepsilon_o)]$
- ΔV_T of Si MOSFETs depends on MOS gate electric field, temperature, and time [1,2]:
  - $\Delta V_T = A*\exp(\gamma E_{ox})*\exp(-\mathbf{E_A}/kT)*t^{\mathbf{n}}$
  - n typically ~0.2 – 0.25 for Si devices
- SiC has an order of magnitude higher number of interface traps (N_{IT}) than Si devices, and likely higher near-interface oxide trap density (N_{ox})
  - V_T stability is a potential concern
- N interface passivation may introduce additional effects.

[1] J.H. Stathis and S. Zafar, “The negative bias temperature instability in MOS devices: A review,” Microelectronics Reliability 46 (2006) pp. 270-286.
[2] D.K. Schroder, “Negative bias temperature instability: What do we understand?” Microelectronics Reliability 44 (2007) pp. 841-852.

Threshold Voltage Stability in SiC Power MOSFETs

n ~ 0.19: similar to nitrided SiO2/Si

Suggests similar mechanism



Wear-out mechanisms & intrinsic reliability

Terrestrial Neutrons

Wear-out mechanisms & intrinsic reliability

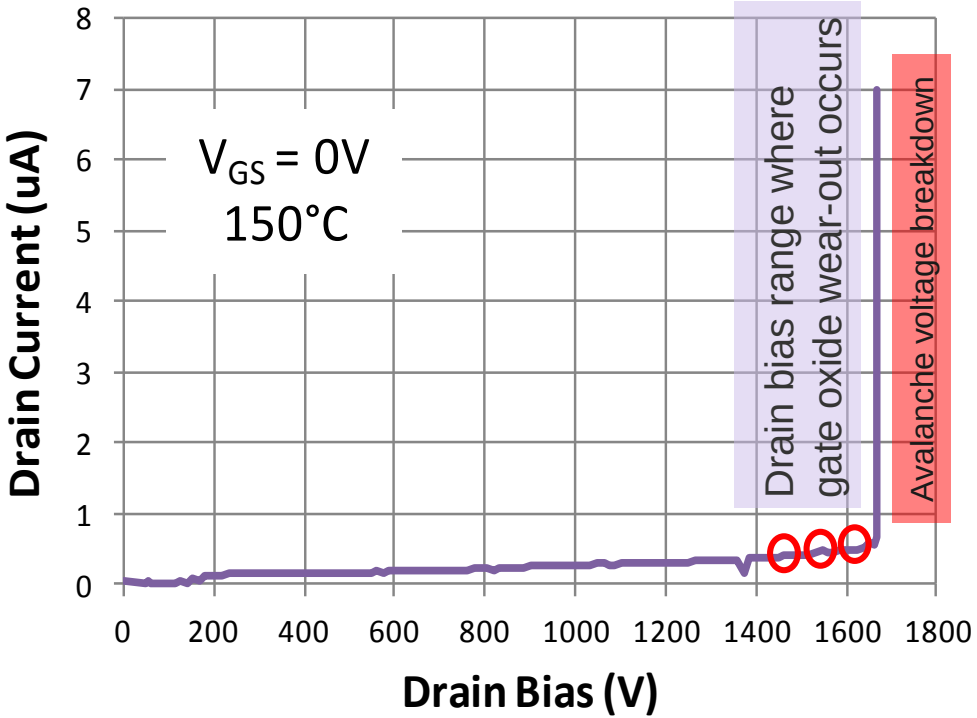
TDDB

Wear-out mechanisms & intrinsic reliability

ALT-HTRB

Accelerated life test high temperature reverse bias (ALT-HTRB)

- Full production
  1200V, 80 mΩ MOSFETs in
  TO-247-3 packages
  (Wolfspeed C2M0080120D)
- Reverse bias breakdown can be accelerated with drain voltage almost up to the avalanche voltage



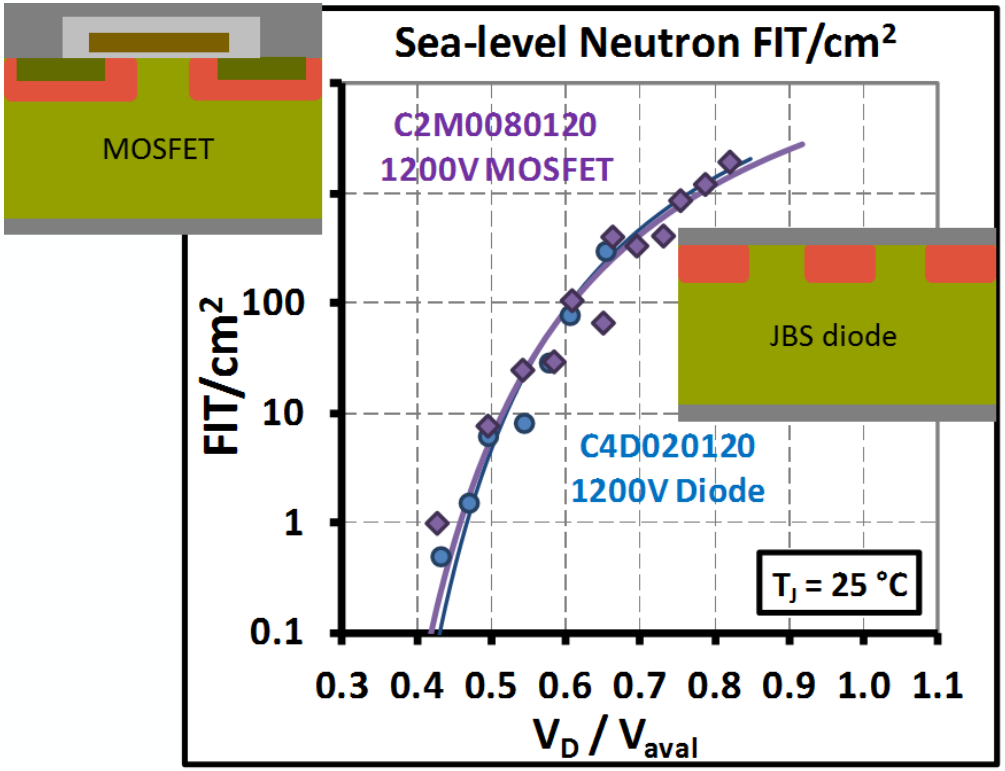
D. Gajewski et al., IIRW, 2016

Accelerated life test high temperature reverse bias (ALT-HTRB)

- Full production
  1200V, 80 mΩ MOSFETs in
  TO-247-3 packages
  (Wolfspeed C2M0080120D)
- ~30 devices per stress voltage;
  MTTFs shown
- Fit with Weibull statistics and
  linear-V model
  - Empirical fit seems pretty good
  - Extensive testing over wide range of
    testing not yet shown to distinguish from
    other gate oxide wear-out models such as:
    - V^{-n}
    - 1/E
- Predicts high lifetimes at typical use
  voltages

Terrestrial Neutrons: MOSFETs and Diodes

- MOSFETs and diodes show the same neutron reliability:
- Active area & drift effects dominate reliability
- Failure analysis shows no indication of MOSFET parasitic NPN turn-on or gate oxide breakdown

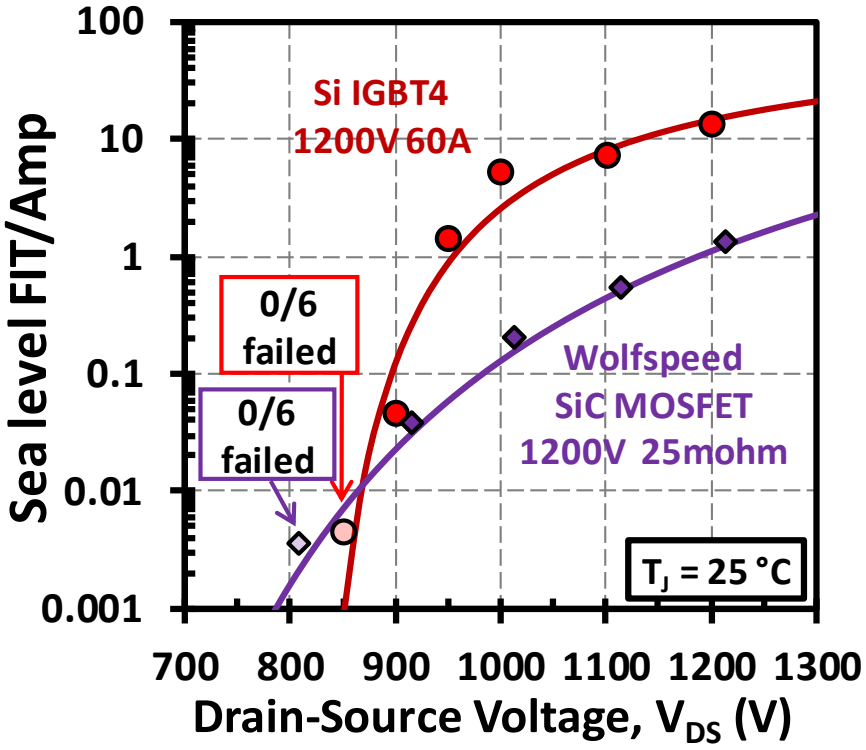


D. Lichtenwalner et al., IRPS 2018

Terrestrial Neutrons: SiC vs. Si

- Si IGBTs show sharper failure onset, but higher max failure rate
- Both the SiC & Si parts may require a VDS derating, but SiC is more immune to VDS overshoot

SiC MOSFET has 10X lower FIT rate at high V_{DS}



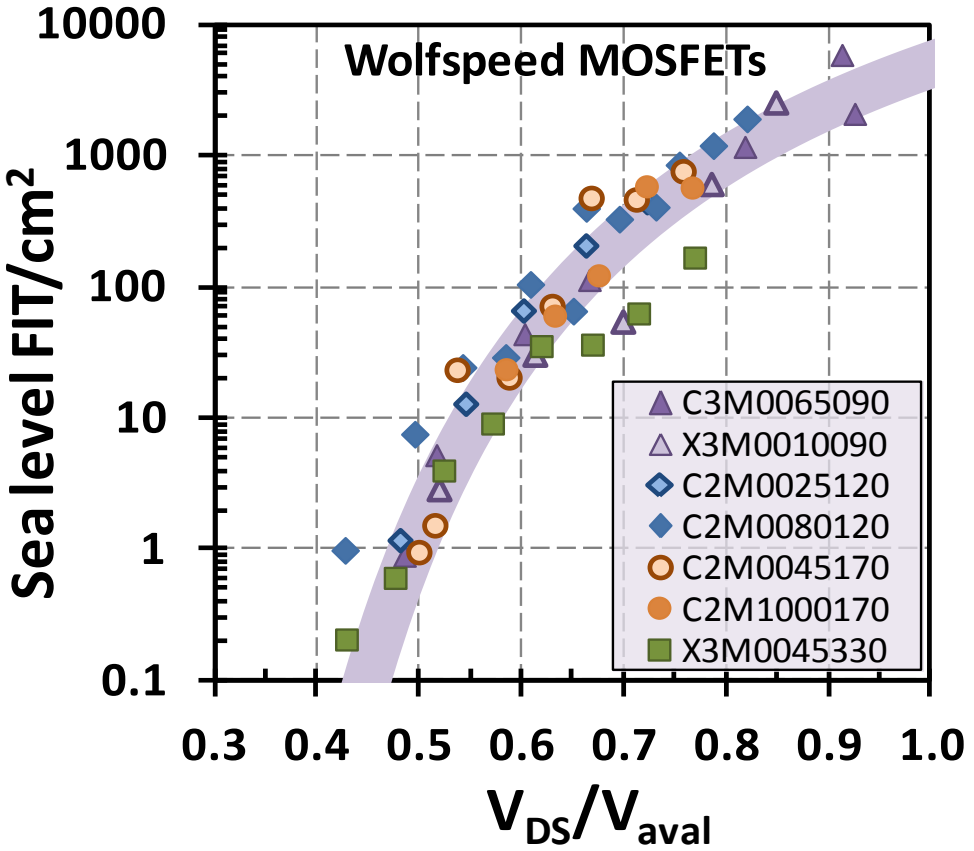
D. Lichtenwalner et al., IRPS 2018

Wear-out mechanisms & intrinsic reliability

Threshold Voltage Stability

Terrestrial Neutrons

- All device FIT rates scale similarly with active area & drift field (relative to avalanche)
- Active area & drift design can be tailored to meet application-specific system lifetime requirements

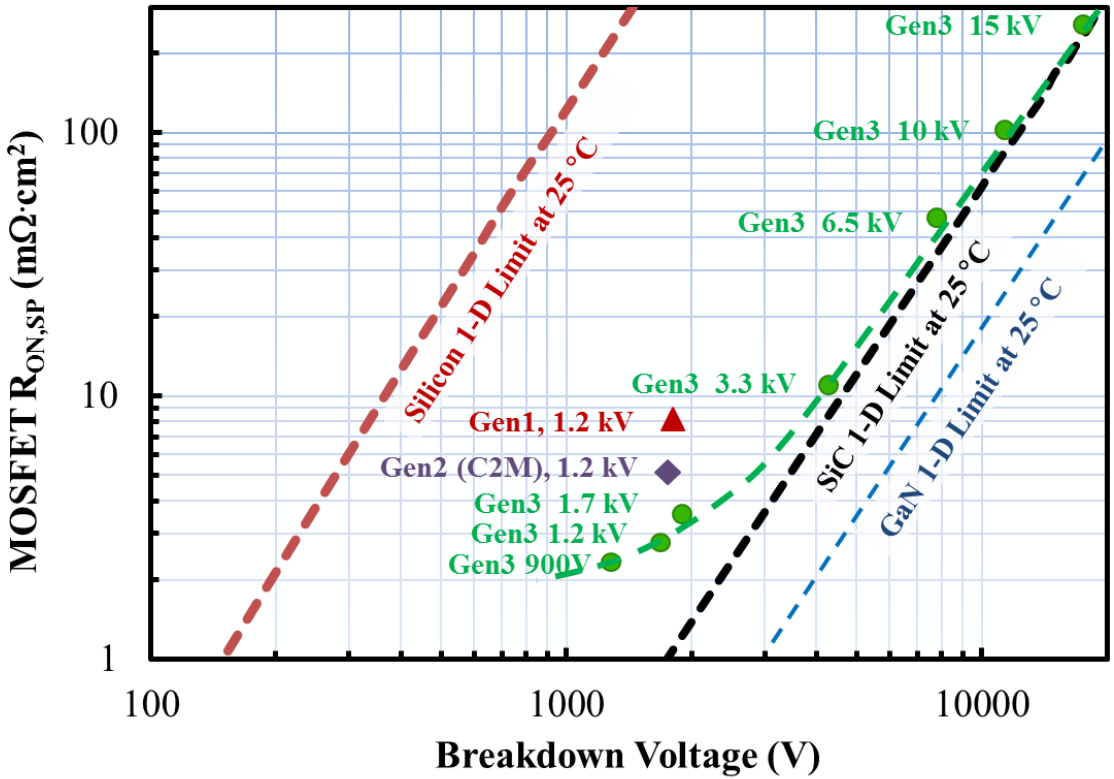


D. Lichtenwalner et al., IRPS 2018

Application considerations

Blocking Voltage -> Electric Field

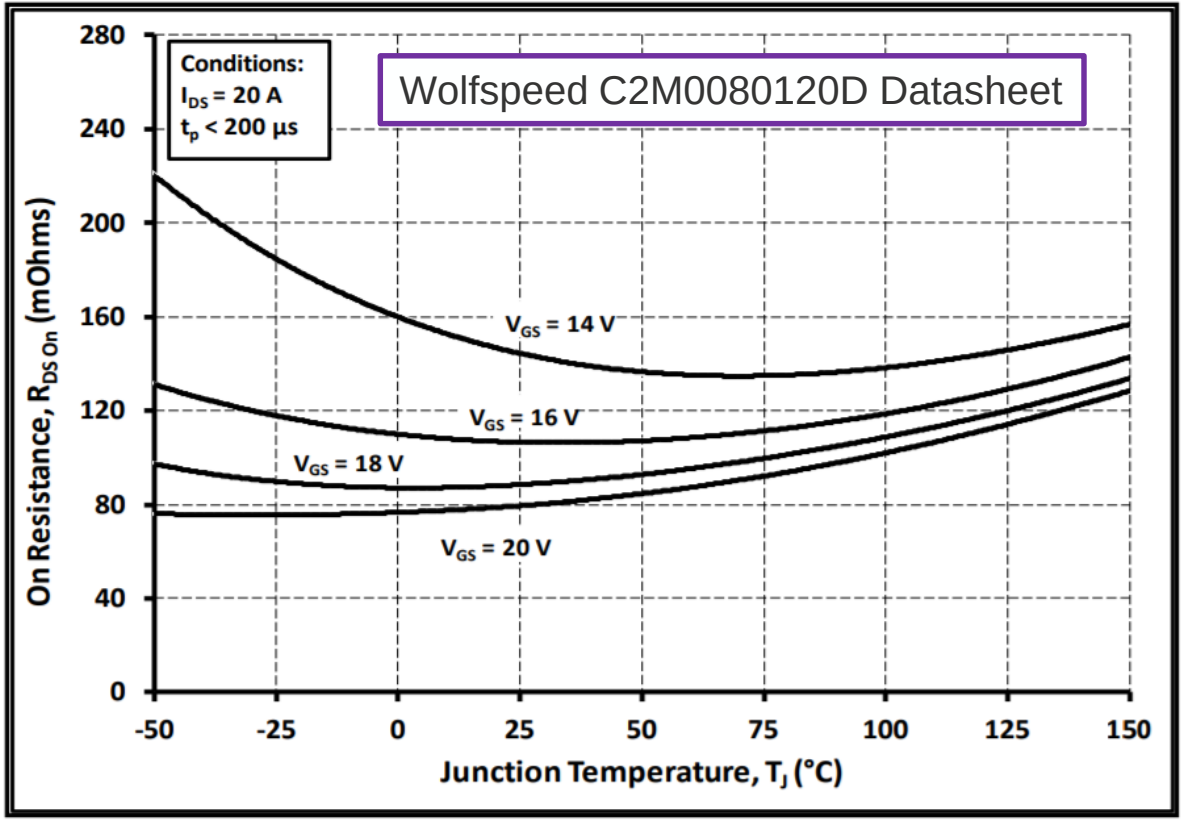
J.W. Palmour et al., Proc. ISPSD, pp.79-82 (2014)



High blocking voltage

Need high electric field reliability

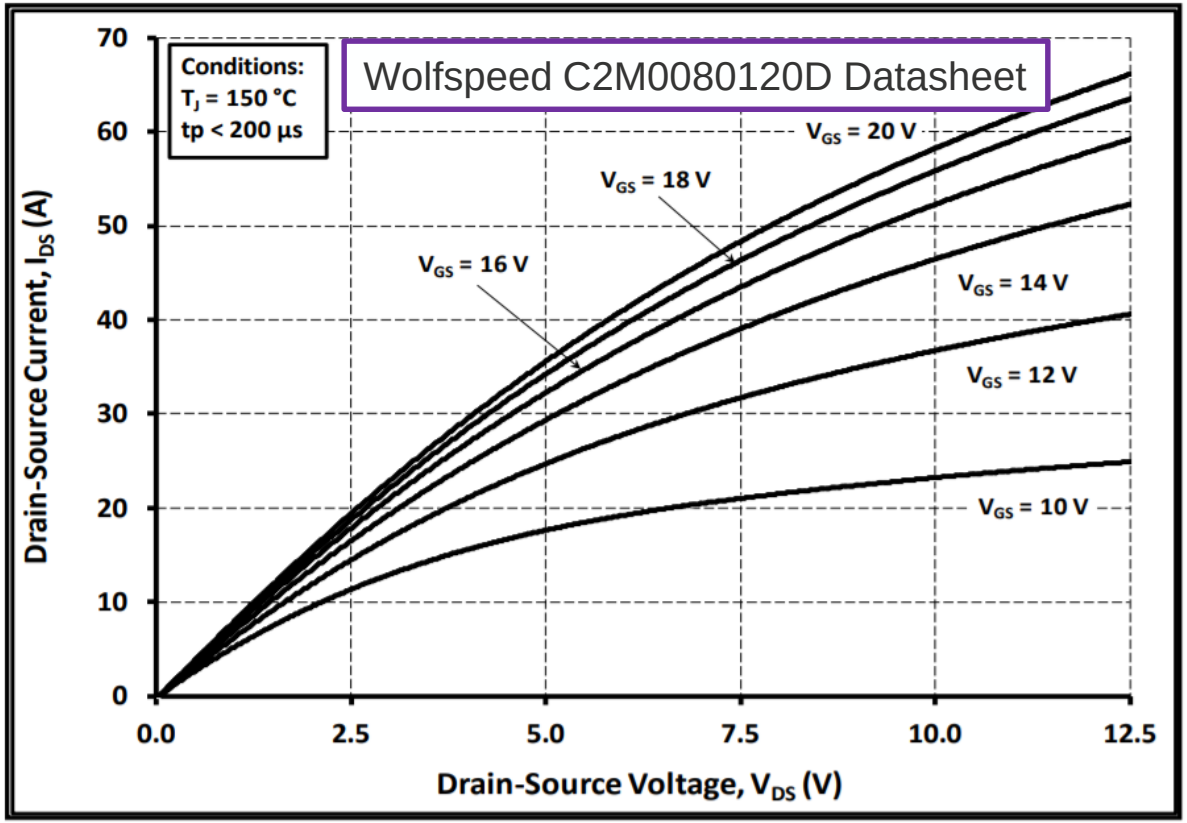
Gate Oxide Voltage vs. On-Resistance -> Performance



High gate oxide voltage

Need high gate oxide reliability

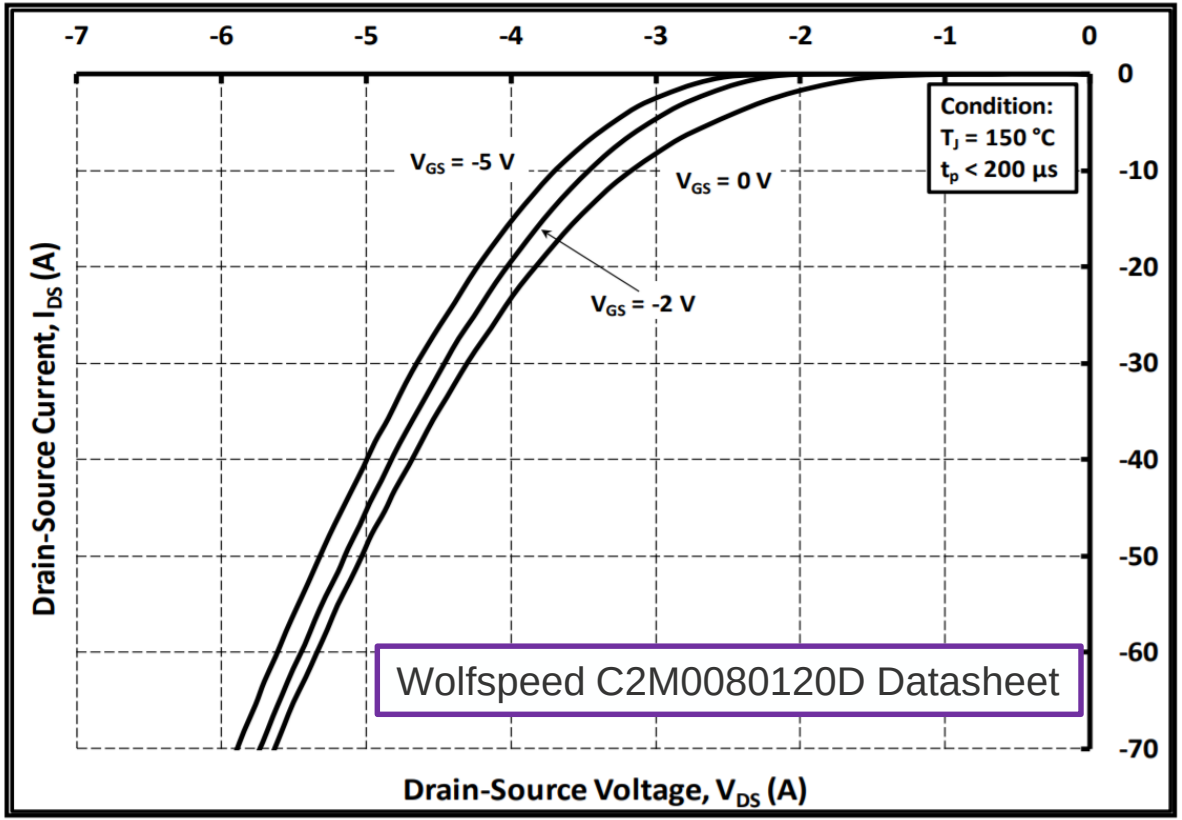
Switching -> Threshold Voltage



Switching

Need high VGS(th) stability

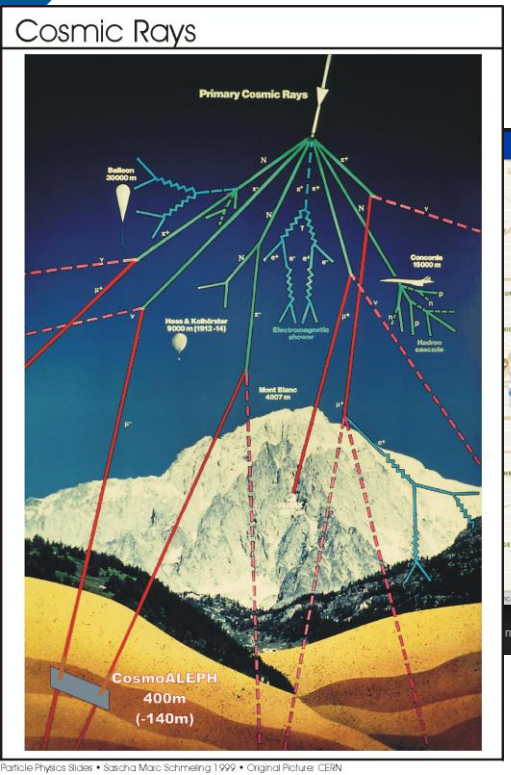
3rd Quadrant Operation

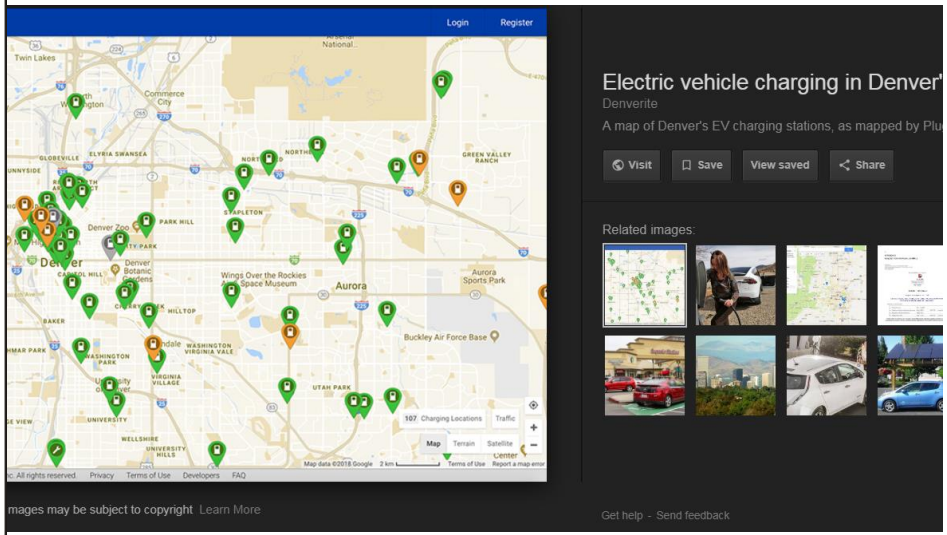


3rd quadrant operation

Need high body diode reliability

High Altitude Applications -> Terrestrial Neutrons





Google, 2018

High altitude applications

Need high terrestrial neutron reliability

Outline

- Mission profile considerations and device salient features
- Potential failure mechanisms
- Wear-out mechanisms & intrinsic reliability
- Product qualification
- Field reliability
- Industry-wide consortia guidelines and standards

Typical THB-80 Assessment

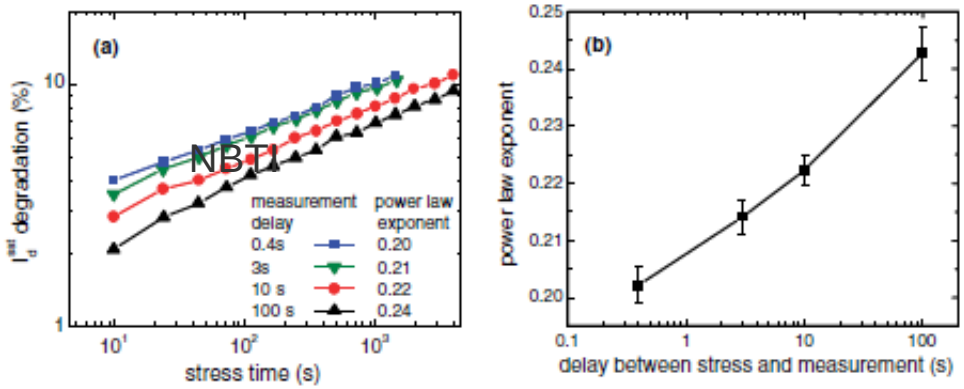
Stress	Abrv	Sample Size Per Lot	# of Lots	Accept on # Failed	Reference (current revision)	Additional Requirements
Temperature-Humidity-Bias at 80% of Rated Voltage	THB-80	77	3	0	NA	1000 hours at 85 °C, 85% RH with device reverse biased to 80% of rated voltage

Typical ESD Classification

Stress	Abrv	Sample Size Per Lot	# of Lots	Reference (current revision)	Additional Requirements
ESD Characterization	ESD	10 each HBM and CDM	3	AEC Q101-001 and Q101-005	For HBM: gate-to-source pulsing (worst case pin combination)

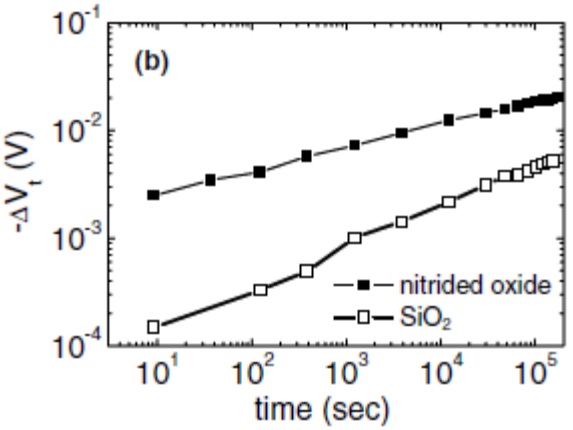
Threshold Voltage Stability in Si CMOS

- $\Delta V_T(t)$ follows a log-log relationship
- ΔV_T and n depend on the sense measurement time (relaxation effects) [1]



1] J.H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability* 46 (2006) pp. 270-286

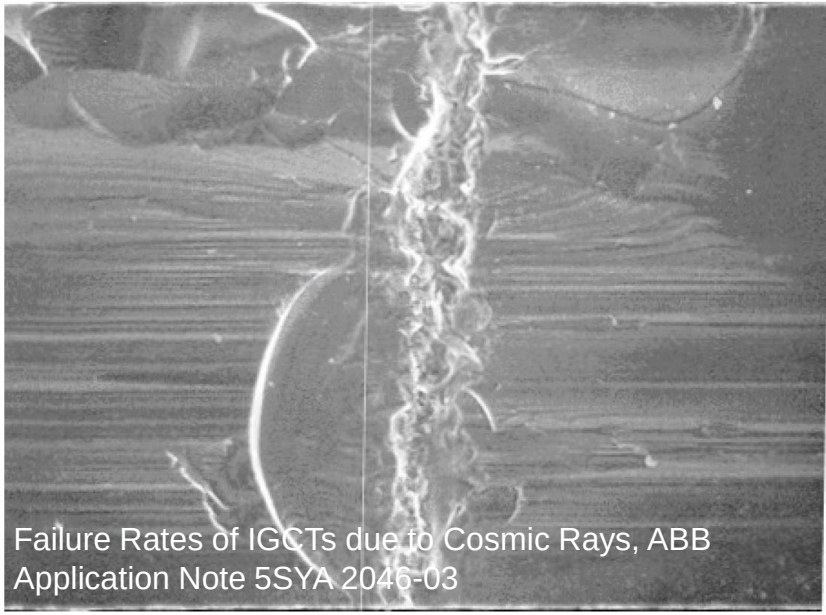
Nitrided oxides on Si have a larger V_T shift, but smaller exponent (n), than SiO_2/Si [1]:



Note: MOS interface on SiC has a ~1/2 monolayer of N due to NO passivation anneal!

Terrestrial Neutrons

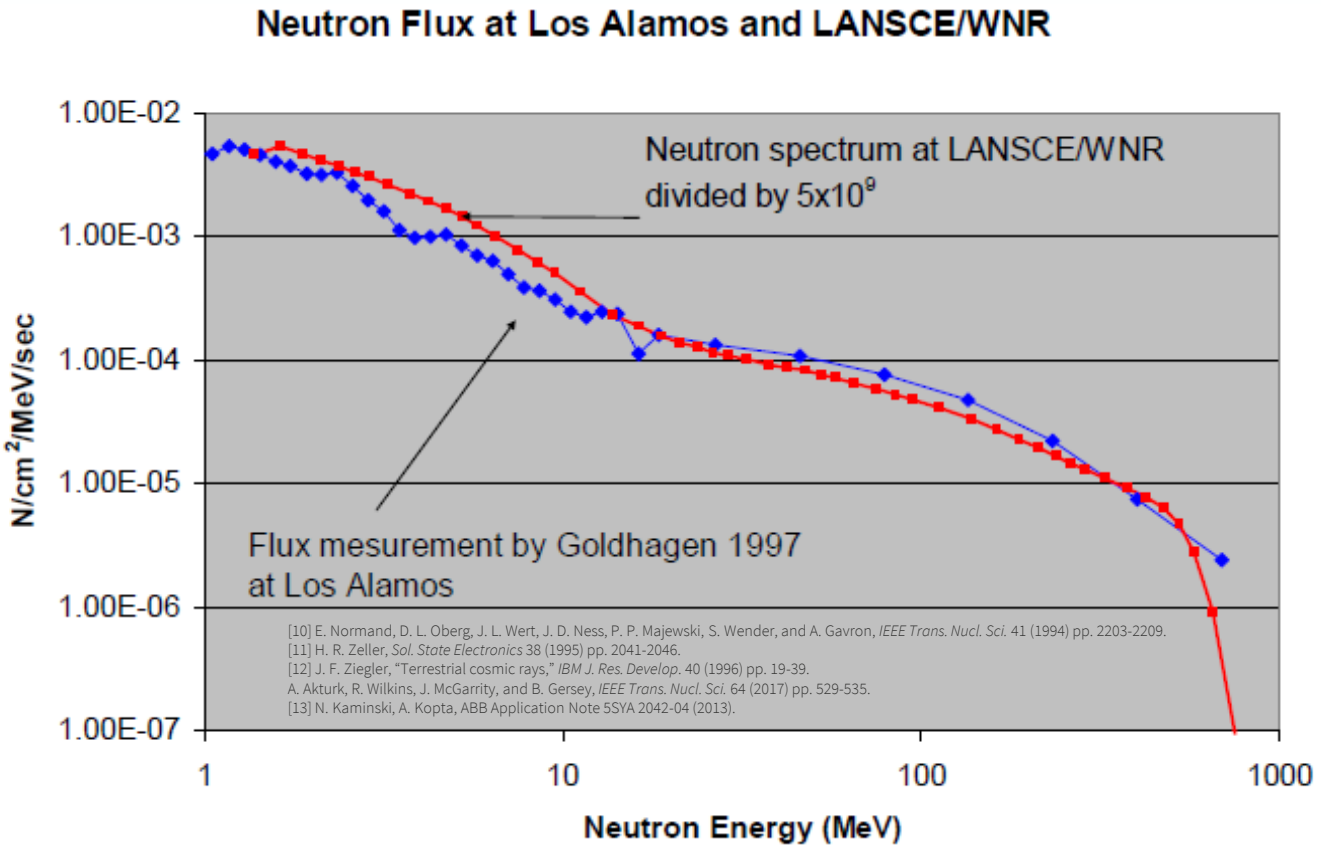
- Failure rate is constant with time (FIT): fails per billion device hours)
- Failures are abrupt with very little sign of degradation prior to failure
- Modeling determined empirically at neutron beam facilities to simulate the effect of terrestrial neutrons:
  - Linear V drain voltage acceleration
  - Temperature deceleration (negative activation energy! but this is a small effect)
  - Altitude / neutron flux
  - C1-6: empirical constants



A molten channel through a silicon device created by a charge avalanche triggered by incident cosmic rays during blocking.

$$\lambda = C_3 \exp\left(\frac{C_2}{C_1 - V}\right) \cdot \exp\left(\frac{T_0 - T}{C_4}\right) \cdot \exp\left(\frac{1 - \left(1 - \frac{h}{C_5}\right)^n}{C_6}\right)$$

Terrestrial Neutrons



Terrestrial Neutrons

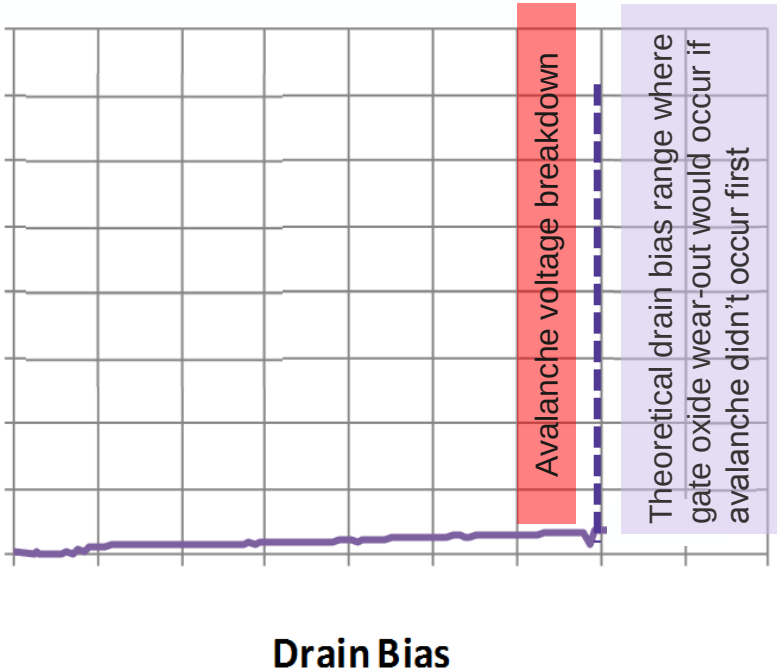
- No lifetime extrapolation required
- Measure actual failure rate due to neutron irradiation @ device use fields
- Only scale the neutron fluence
  - **F**ailure **I**n **T**ime (FIT) = Failures per billion device hours – failure rate
  - FIT rate is scaled to sea level

$$FIT\ Rate\ @\ Sea\ Level = \frac{FIT\ Rate\ under\ Neutron\ flux}{Neutron\ flux}$$

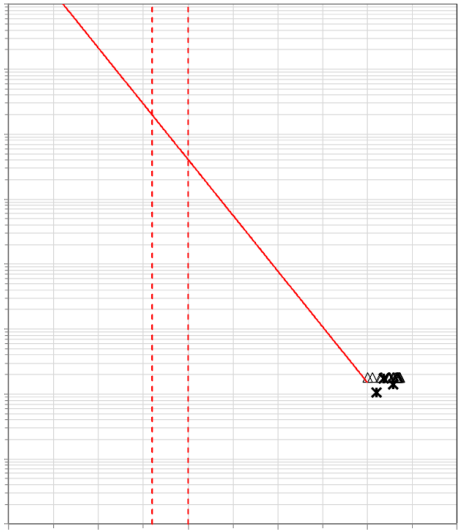
After D. Lichtenwalner et al., IRPS 2018

Accelerated life test high temperature reverse bias (ALT-HTRB)

For certain MOSFET device designs, ALT-HTRB does not work because avalanche breakdown occurs at lower voltage than gate oxide wear-out would theoretically occur



Compare right-censored life test results to other generations (or devices with exaggerated and non-standard channel designs), the voltages and acceleration coefficient can be scaled, and a lower bound can be placed on the lifetime curve



D. Gajewski et al., IIRW, 2016

Reliability Testing

Testing Type	Purpose	Key Metric	Example
Qualification Testing	Designed to demonstrate a minimum outgoing quality and early life failure percentage	Lot Tolerant Percent Defect (LTPD)	3 lots * 77 samples per lot, with ZERO FAILURES, demonstrates LTPD < 1% with 90% statistical confidence
Reliability Testing	Designed to demonstrate the long-term wear-out lifetime that can be expected	Median Time To Failure (MTTF) or t1% (time to 1% failures)	TDDB testing to failure shows that C2M MOSFET MTTF is ~ 30 million hours

Potential Failure Mechanisms Summary

Requirement	Gate oxide breakdown	SiC breakdown	Bipolar NPN	Termination breakdown	Threshold drift	Increased resistance / reduced current flow
High drain bias	HTRB, ALT-HTRB	HTRB, ALT-HTRB		HTRB, ALT-HTRB	HTRB, ALT-HTRB	
High altitude	n-irradiated HTRB	n-irradiated HTRB	n-irradiated HTRB			
High humidity	THB			THB		
High gate bias	TDDB, HTGB				NBTI, PBTI	
3rd quadrant						Body diode HTOL

Industry consortia guidelines and standards

Industry consortia

Consortium	Abbreviation
Joint Electron Device Engineering Council	JEDEC
Automotive Electronics Council	AEC
International Electrotechnical Commission	IEC
Japan Electronics and Information Technology Association	JEITA

JEDEC

- JC-70 committee newly formed to create guidelines (JEPs) and standards (JESDs) for power conversion devices
- Each subcommittee has 3 task groups (TGs)
- TG702_1: SiC reliability and qualification
  - Kicked off activities at WIPDA 2017
  - Charter established, Teams formed to work on guidelines first, to be followed by standards
  - Currently > 50 members from >28 member companies + SMEs
  - Contact me if interested in participating!
- Task groups are open to paid member companies
  - Also welcome participation from subject matter experts from non-member entities, such as academia