Meeting Industry Requirements for GaN Device Reliability

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Agenda

1 GaN and Silicon structures

2 Qualification model for Infineon CoolGaN™

3 Key failure mechanism and degradation models

4 Summary

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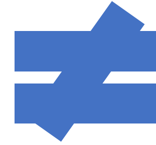
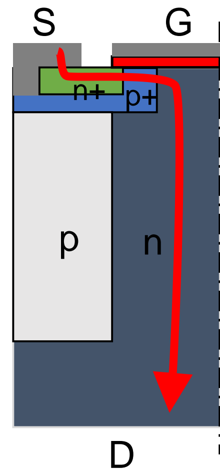
Why it is important to talk about GaN Quality and Reliability?

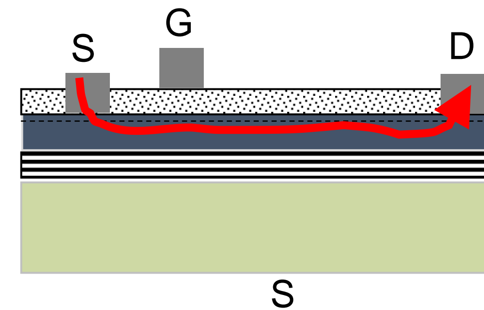
Si



GaN



Silicon Mosfet



GaN HEMT

- GaN HEMT structure is different in many aspects from Silicon MOSFET

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Product qualification standard Stress Tests, based on JEDEC JESD47

JEDEC applies ~9 different procedures based on
Stress type, Conditions, Duration and Sample size

Stress	Conditions	Duration	Sample Size
Temperature Cycling JESD22 A104	With PC*, -55 °C / +150 °C	1000x	3 lots x 77 pcs
High Temperature Reverse Bias JESD22 A-108	With PC*, 150 °C / 600 V	1000 h	3 x 77
High Temperature Storage Live JESD22 A-103	With PC*, 150 °C	1000 h	3 x 45
Positive High Temperature Gate Stress JESD22 A-108	With PC*, 150 °C / 50 mA	1000 h	3 x 77
Negative High Temperature Gate Stress JESD22 A-108	With PC*, 150 °C / -10 V	1000 h	3 x 77
High Humidity High Temperature Reverse Bias JESD22 A-101	With PC*, 85 °C / 85 % r.h. / 100 V	1000 h	3 x 77
Intermittent Operational Life Test MIL-STD 750/Meth.1037	With PC*, ΔT = 100 K	15,000x	3 x 77
ESD-HBM JS-001	Without PC	-	1 lot x 3 pcs per voltage level
ESD-CDM JS-002	Without PC	-	1 lot x 3 pcs per voltage level

*: Preconditioning acc. JEDEC-MSL3

Though many or most of these also apply to GaN devices, this cannot be considered as a sufficient list for consideration to qualify GaN devices!

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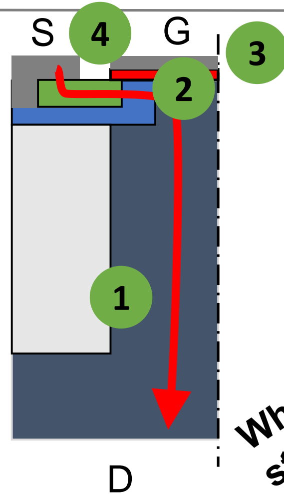
Qualification method must address the device/structure specific failure modes of GaN

Si MOSFET

Existing qual plan addresses mature Si technology/structure

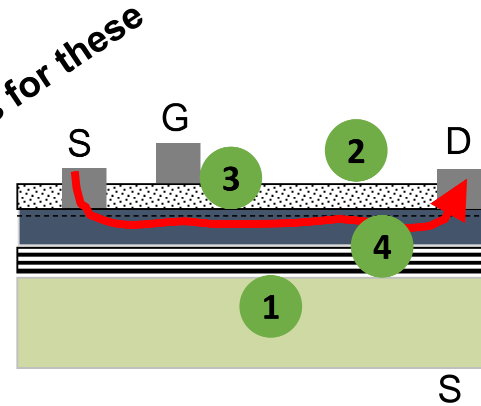


What are the correct stress tests for these structures?

1. p-n body diode and termination stressed during **HTRB**
2. Gate Oxide Dielectric stressed by **HTGB** test
3. Passivation and mould compound stressed by Temperature, Humidity and Bias (**THB**) and autoclave (AC) tests
4. Top Aluminum Metal and wire bonds stressed during temperature cycling **(TC)**

GaN HEMT

New Structure: what tests will stress them? Standards yet to be defined



1. Lateral device
2. Field terminates in active area
3. Non-insulated gate structure
4. Channel conducts through two dimensional electron gas (2DEG)

No p-n drain to source junction

Higher risk of humidity-induced corrosion

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How did Infineon determine a new qualification plan for 600 V CoolGaN™?

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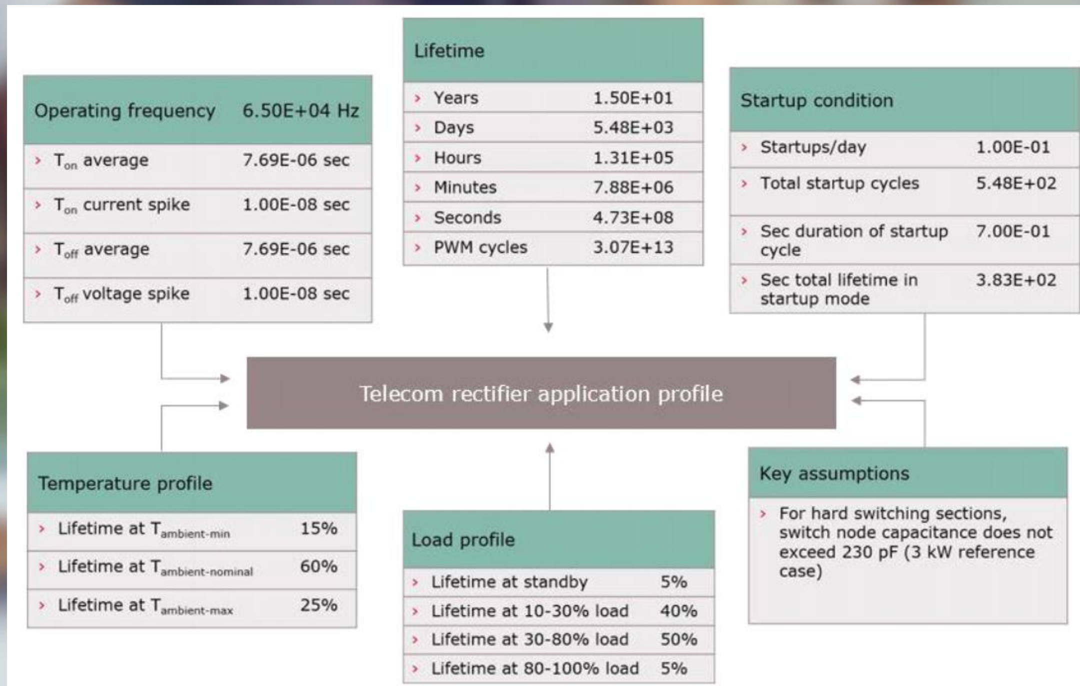
1. Application Profile

Application profile: typ use conditions in target applications

› Application lifetime
› Operating hours by mode
› Currents, voltages and temperatures at different load conditions
› Time of abnormal use conditions within lifetime
› Currents/voltages at peak and spikes during switching

1.
Application Profile

List of bias, time temperatures for both **normal and abnormal** operations



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2. Quality Requirement Profile

2.
Quality Requirement Profile (QRP)

Displays the development targets (Consumer/Industrial, FIT rates, Humidity specs,...) of a new technology or product in what concerns its reliability, performance and target applications

1. General definition of the target application
2. Definition of the product components
3. Maximum operation voltages and currents
4. Operation temperature range
5. Electro Static Discharge classification
6. Moisture Sensitivity Level class definition
7. Lifetime targets and failure rates for device, dielectrics and metallization
   - Drift limits parameter definition:
     - V_{th}
     - Drain leakage
     - R_{on}
     - Time to failure

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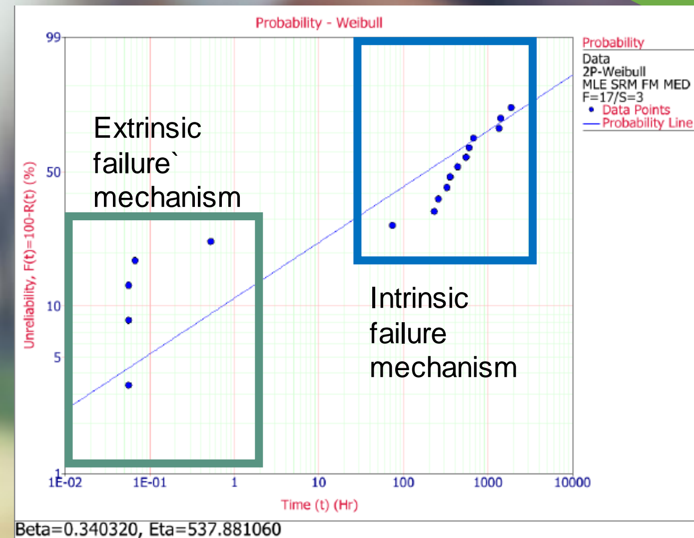
3. Reliability investigations during development

3.
Rel. investigation during development

Reliability investigations during development aims to discover ***intrinsic and extrinsic failure mechanisms***

Purpose: find path of process, design or test changes to *minimize occurence of extrinsic failures*



Early failures referred as **extrinsic** since their source is external to the real capabilities of the design and materials.

Later failures referred as **intrinsic** since they fail in a predictable manner at the physical limits of the intended device design and materials

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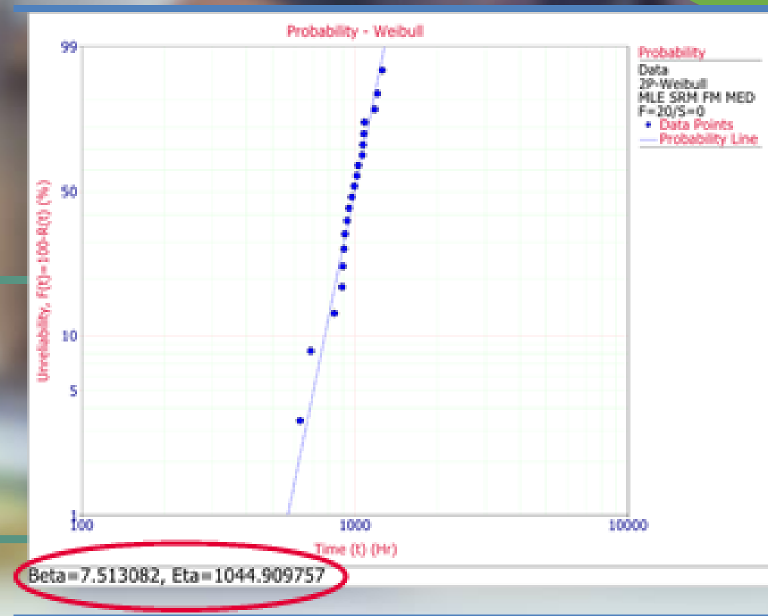
4. Degradation models for predicting reliability/lifetime

4.

Degradation Models

Degradation (failure models) allow use of short duration testing at accelerated conditions to predict lifetime at lower stress and longer time



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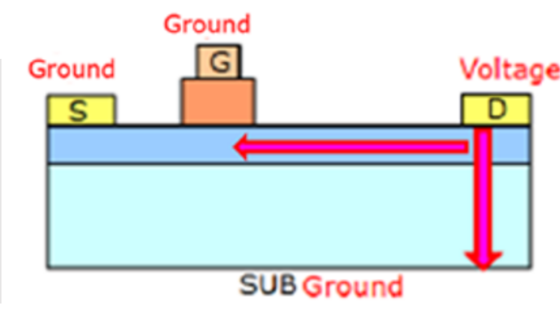
DC Bias Failure: TDDB

TDDB:

Time Dependent Dielectric Breakdown

Polar molecules lead to asymmetrical lattice distortion when subject to electric fields

Chemical bonds strain will break over time generating failure



Silicon

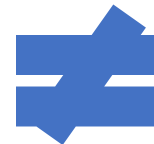
- Silicon-Silicon structure are not subject to TDDB
- Silicon-SiO2 and Si-other polar materials are subject to TDDB

GaN

- GaN is highly polar in nature, then subject to TDDB

Degradation of Silicon devices responds almost only to

Temperature



GaN devices respond strongly and primarily to temperature and **applied bias**

(accelerated voltage stress testing required)

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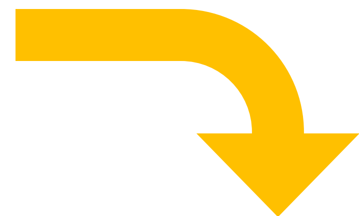
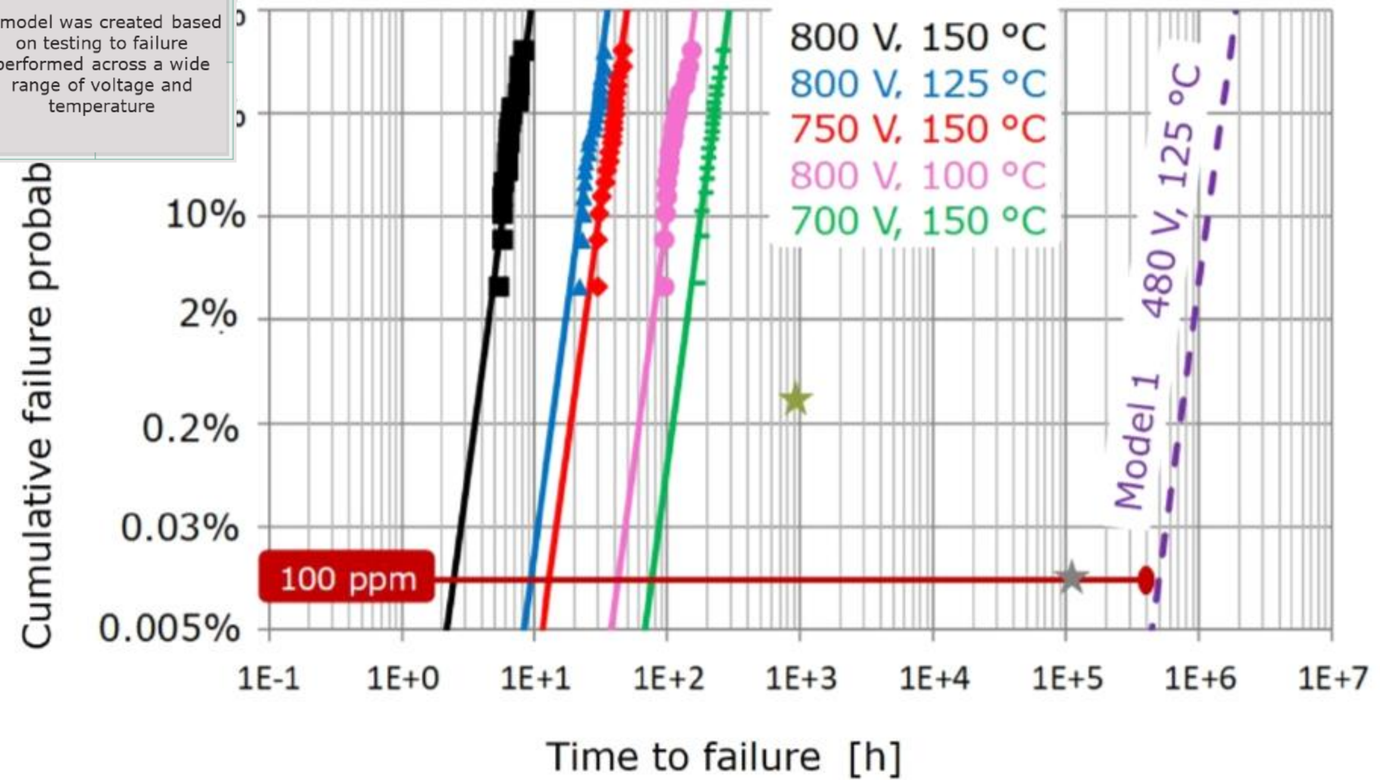
Weibull plots for Voltage/Temperature

Ground / Ground / Voltage / S / G / D / SUB Ground	Stress voltage		
	800 V	750 V	700 V
Stress temp. 150°C	√	√	√
Stress temp. 125°C	√	A model was created based on testing to failure performed across a wide range of voltage and temperature	
Stress temp. 100°C	√		





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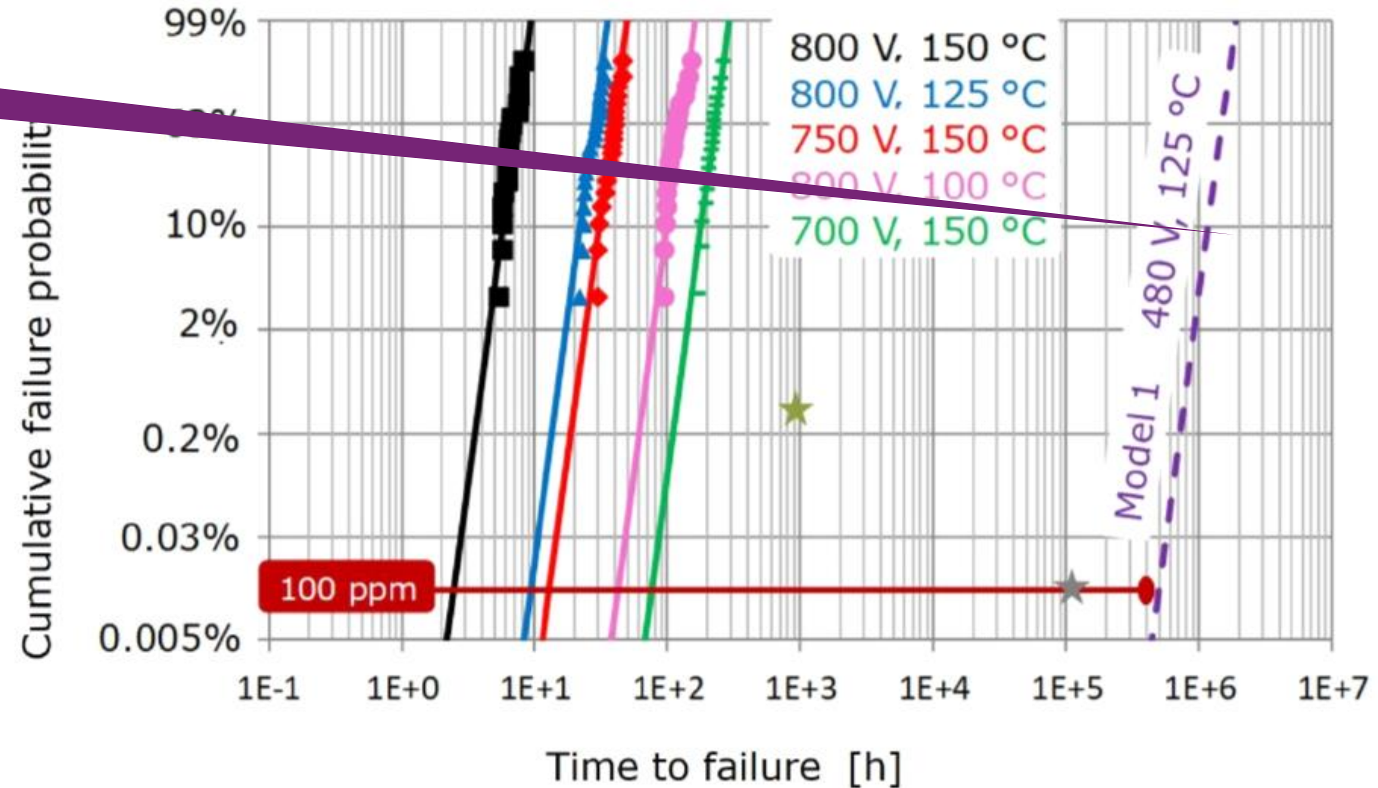
Weibull plots for Voltage/Temperature

Life Time Model at unified condition

$$L(t) = A * e^{-\gamma V} * e^{\frac{E_a}{kT}}$$



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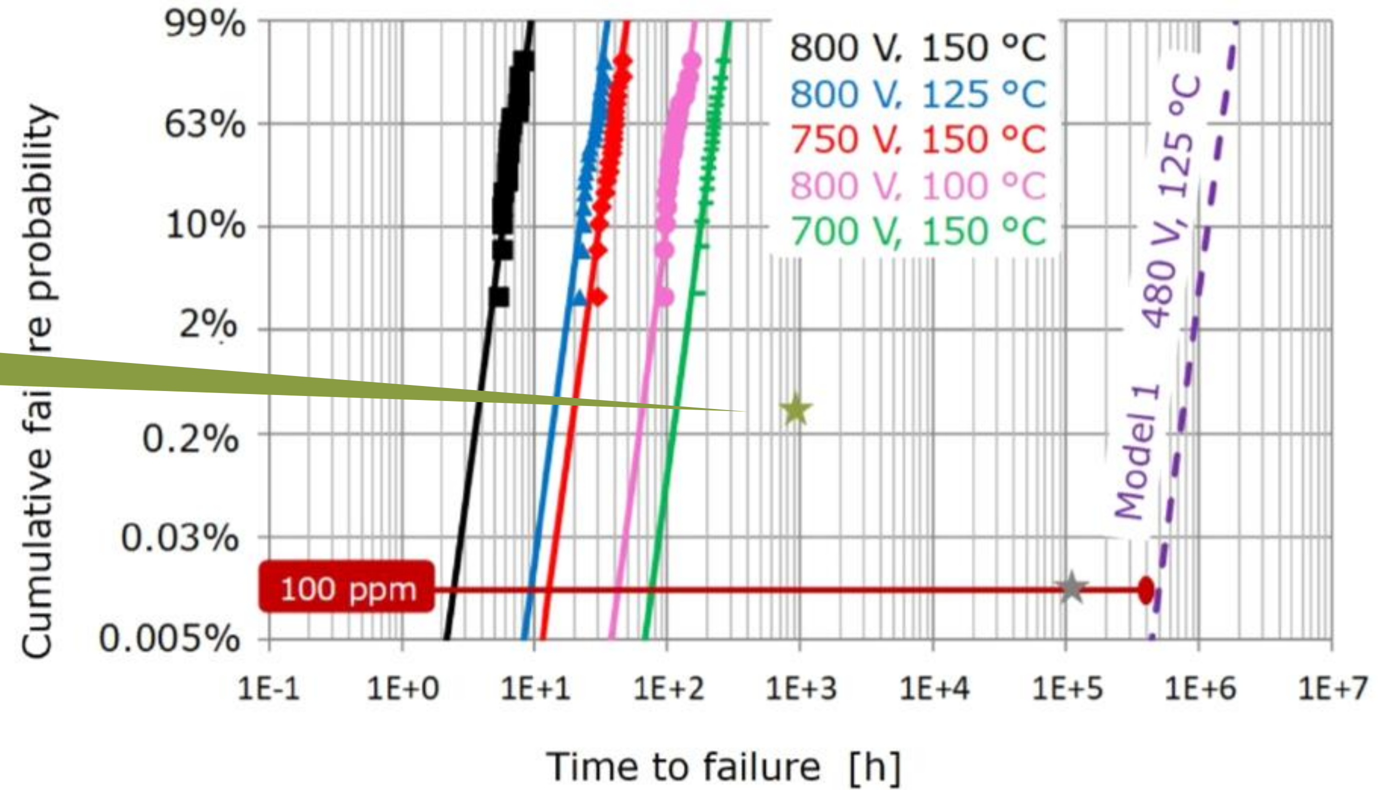
Weibull plots for Voltage/Temperature

JEDEC testing 3 x 77 parts, 480 V, 1000 h



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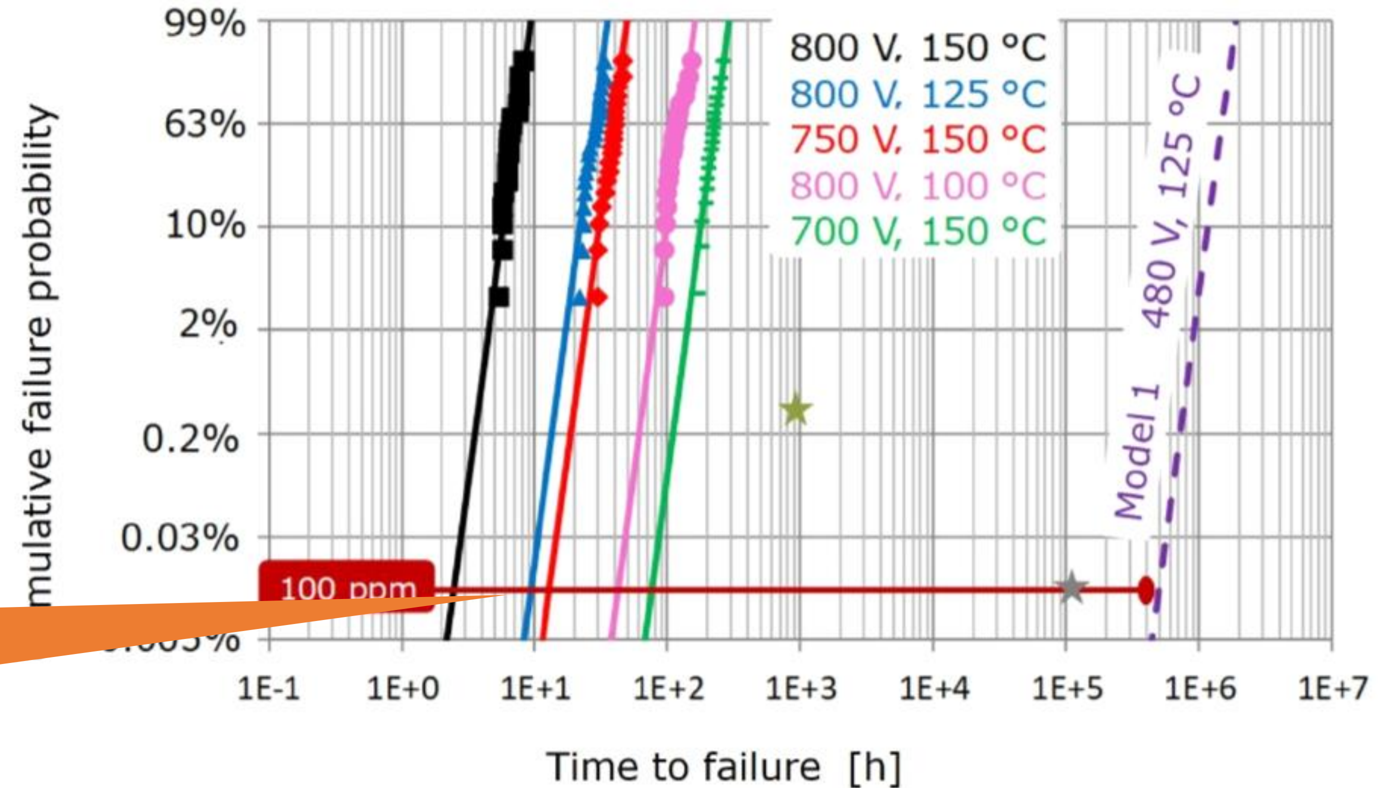
Weibull plots for Voltage/Temperature



Model shows 55 years lifetime vs requirement:
< 1 fit for 15 years
at 480 V, 125 ˚C
(131 ppm)

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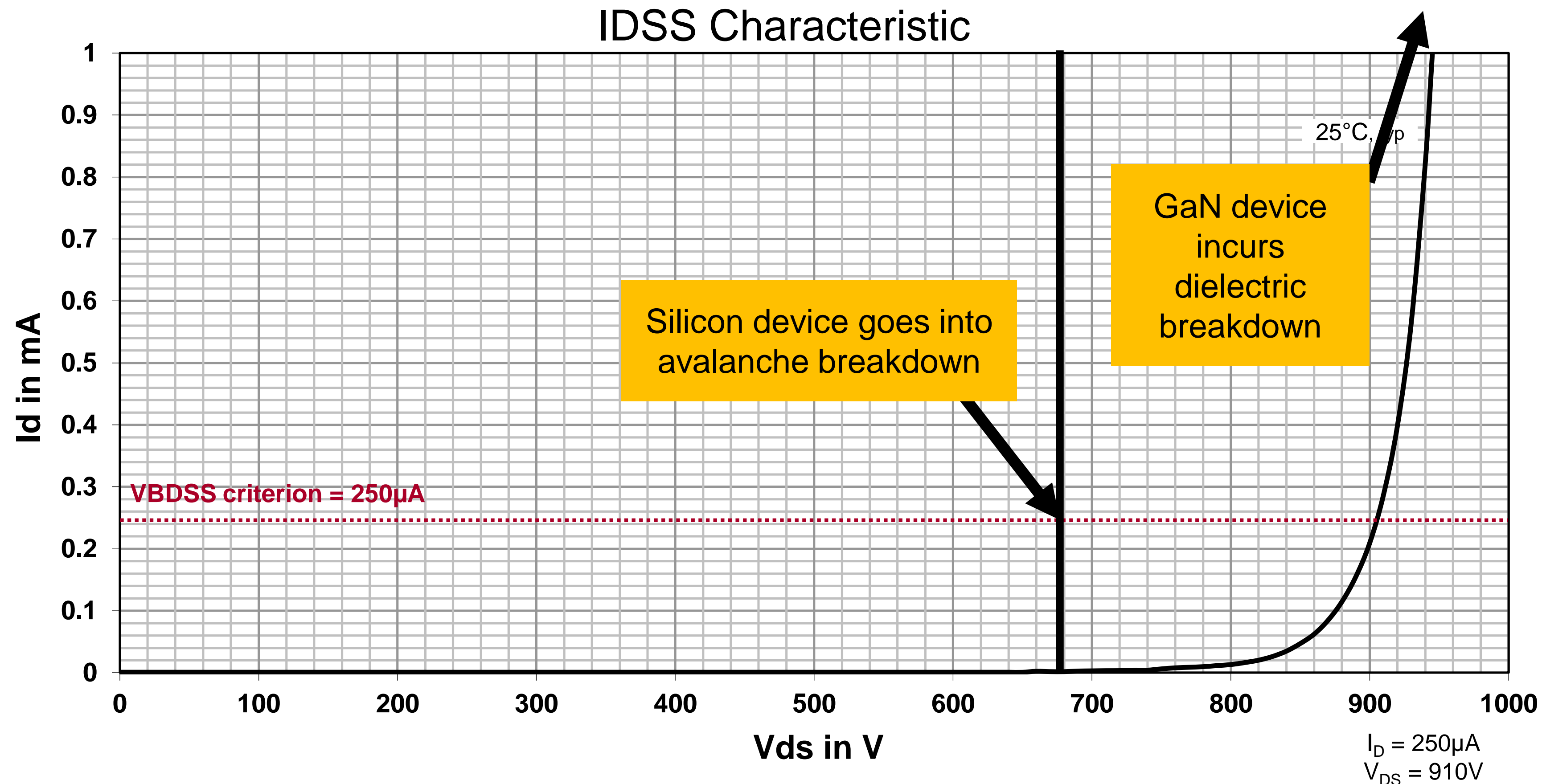
GaN Device breakdown at higher voltage than Si MOSFET but mechanism is different



- GaN can withstand much higher voltage stress than silicon
- …but lifetime at such high voltage is limited

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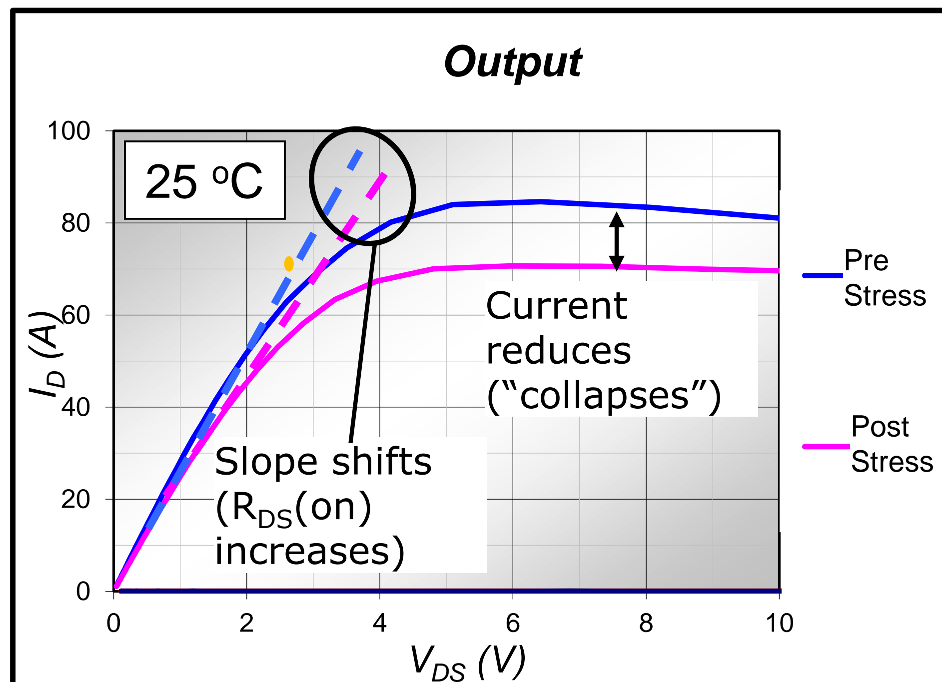
Dynamic Rdson

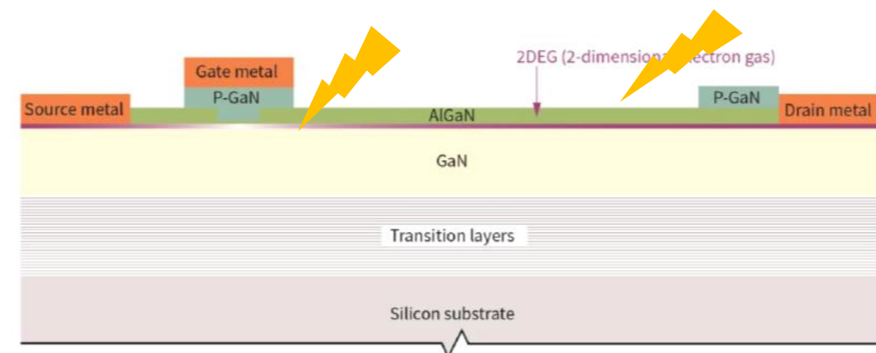
- Post application of DC bias Stress, RDS(ON) shifts (increases) and peak output current reduces.
- This phenomenon is attributed to surface states and trapping in the device
- ***The result is an unstable increase in conduction losses than can change in time (device could fail).***



- High voltage

Positive traps for 2DEG layer electrons

Generation of a temporary (dynamic) increase in conductivity



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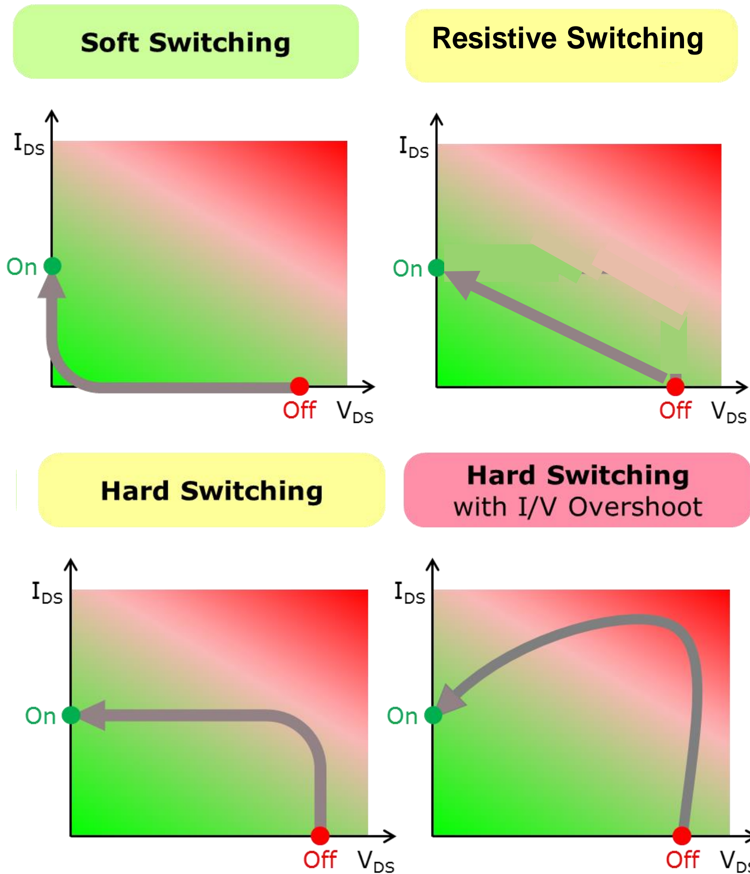
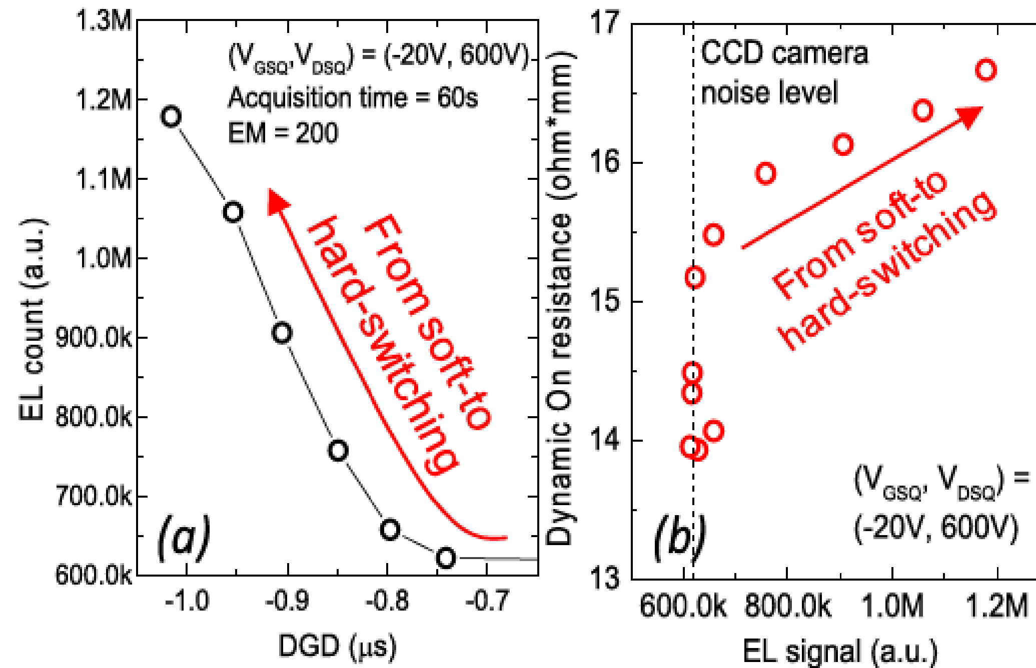
Dynamic R_{ds}ON shift increases with degree of hard switching : focus on the I,V locus





From: I. Rossetto et al, "Evidence of Hot Electron Effects During Hard Switching of AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 64, No, 9, September 2017

- Dynamic RDS(ON) increases with Electro-luminescence (EL) count –(proxy for hot electrons)
- Electro-luminescence increases with degree of hard switching (Higher peak I,V point)
- **Worst case Dynamic RDS(ON) occurs in hard switching (inductive load)**

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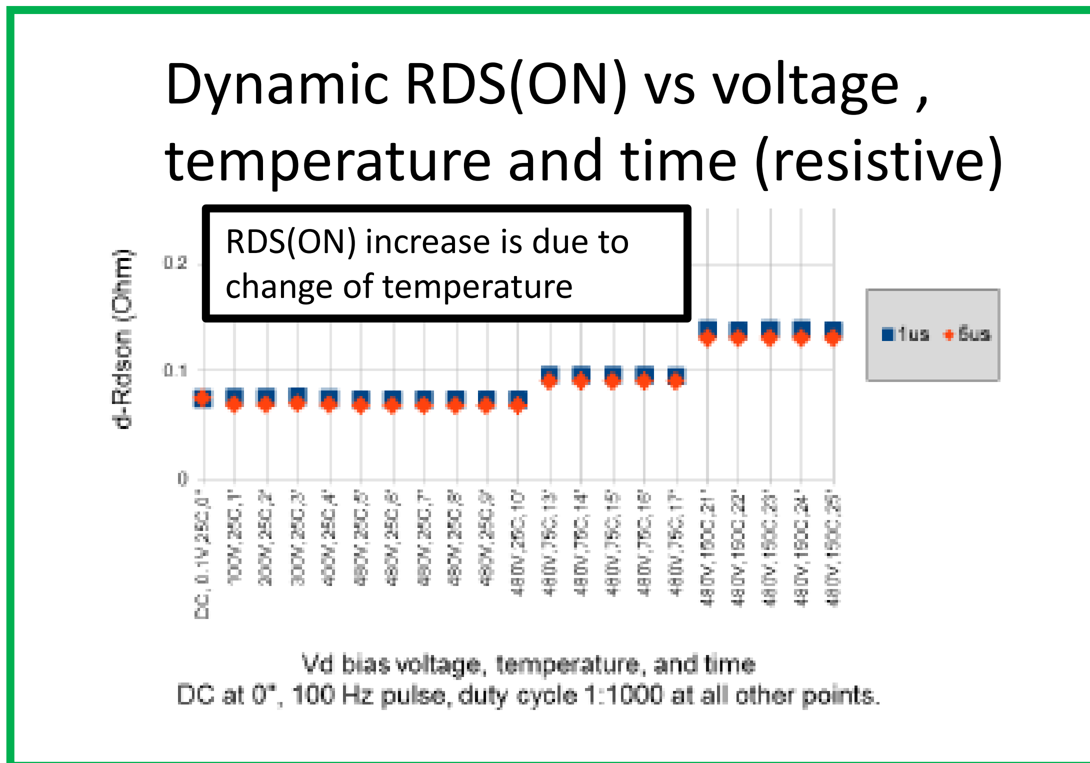
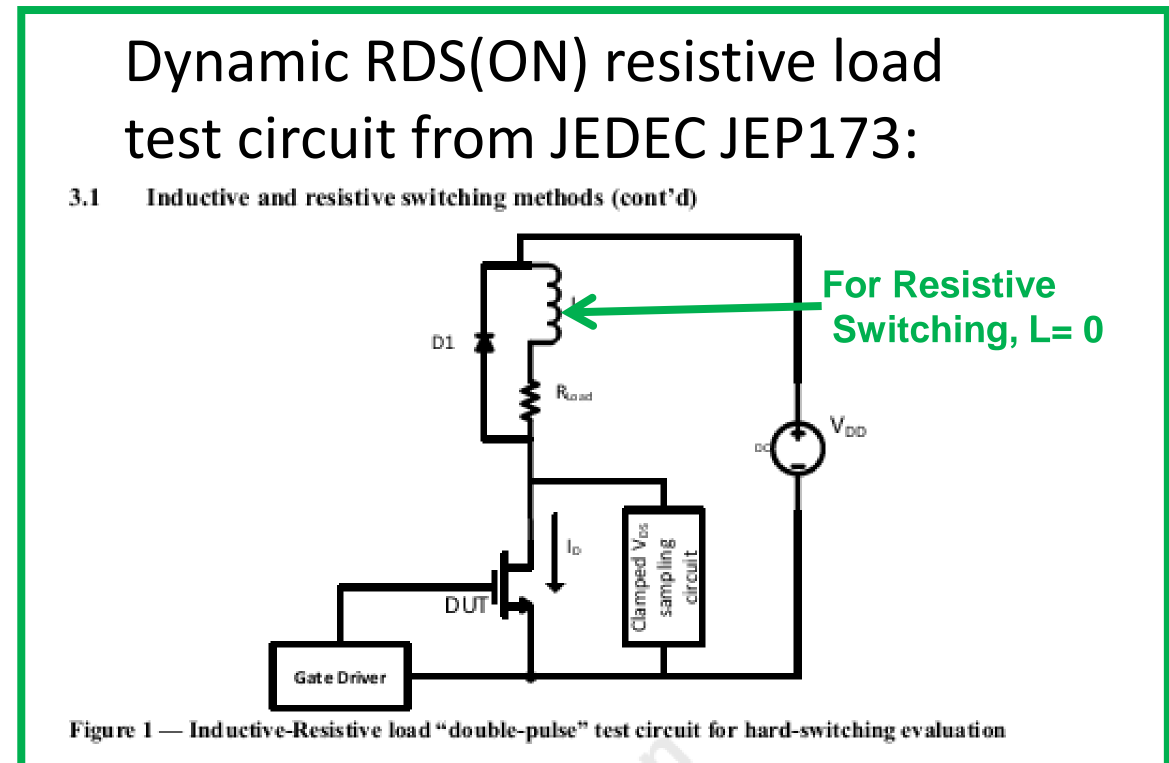
600V CoolGaN™ technology reliability dynamic R_{DS}ON over time – Very low in resistive load condition

Tested over voltage (from 100 to 480V) and temperature (from 25C to 150C)

RDS(ON) measured 1 and 5 microseconds after voltage stress ends

Stress held at 5 minutesTotal test duration = 1 hour and 40 minutes, little to no increase: resistive switching is not highest stress condition





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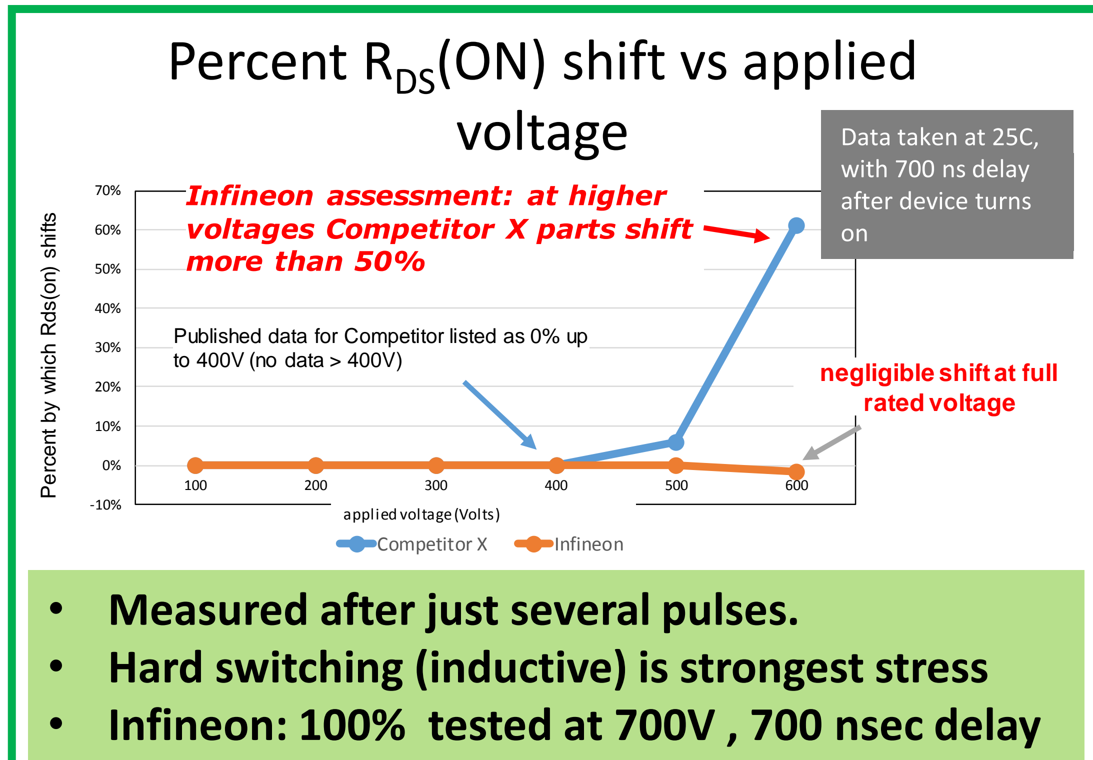
600V CoolGaN™ dynamic R_{DS}(ON) – also very low in (worst case) inductive hard switching out to 600V

- **Testing ramped voltage (from 100 to 600V)**
- **More hot electrons produced during hard switching at high simultaneous I,V (eg: inductive load)**
- **Most stressful test condition for dynamic R_{DS}(ON).**



- **Measured after just several pulses.**
- **Hard switching (inductive) is strongest stress**
- **Infineon: 100% tested at 700V , 700 nsec delay**

Dynamic R_{DS}(ON) inductive load boost test circuit from JEDEC JEP173:

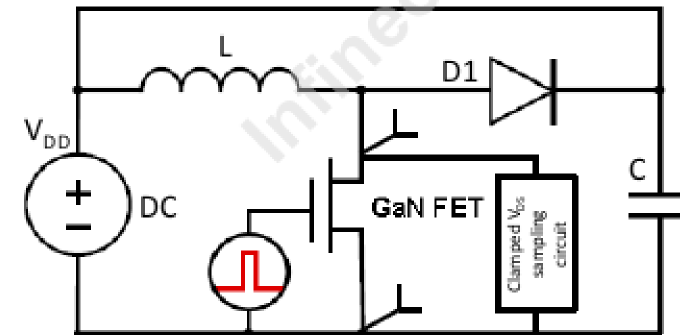


Figure 2 — Depiction of the hard-switching "double-pulse" test circuit (showing its similarity to a boost converter)

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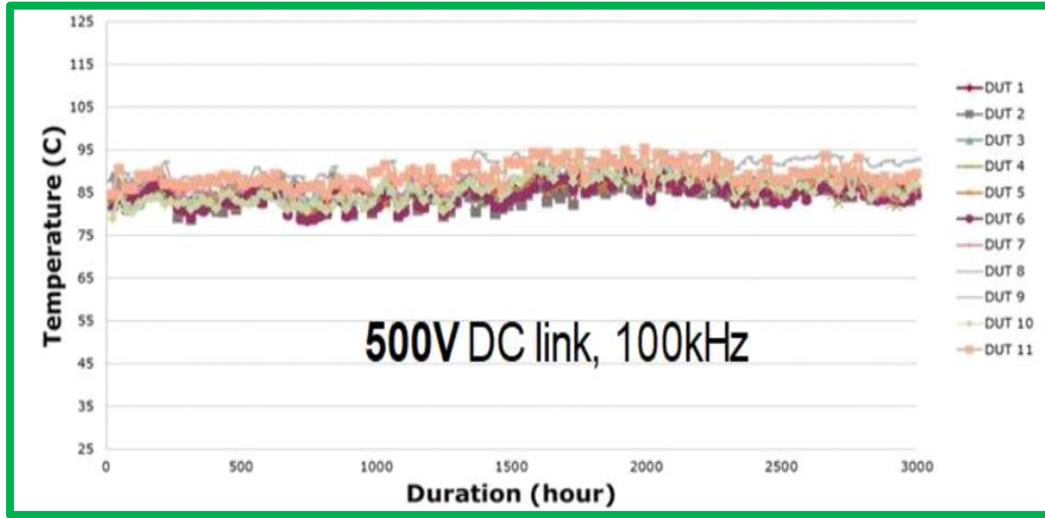
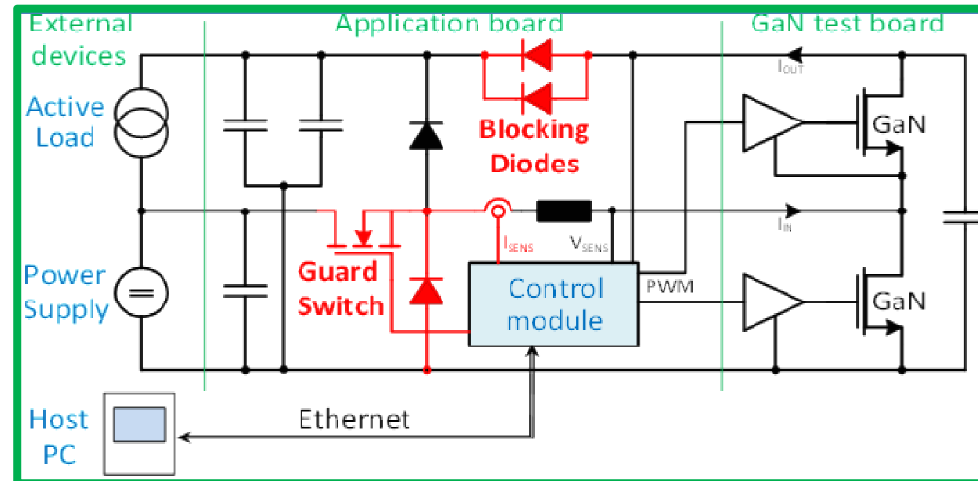
What about reliability of hard switching over time?



- 11 devices tested under boost (inductive load) hard switching topology
- 3,000 Hrs operation without evidence of increased power dissipation
- No evidence of shifting RDS(ON)
- Is **this test sufficient?**

- Infineon created an accelerated test vehicle
- Switching up to 700V (vs use at ~410V)
- High current and elevated temperature
- Switching related failures do occur at accelerated conditions: need for a model to predict useful life



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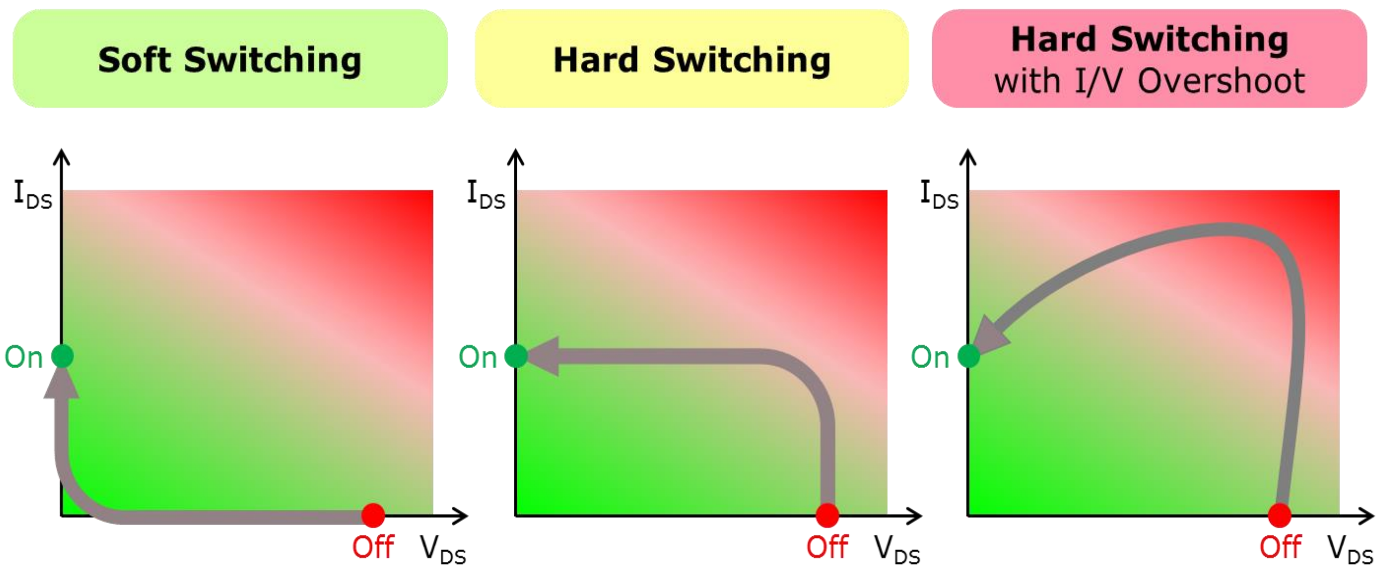
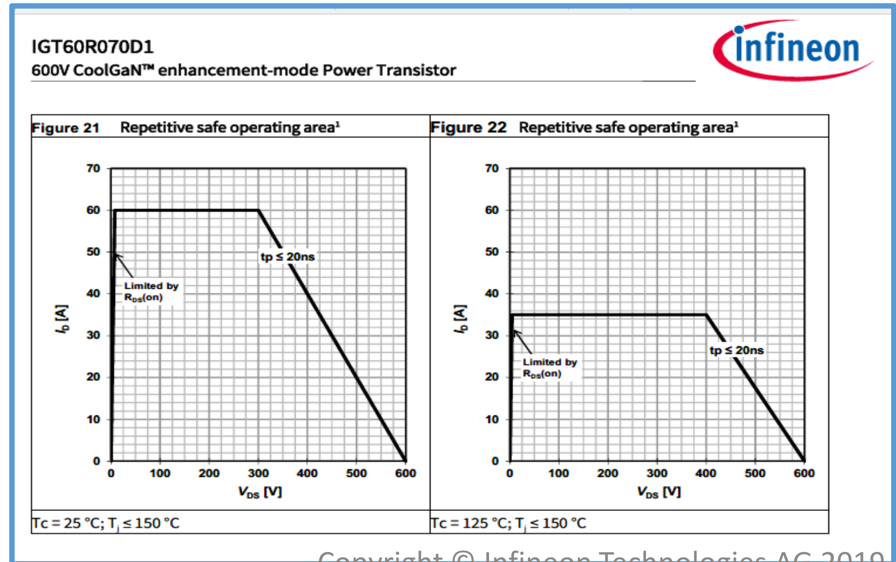
Results of repetitive switching-SOA (D-HTOL) degradation model





- Focus on the locus:
- No evidence seen that soft switching results in destructive failure in any usable timeframe (**caution: ZVS systems do operate some time in hard switching!)**
- Depending on I,V path, hard switching can result in ocurrence of the destructive repetitive switching failure over time
- This failure mode is different from dynamic R_{DS}(ON).
- CoolGaN^{TM} datasheets include repetitive switching SOA curves
- These curves detail hard switching operation limits to avoid premature destructive failure
- See details at www.infineon.com/gaN (go to «documents», «White paper»

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Summary

- GaN Devices have different material and device structure compared to silicon superjunction transistors; there is a need for a different qualification and reliability evaluation criteria
- Infineon has completed an application specific qualification with 4 elements which uses Telecom rectifier base station as the initial application (can be used to cover a wide variety of applications)
- There are failure modes which occur in GaN but not in silicon. Important among these is DC Bias and repetitive switching SOA. Infineon has developed models which ensure robust operation in targeted applications
- Full info available at : www.Infineon.com/gan

2 Gallium nitride - Reliability and qualification of CoolGaN™ › EN › CN
01_00 | 2018-10-31 | pdf | 2.3 MB

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Thank you!

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