Recent Advances in Embedded Capacitors

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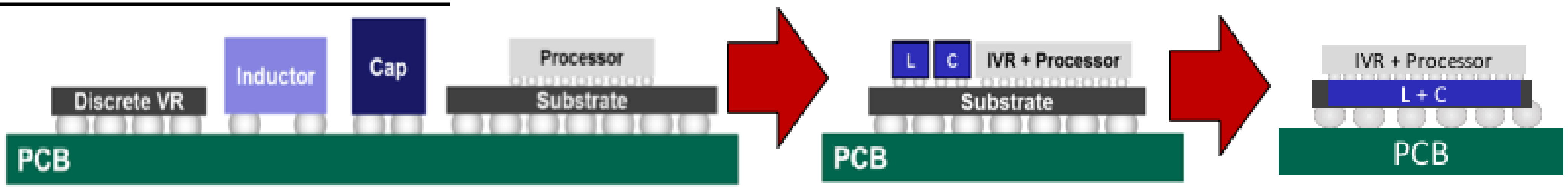
Outline

- Technology drivers
- Embedded Capacitor Technologies
  - Inserted MLCC
  - Embedded film capacitors
  - Silicon trench
  - Embedded electrolytic capacitors
- Roadmap projections
- Summary

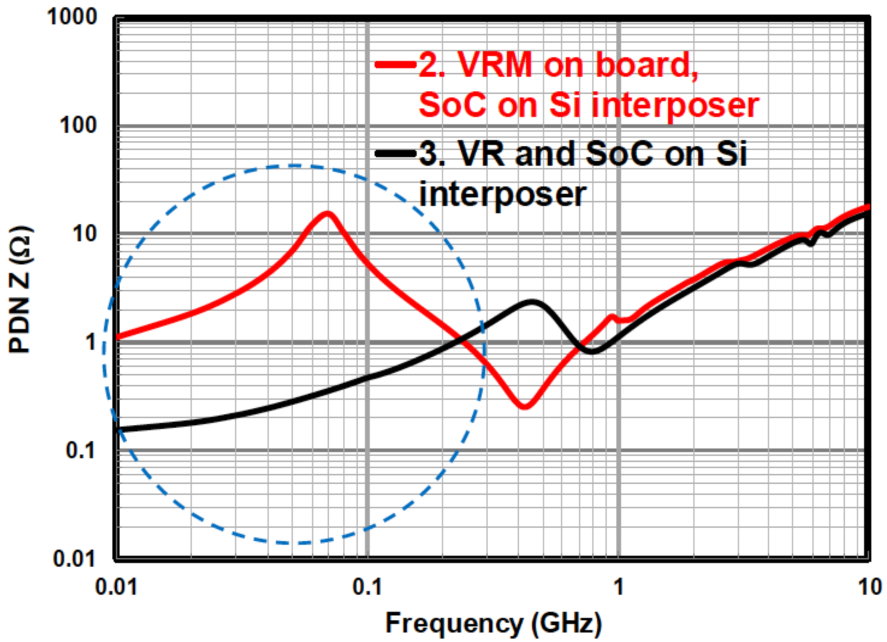
Why capacitor embedding?

System miniaturization

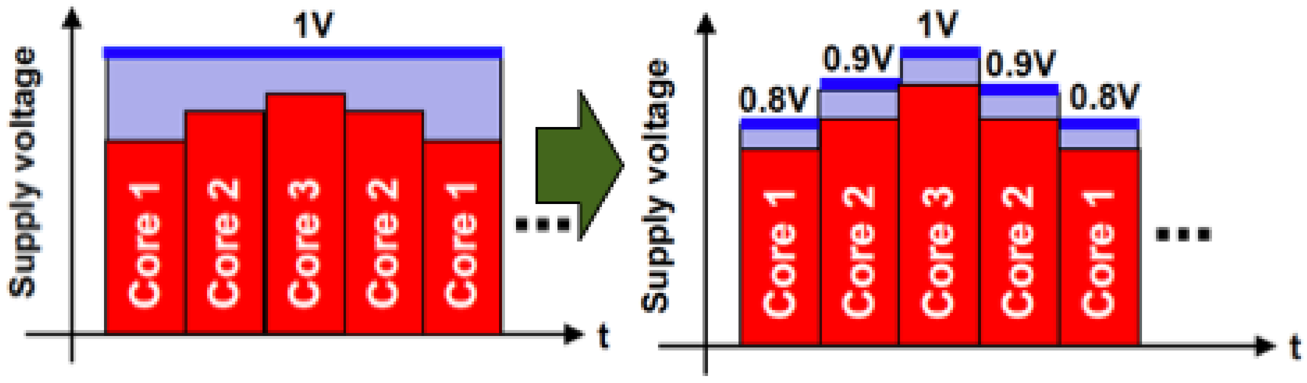


Reference: TSMC

Reduced impedance

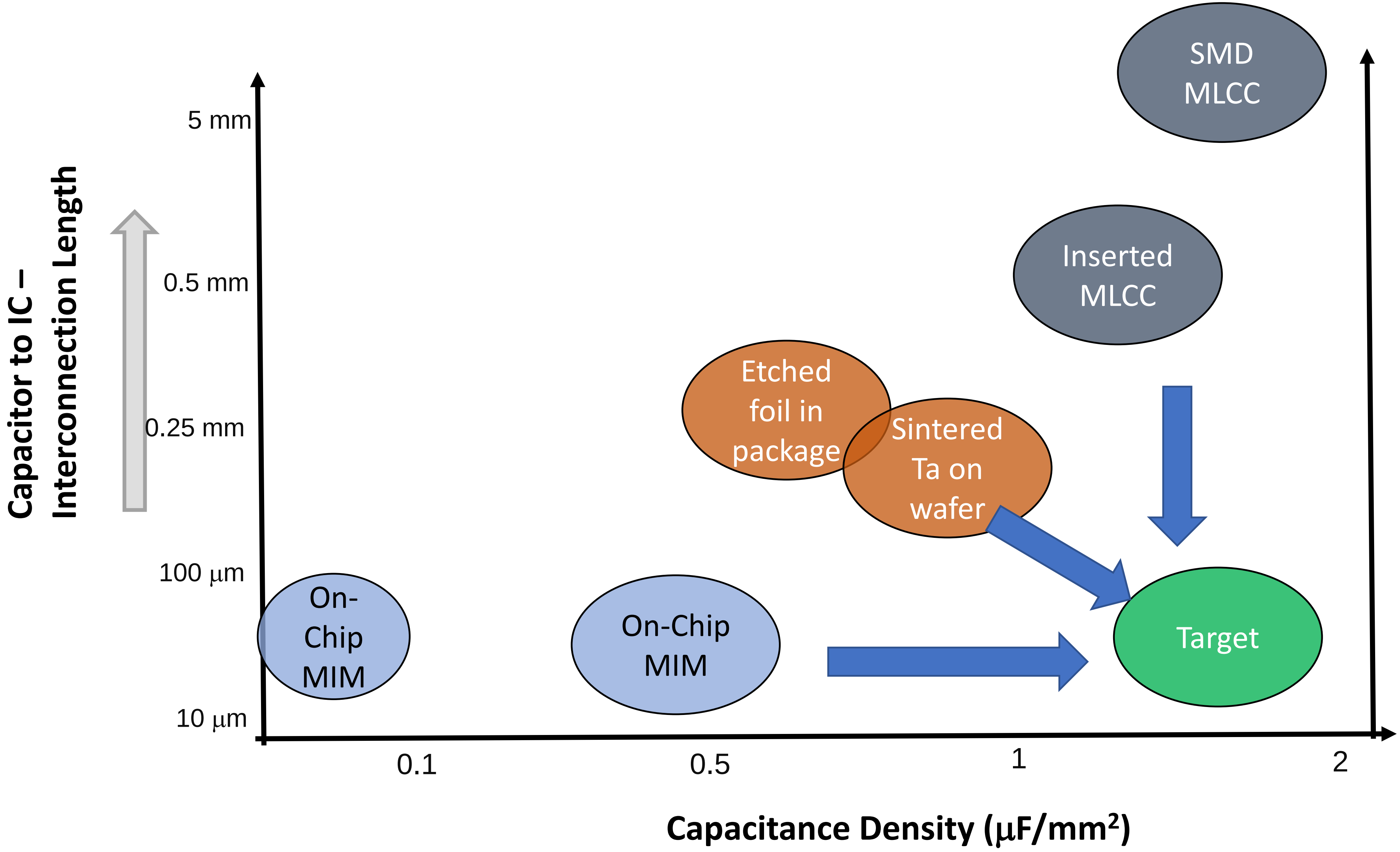


Granular power management



Reference: Harvard Univ

Trend to Embedded Capacitors



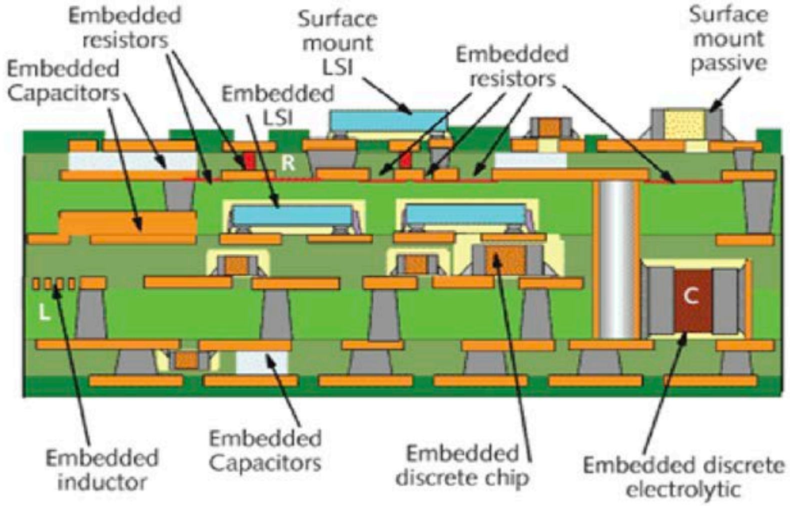
Challenges to Embedded Capacitors

Technology option	Challenges	This presentation
MLCC	• Availability in thin form factors; • Cu termination • Integration process • Reliability	I Part
Embedded film capacitors	• Not enough density	II Part
Trench capacitors	• Expensive processes	III Part
Etch foil or Ta electrode capacitors	• Thick electrode carriers • High ESR • Process integration • Reliability	IV Part

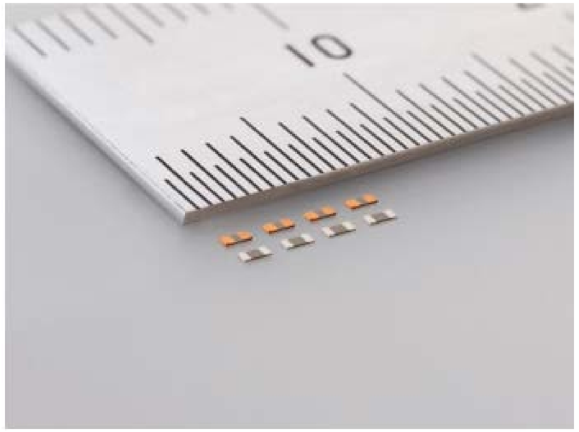
Inserted MLCCs

Inserted Ceramic Capacitors

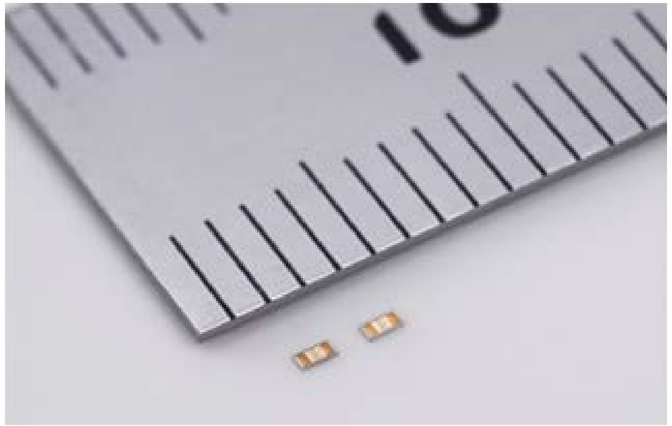
Embedding technologies (AVX)



Taiyo-Yuden

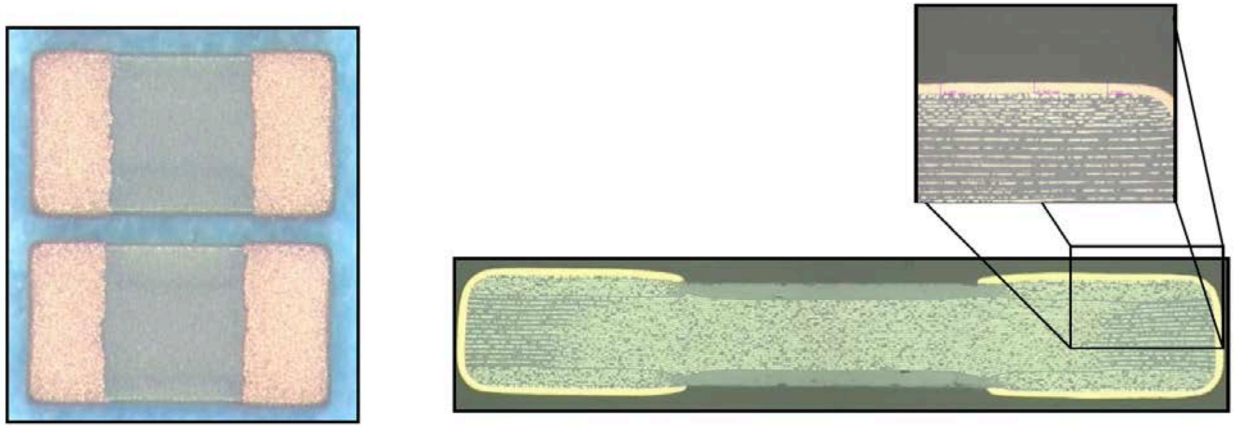


Murata

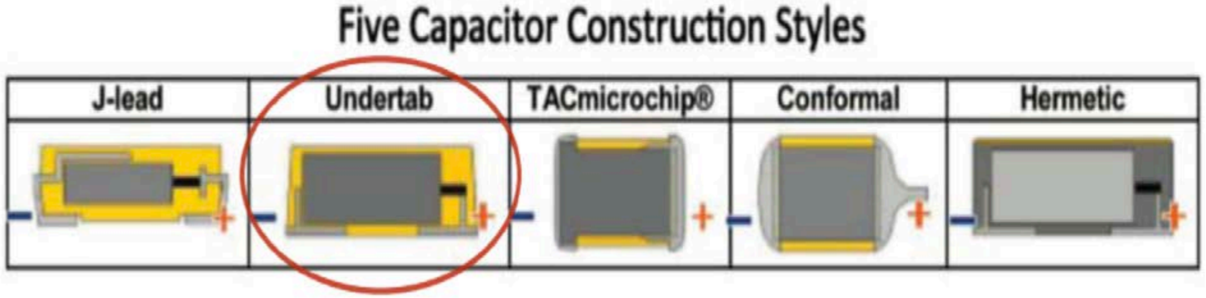


- Many companies offering low-profile discrete options
  - AVX down to 0.15 mm
  - Taiyo-Yuden down to 0.11 mm
  - Samsung down to 0.1 mm
  - Murata down to 0.05 mm
- Ultra-low footprints for fine-grain power management
- Single layer ceramics also available with lower density
- Copper termination becoming more common as trend towards embedding continues

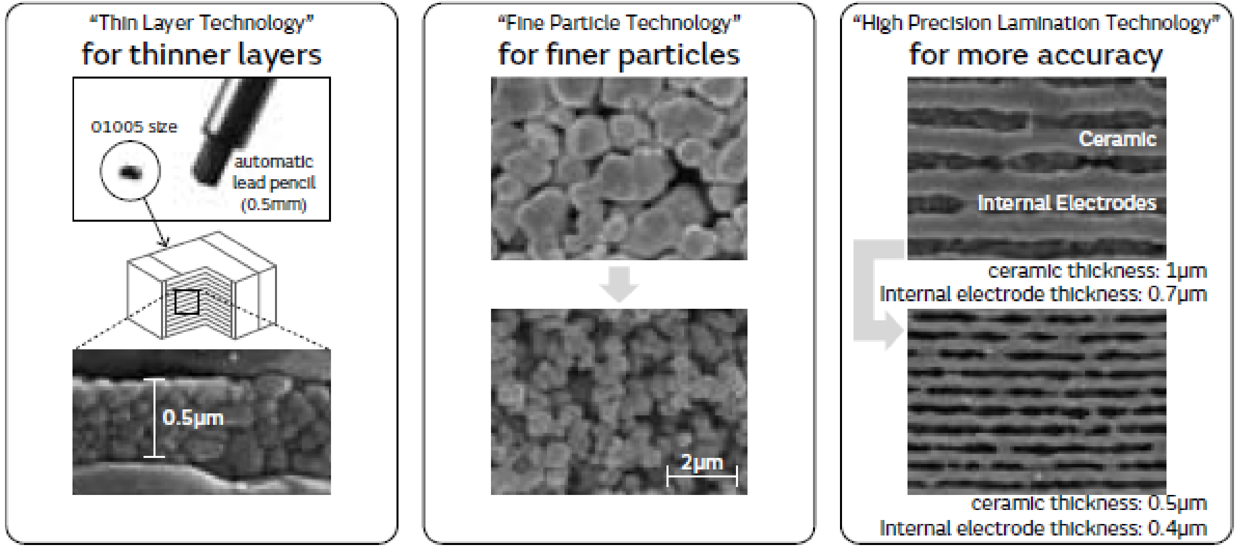
Key Enablers for Inserted MLCCs



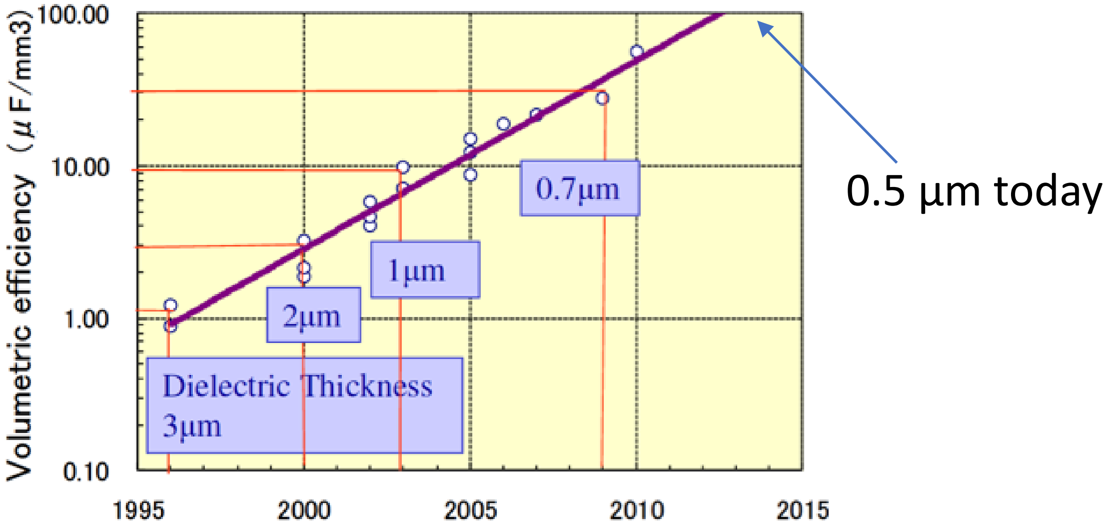
Fine copper termination (Source: AVX)



Efficient packaging and integration (Source: AVX)



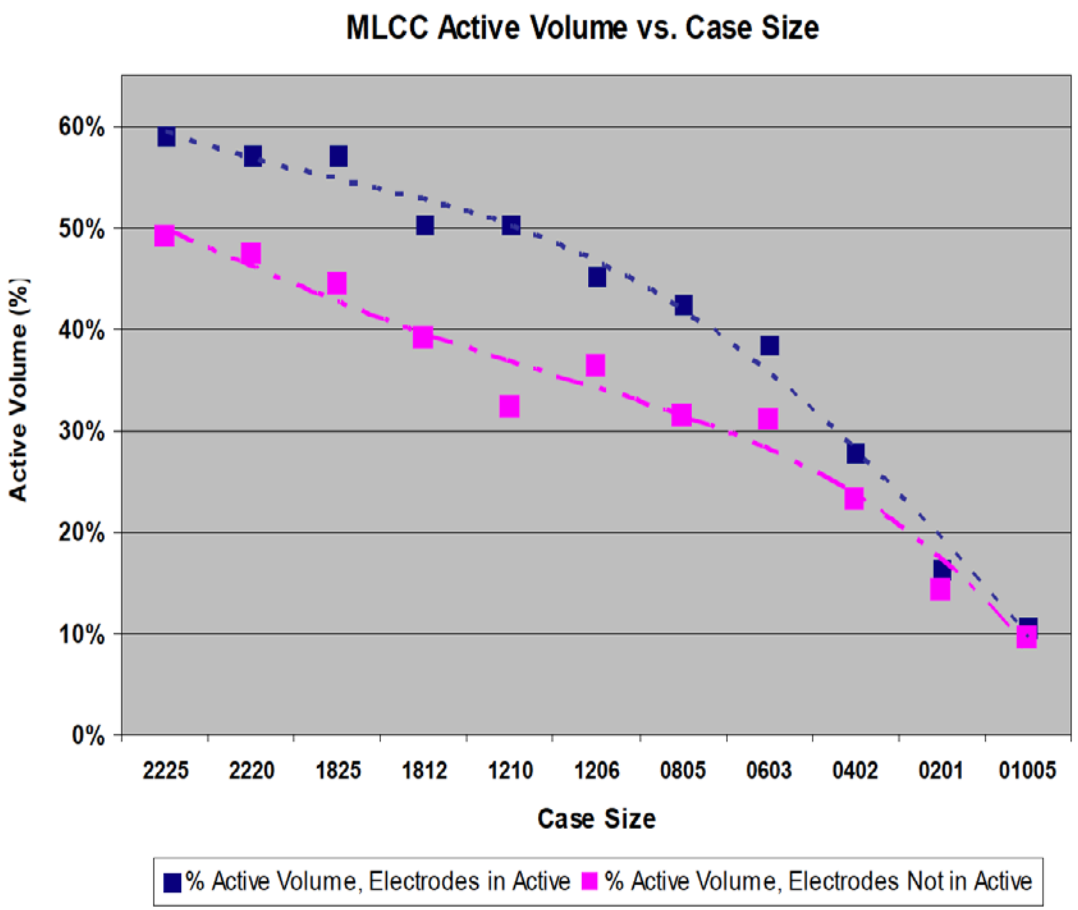
Thinner dielectric layers (Source: Murata)



Reduction in BST dielectric thickness with time (Source: Murata)

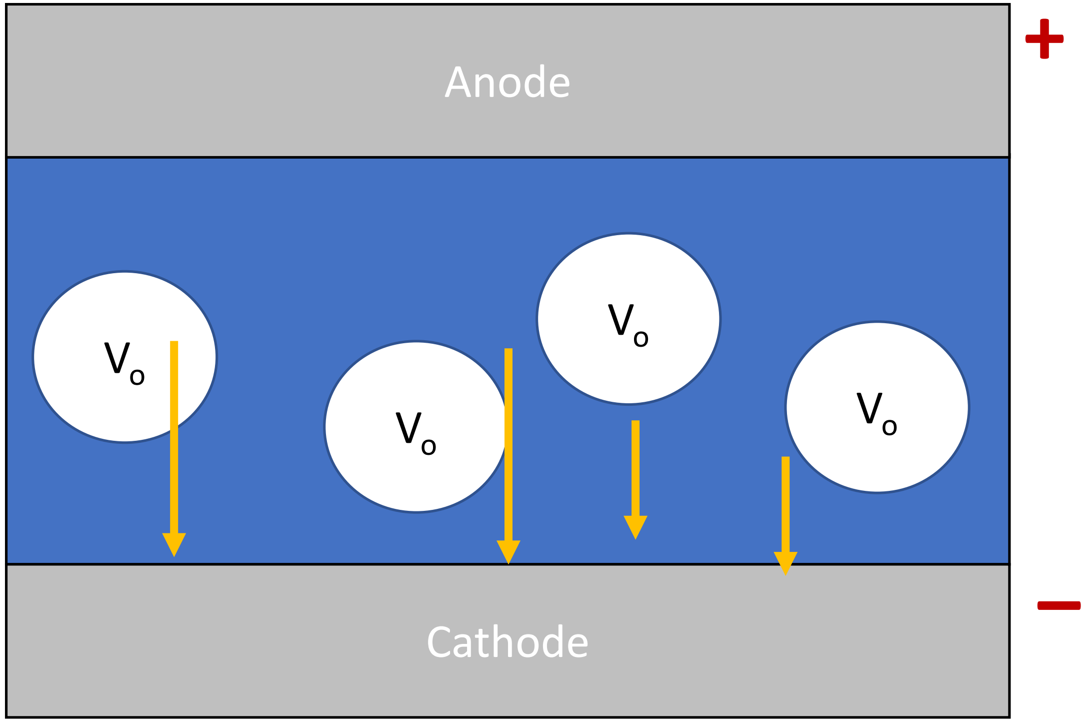
Barriers to achieve Thin MLCCs

Smaller components provide reduced volumetric efficiency



Source: InEMI 2013

Premature dielectric breakdown with thinner dielectric layers



High-temperature and high operation voltage:
2 microfarad/mm^2 with <150 micron thickness
T ~85
V < 6 V

Availability of Thin Inserted MLCCs

Thickness Footprint	0.5 mm	0.4 mm	0.3 mm	0.2 mm	0.1 mm	0.05 mm
0805 2x1.2mm						
0603 1.6x.8mm	10 µF -6.3 V (Murata, Samsung) 1 µF-25 V (Murata) 2.2 µF – 25 V (Samsung) 2.5 nF – 100 V (Murata)	1 µF-6.3V (TY)				
0402 1x.5mm	10 µF – 4 V (Samsung) 2.2 nF - 250V (KEM) 10 nF – 50V (TDK) 2.2 µF - 10V (Murata) 2.2 µF – 4-25V (AVX)	4.7 µF– 6.3 V (Samsung)	.1 µF-50 V (TY) .47 µF-16V (TY) 1 µF – 10V (Murata) 2.2 µF – 6.3V (TDK) 2.2 µF-6.3 V (Samsung)	.1 µF – 10V (TY) 1 µF – 4-6.3 V (TY, Murata) .47 µF-6.3V (Samsung)	.1 µF-6.3 V (Murata) .22 µF-6.3 V (TY) .47 µF – 2.5 V (TY) .22 µF-4 V (Samsung)	.1 µF-4 V (Murata)
0201 .6x.3mm	4.7 µF – 4-6.3 V (Murata)	2.2 µF-6.3V (AVX) 1 µF-10 V (AVX, TY)	1 µF - 4-6.3 V (Murata, Samsung) .47 µF-6.3 V (Samsung) 1 µF - 10 V (Murata) 10 nF – 25V (Yageo) 1 nF – 50 V (NovaCap)	.1 µF-4V (TDK) 10 nF – 10 V (Samsung)	.1 µF -6.3 V (AVX) .1 nF-50 V (Knowles) .22 µF – 6.3 V (TY)	10 nF-4V (Murata)
01005 .4x.2mm			.1 nF-100V (ATC) 0.22 µF – 4 V (Murata)	.1 µF – 2.5-6.3 V (Murata, AVX) 1 nF – 6.3-10 V (Samsung)		
008004 .25x.125 mm					10 nF-6.3V (TY) 1 nF-16V (TY) 10 pF – 25 V (TY) 1 nF-6.3 V (Murata) 10 nF-4V (Murata) 9.9 pF-25 V (Kyocera)	

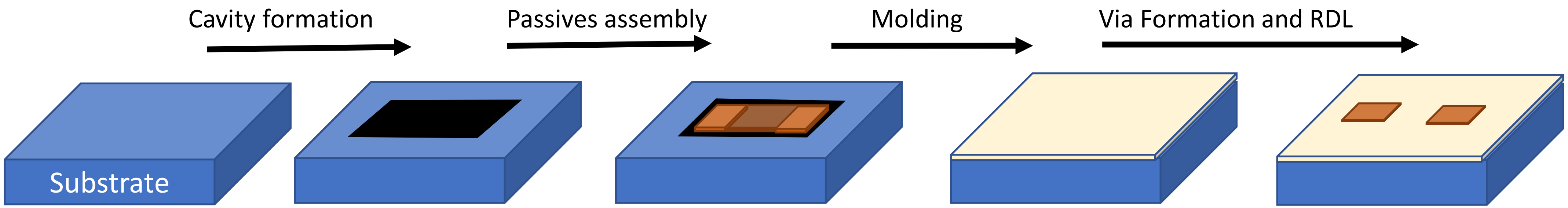
Availability of Thin Inserted MLCCs

Thickness Voltage	0.5 mm	0.4 mm	0.3 mm	0.2 mm	0.1 mm	0.05 mm
1-3 V					0.94 µF/mm^2	
4-5 V	20 µF/mm^2	8 µF/mm^2	6 µF/mm^2	2.75 µF/mm^2	.44 µF/mm^2	.2 µF/mm^2
6-10 V	8 µF/mm^2	8 µF/mm^2	4.4 µF/mm^2	2 µF/mm^2	.44 µF/mm^2	
11-25 V	2 µF/mm^2		.1 µF/mm^2		.03 µF/mm^2	
26-50 V	20 nF/mm^2					
51-100 V						
>100 V	5 nF/mm^2					

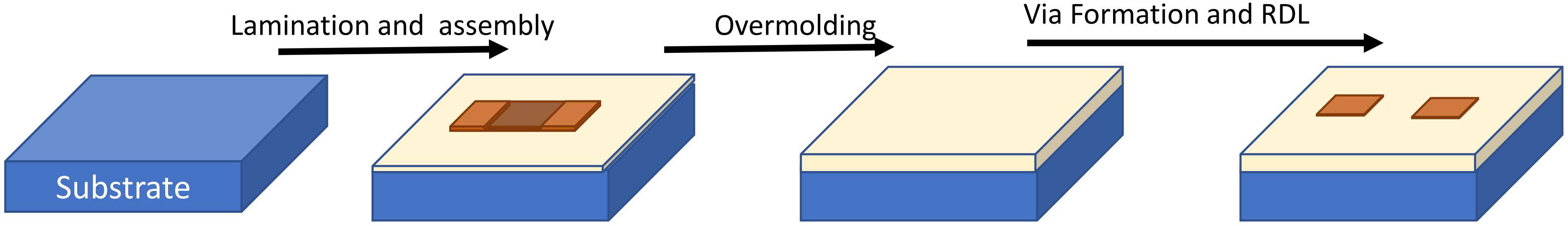
- High-density options using mostly X5R dielectric (only up to 85° C with strong dependence on temperature)
- Temperatures higher near IC
  - Need to reduce thickness of more temperature-stable dielectrics
  - Thermal management is critical

Functional Substrate Using Inserted Discrete Capacitors

Method 1: Cavity insertion

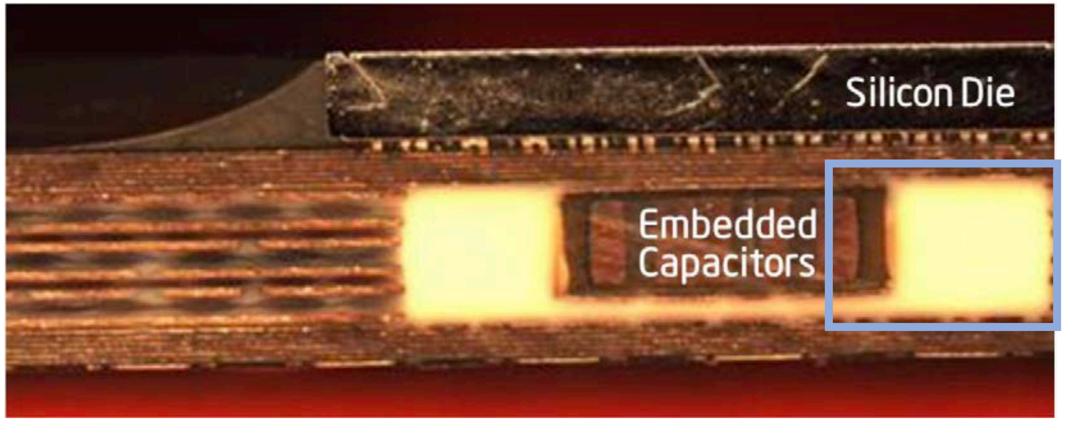


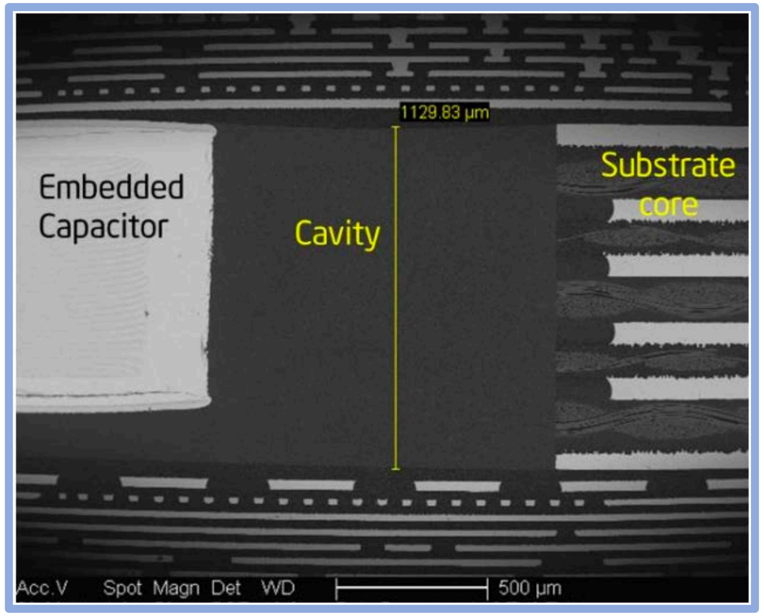
Method 2: Overmolding

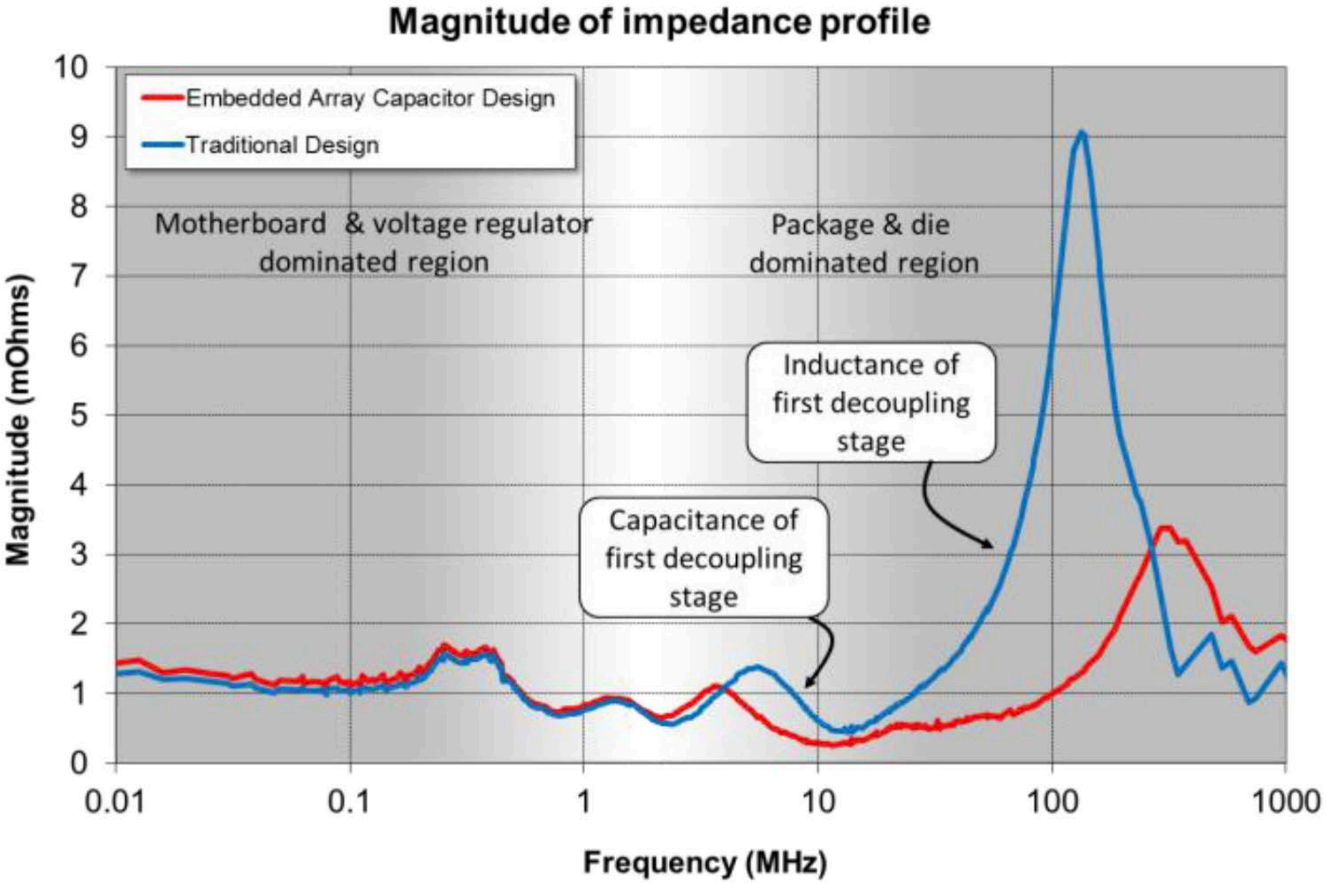


Result: Power-on-package solution

High-Frequency Decoupling with Inserted Caps





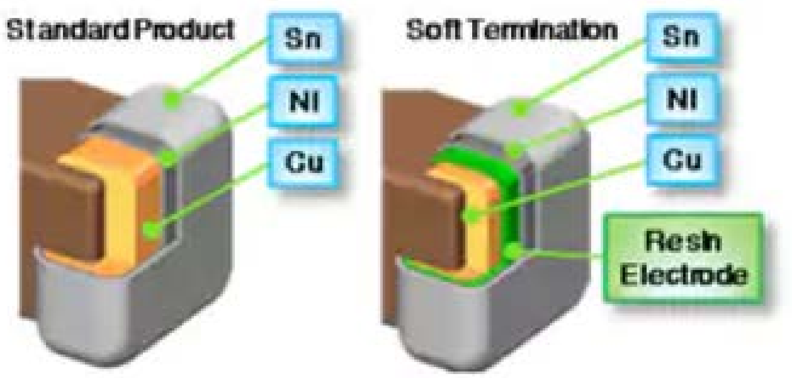


Min, Y., Olmedo, M.H., Radhakrishnan, K., Aygun, K., *Embedded Capacitors in the Next Generation Processor*, in *Electronic Components & Technology Conference*. 2013.

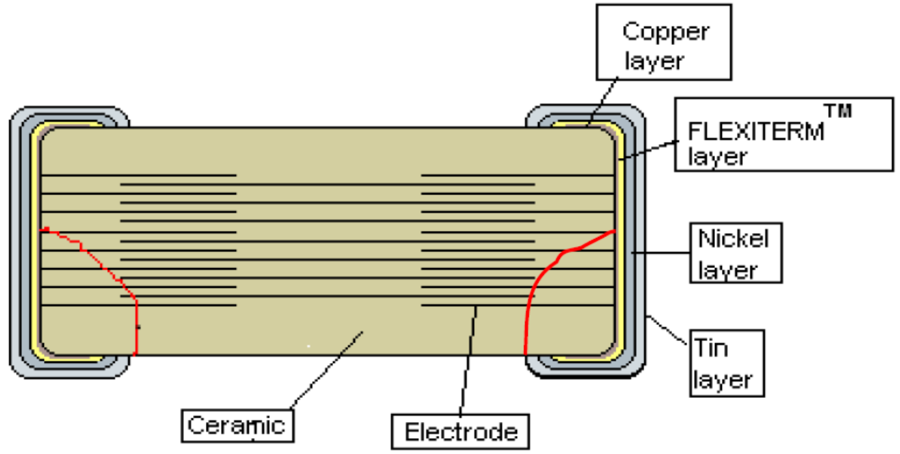
Reliability Considerations

- Aggravated reliability concerns with embedding
  - Susceptible to cracking due to CTE mismatch
  - Higher ambient temperatures near IC
  - Failure more expensive due to disposal of entire substrate with passive

- Critical parameters for reliability
  - CTE matching
  - High Flexural strength
  - Operating lifetime data under accelerated conditions



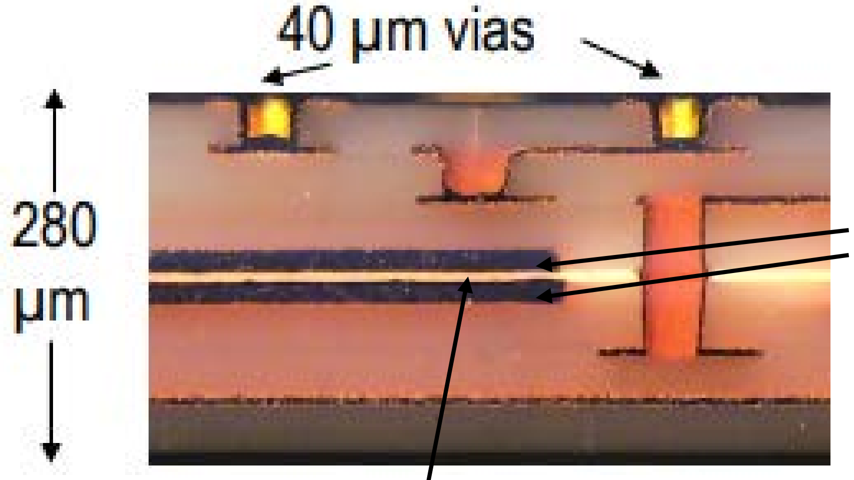
Stress-absorbing soft termination (TDK)



Open-mode failure with floating electrode design (AVX)

Formed Film Capacitors

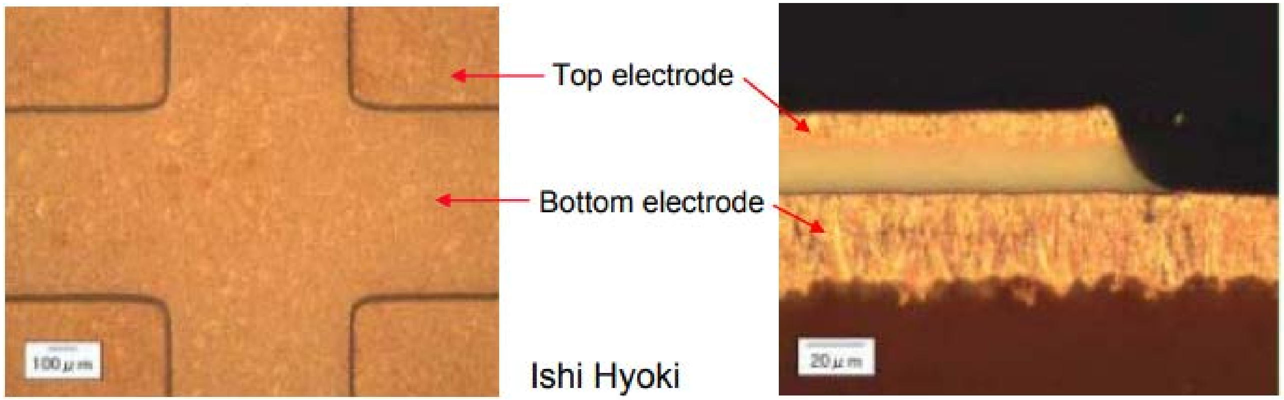
Polymer Film Capacitors



Embedded capacitor core

3M. *Electrical Performance, Miniaturization and EMI Advantages of Very High Capacitance Density Laminates in PCBs and IC Packaging*. in *PCB West*. 2011. Santa Clara, CA.

- Polymer laminates with ferroelectric fillers
- Can achieve dielectric constants of 20-30
- Up to ~ 6 nF/cm^2 for thinner layers
- Capacitance limited due to epoxy matrix
  - Therefore, mainly for high frequency filtering applications

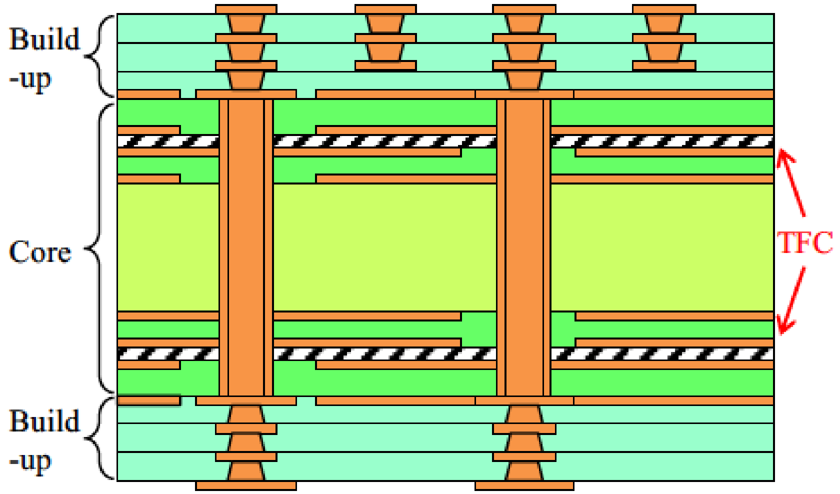


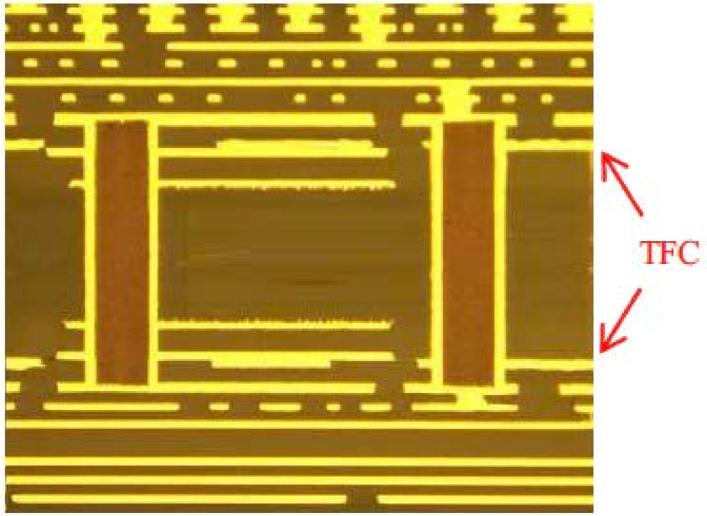
Patterned laminates from Oak-Mitsui

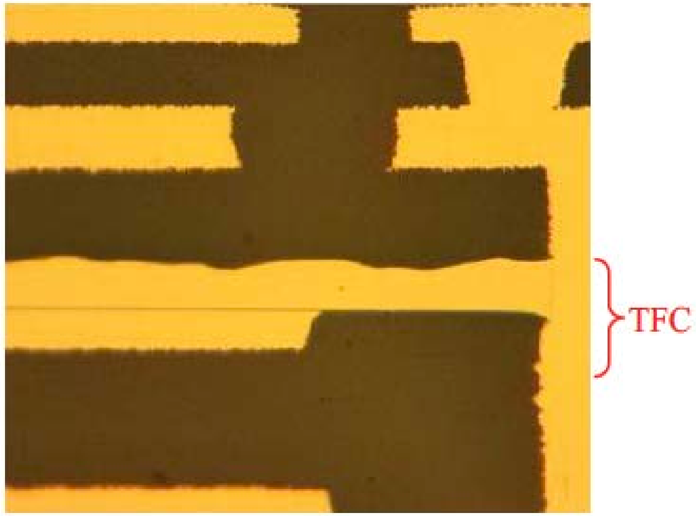
Characteristics	Condition	Unit	*BC16TR*
Capacitance	1MHz	pF/cm^2	1,700
Dk	1MHz	N/A	30
Df	1MHz	N/A	0.019
Dielectric Thickness	Nominal	Micron Meter	16
Peel Strength	IPC TM-650 2.4.9	kN/m	>0.7
Thermal Stress	20sec @288C	times	>10
Electrical Migration	85C/85%RH/ 35V	hrs	>1000

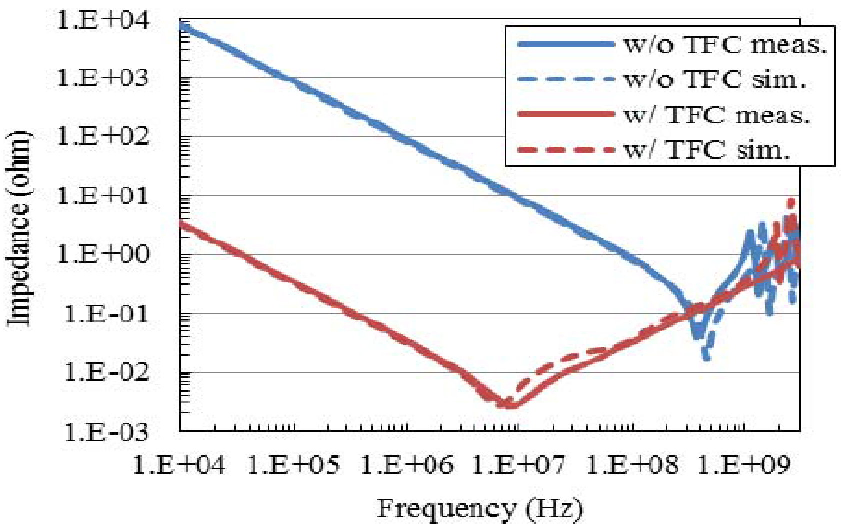
General characteristics of high D_k film

Formed Ceramic Film Capacitors





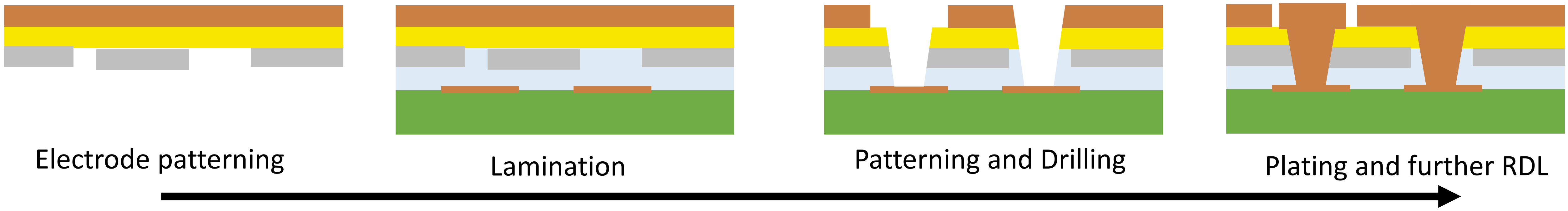


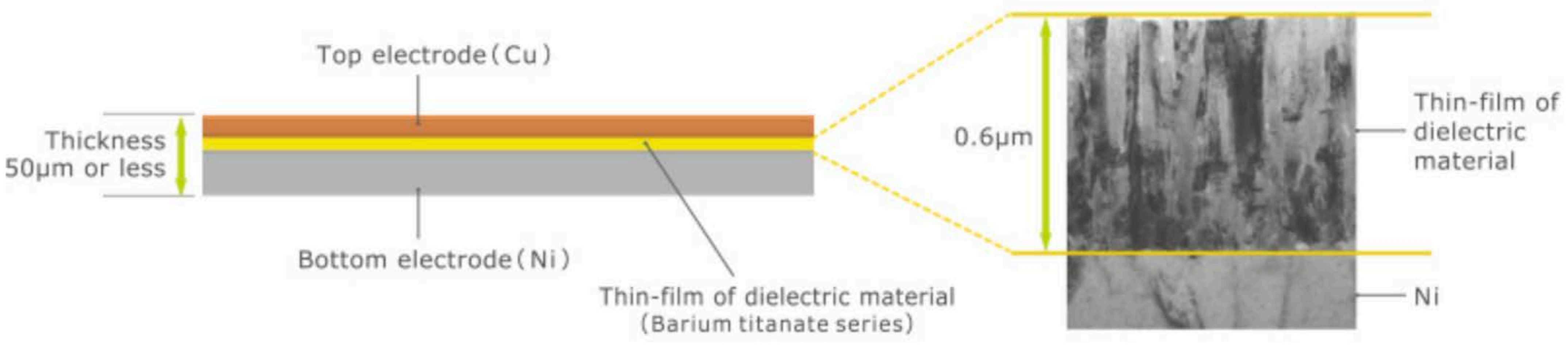


- Fujitsu BGA Package using TDK TFCs
  - 50 µm thick
  - 1 µF/cm^2
  - <0.1 loss
- Significantly reduced impedance up to ~300 MHz with addition of thin-film capacitor (TFC) layers

Akahoshi, T., et al., *Development of CPU Package Embedded with Multilayer Thin Film Capacitor for Stabilization of Power Supply.* 2017: p. 179-184.

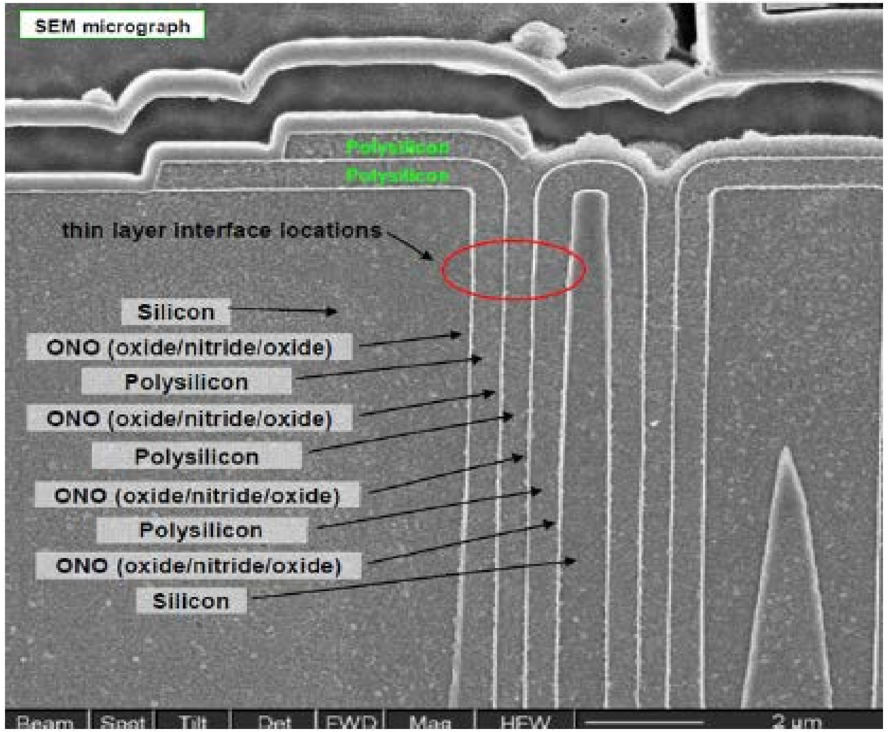
Formed Ceramic Thin-film Formation Process



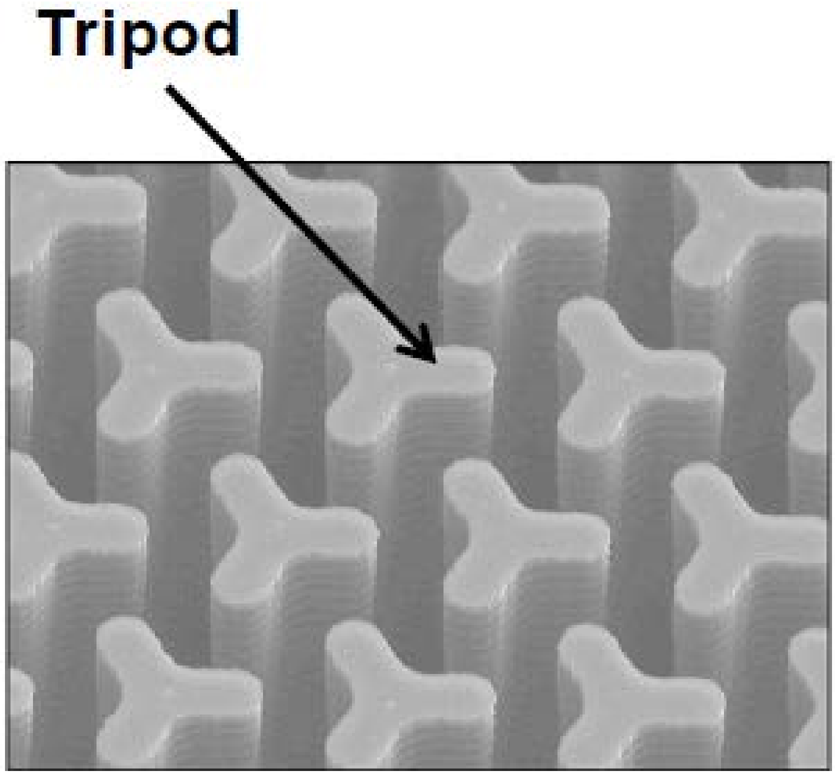


- Thin , flexible Ni carrier substrate
- Foil-transfer for easy processing
- BST dielectric (max ε=1000)
- 30-50- nF/mm^2
- Panel-scalability

Silicon Trench Capacitors

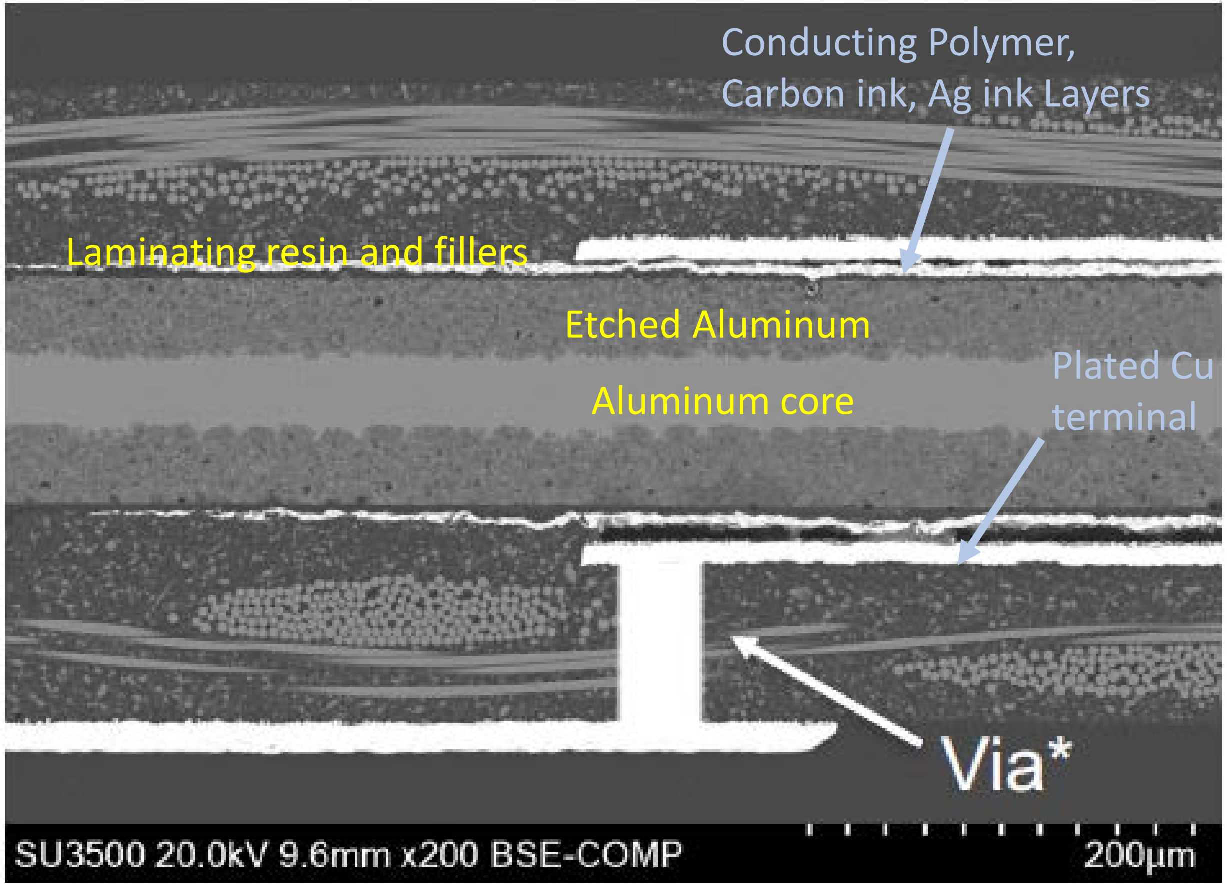


Silicon trench capacitors from IPDiA



- Silicon chip capacitors offer highest temperature capabilities and compatibility with wafer-level integration (150° C – 250° C)
- Down to 80 µm thickness
- Densities beginning to compete with MLCCs due to high-surface areas (500 nF/mm^2 max)

Embedded Electrolytic Aluminum Capacitors



Thin, planar format

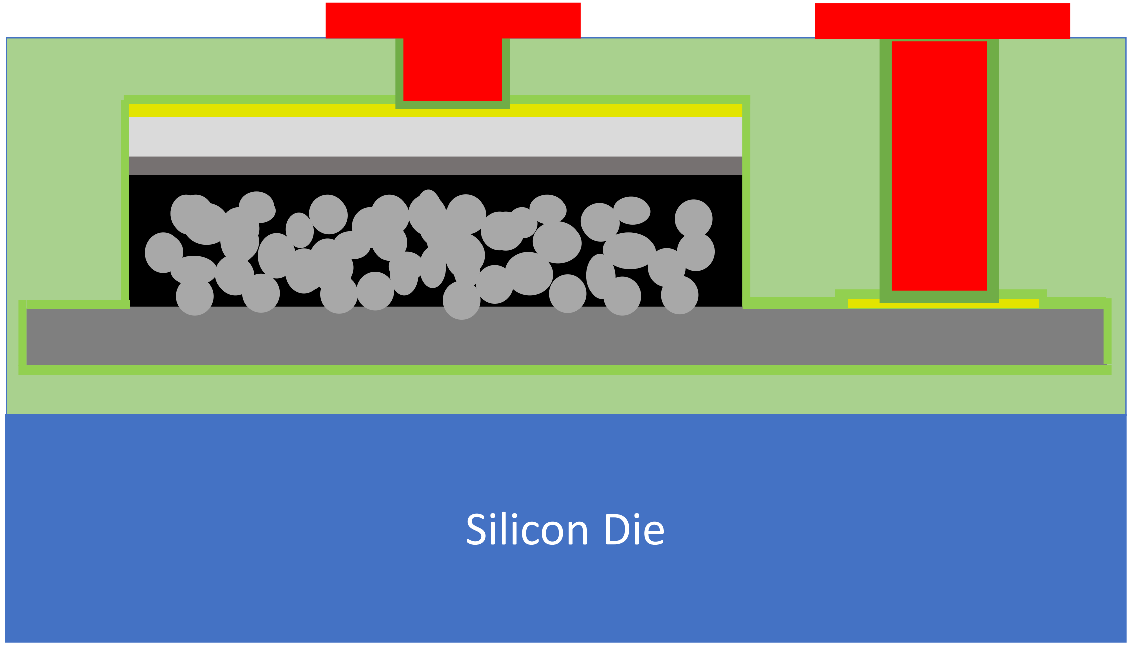
High capacitance density (> 2× that of MLCCs)

Capability	Target
Rated voltage	2V-50V+
Capacitor size	≤1mm
Cap thickness	~50µm
Capacitance	≥100µF/cm^2
DC leakage	<50 nA/CV

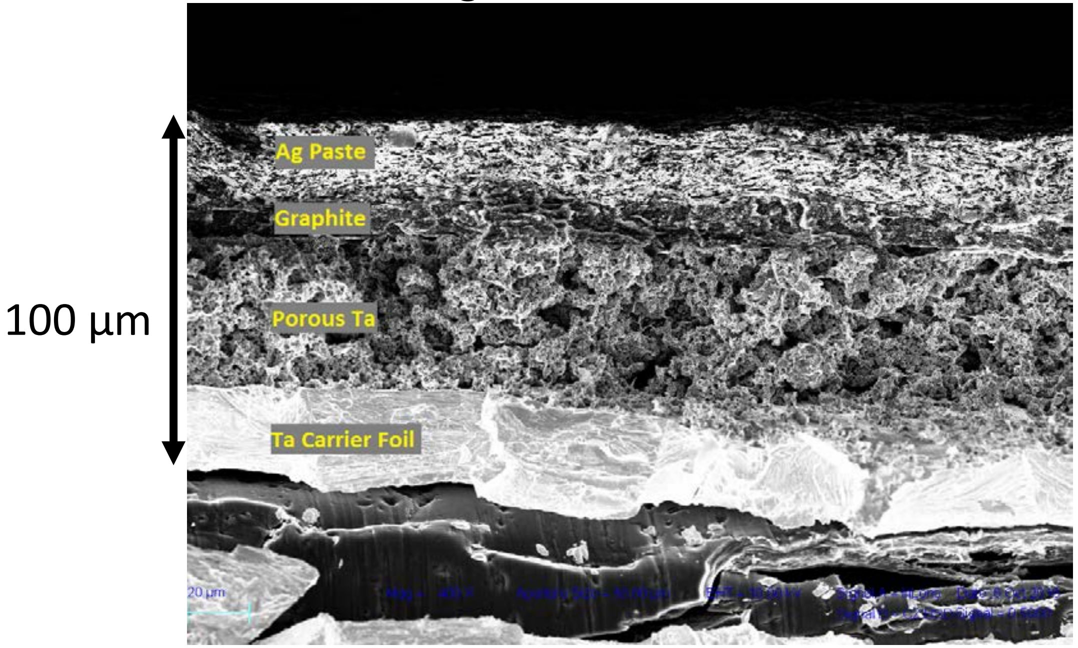
- Terminals formed by copper cladding and plating
- Capacitors patterned onto transfer release film for panel-scale processing
  - Arrayed sheets
  - Individual taping

Summey, B., KEMET Corporation. *Embedding Aluminum Polymer Capacitors* in *APEC* 2017.

Embedded Tantalum



Thin-film design



Improved capacitance density and frequency stability

Capacitor Type	Operating Voltage (V)	Thickness (mm)	Volumetric Density 1 kHz (µF/mm^3)	Volumetric Density 1 MHz (µF/mm^3)	ESR (mΩ)
Thin-film	2	0.1	32.4	14.3	58
Thin-film	3	0.1	24.1	13.5	54
Thin-film	5	0.1	15.6	11.1	65
Commercial	2	1.9	7.88	2.36*	40
Commercial	3	1.9	5.53	1.66*	15
Commercial	4	0.9	8.68	Not reported	500
Commercial	6.3	0.6	11.87	Not reported	1500

**Specific values not provided, only general characteristics of the series*

Roadmap of Formed Capacitors for Embedding

2000 | 2008 | 2016 | 2020

Board or package embedding;
I/O decoupling; 100 MHz

Polymer film capacitors

0.02 nF/mm^2
Polymer laminate dielectrics

0.1 nF/mm^2
Polymer film and adv.
polymer-ceramic composites

Ceramic film capacitors

2-3 nF/mm^2
Thin oxides

20-30 nF/mm^2
BaTiO3 film

30-50 nF/mm2
enabled by
dielectric thinning

Package embedding;
Core and I/O decoupling; 100-500 MHz

Silicon trench capacitors

Silicon capacitors Deep trench
0.08 µF/mm^2 0.25 µF/mm^2 0.3 µF/mm^2

Ultra-high surface area silicon
0.4 -0.8 µF/mm^2

IVR; Embedded PoL
1-20 MHz

Ta or etched foil capacitors

Embedded
nanoporous
electrode
1 µF/mm^2

Adv.
Nanotech.
> 5µF/mm^2

IVR; Embedded PoL
1-5 MHz

Emerging Technologies

Barrier-layer capacitors –
1-5 µF/mm^2
- Early stage development

Summary

- New era of packaging involving embedding of passive components
  - Reduce system size, lower parasitics, thinner modules
  - High-frequency noise filtering or decoupling
  - High-efficiency, fine-grain power management
- Inserted MLCCs becoming more available, enabled by thinner dielectrics and improved process integration
- Silicon trench capacitors for improved thermal and voltage stability, and on-chip integration
- For high-density, embedded electrolytic capacitors in development