2022 PSMA/PELS Capacitor Workshop:
How Materials and Environmental Effects Influence Capacitor Performance
George R. Brown Convention Center in Houston, TX
Saturday March 19, 2022

Packaging MLCCs for Higher AC Voltage Applications/Future Developments

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Speed of Switching – dv/dt Possible Across the Capacitors

GaN-based DPT Switching: 400V/40A with 48V/ns*

40A

61A (above saturation current limit)

Vrise= 12.1ns

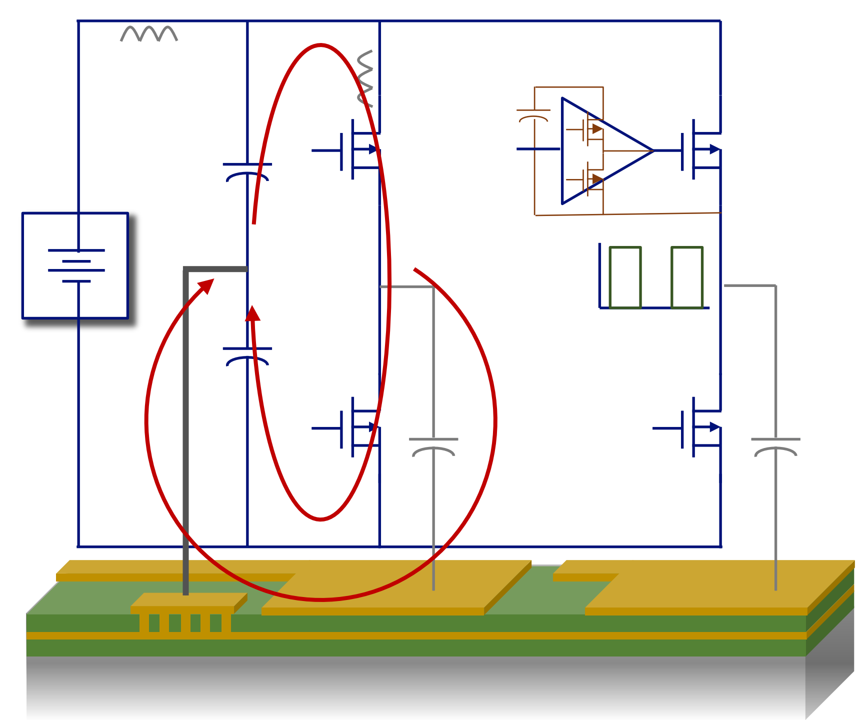
Vfall= 8.3ns

dV/dt,rise = 24.4V/ns at 40A; 4 times increase than at 21A

SiC-based DPTSwitching: 4kV/20A with 113V/ns**

i = C *dv/dt* for 15nF

i: 720A or 1.7kA



* Sourish Sinha from Mar 2022 PowerAmerica MIP Report

** Utkarsh Mehrotra March 2022 Dissertation

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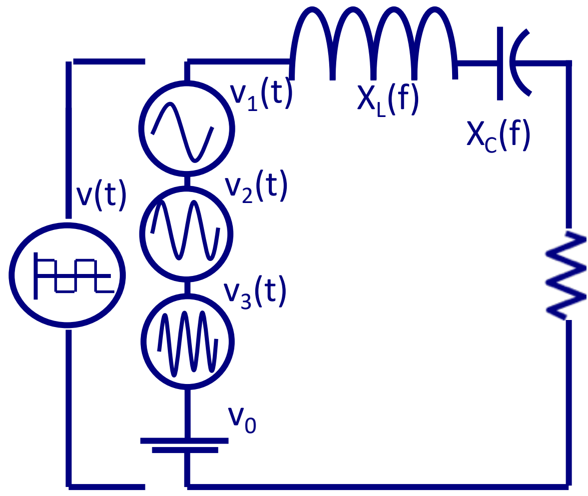
PREES Laboratory NC STATE UNIVERSITY
PACKAGING RESEARCH IN ELECTRONIC ENERGY SYSTEMS

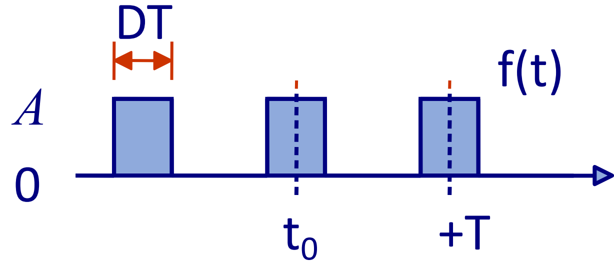
Objective

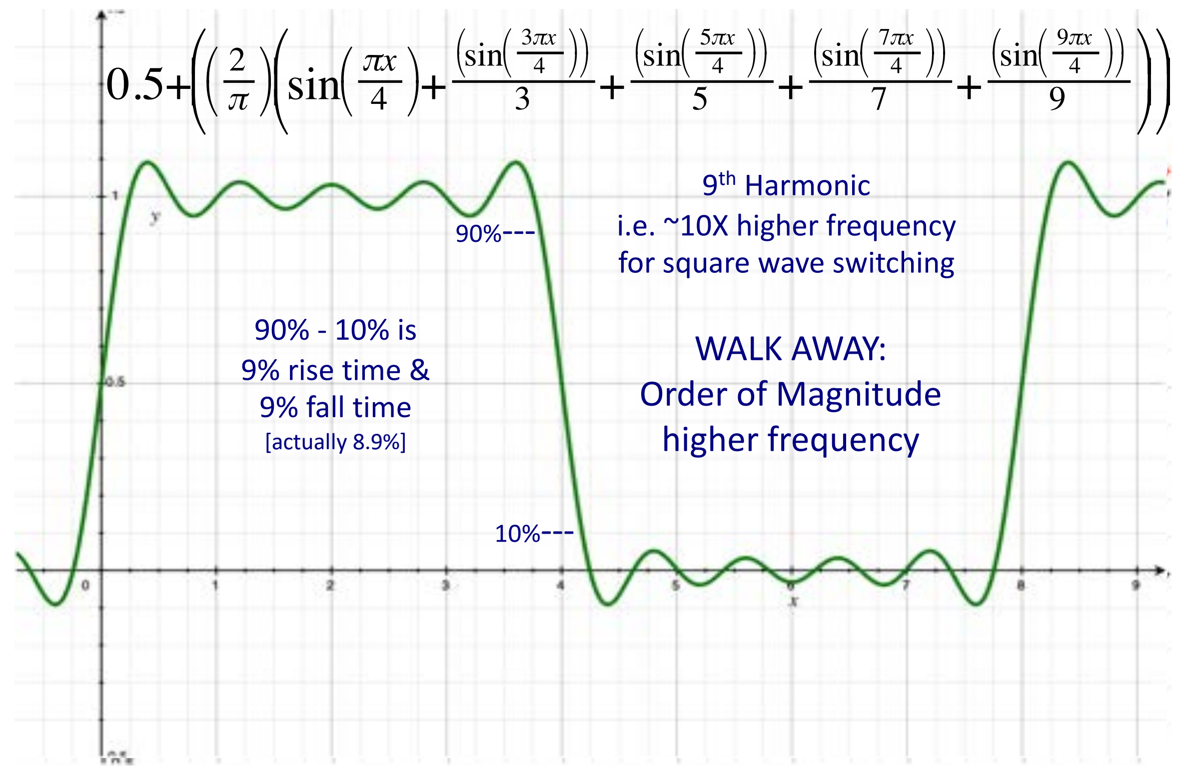
High *dv/dt* from new Wide Band Gap devices, e.g. GaN & SiC, present very high voltage stress levels on MLCCs.

$$f(t) = (AD) + \frac{2A}{\pi}\sum_{n=1}^{\infty}\frac{sin(n\pi D)}{n}\cos(n\omega t - \theta) \qquad \theta_n = n\omega t_0$$

$$c_n = \frac{2A}{\pi}\frac{sin(n\pi D)}{n}, n \neq 0$$







$$f(t) \approx 2.5 + \frac{10}{\pi}\left(\sin\frac{\pi t}{4} + \frac{1}{3}\sin\frac{3\pi t}{4}\cdots\right)$$

For a "SQUARE WAVE" only ODD harmonics exist

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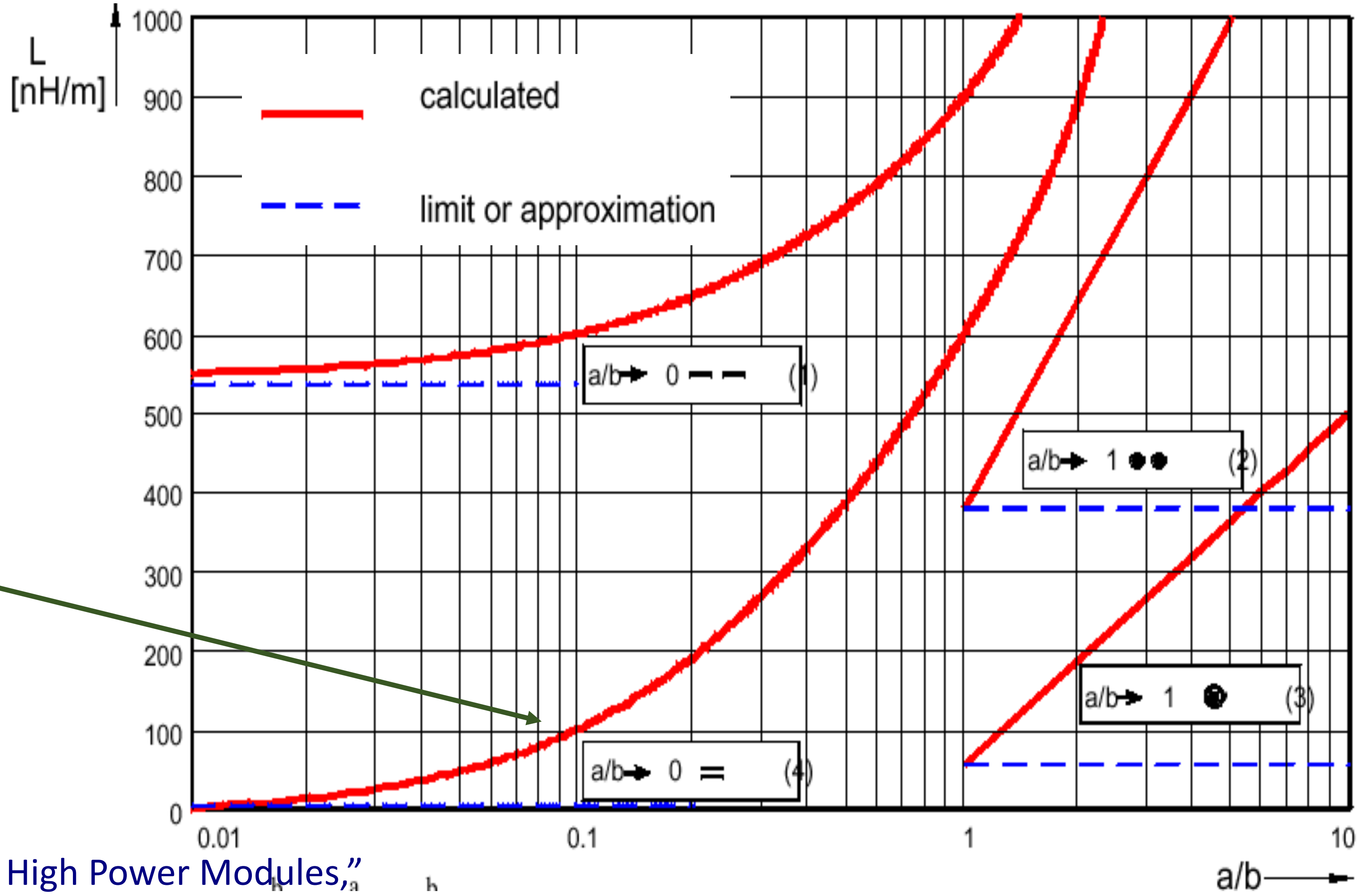
Packaging Inductance – Key is Electromagnetic Cancellation

Several approaches to trace and COMPONENT placement. Wherever the current flow reverses and flows back over itself, the flow provides a reduction of the electromagnetic field, and hence lower inductance.

Hence, the Strip Line approach is preferred.

Lower inductance then the lower the *dv/dt* from high speed switching



"Design Aspects for Inverters with IGBT High Power Modules," Dr.-Ing. Th. Schütze, eupec GmbH & Co KG, Warstein, Germany

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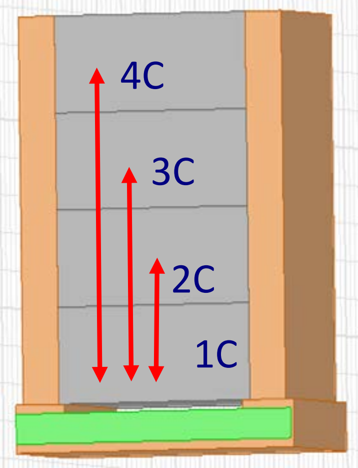
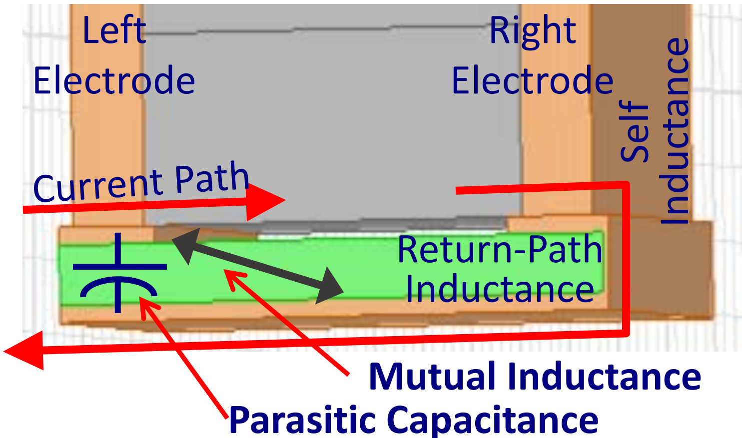
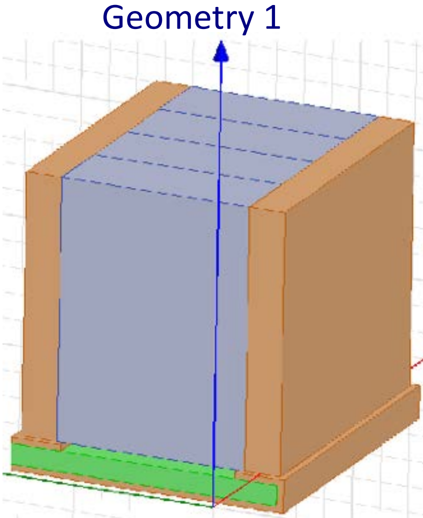
Optimum Mounting for Inductance



Geometry 1





Geometry 2

Return Path + Right Electrode base inductance after inductance cancellation

Mutual Inductance is between left electrode and return path - nH

ANSYS Parasitics Simulation for Capacitor Structures on Fr4 PCB

Geometry	Substrate Thickness	Sample	Self Inductance	Mutual Inductance	Return Path	Parasitic Capacitance
	um		nH	nH	nH	pF
1	800	1C	0.36	-0.181	2.24	1.39
		2C	1.02	-0.520	3.74	1.46
		3C	1.90	-0.894	4.69	1.51
		4C	2.94	-1.38	5.78	1.57
	400	1C	0.359	-0.270	2.86	2.38
		2C	1.03	-0.510	3.59	2.45
		3C	1.90	-0.875	4.51	2.50
		4C	2.94	-1.35	5.57	2.56
2	800	1C	4.79	-1.53	9.61	0.510
		2C	3.85	-1.48	7.66	0.879
		3C	3.28	-1.42	6.50	1.24
		4C	2.89	-1.36	5.71	1.62
	400	1C	4.79	-1.52	9.30	0.810
		2C	3.85	-1.46	7.40	1.43
		3C	3.28	-1.40	6.28	2.04
		4C	2.89	-1.34	5.51	2.66

Capacitor: C3640C884MCGLC

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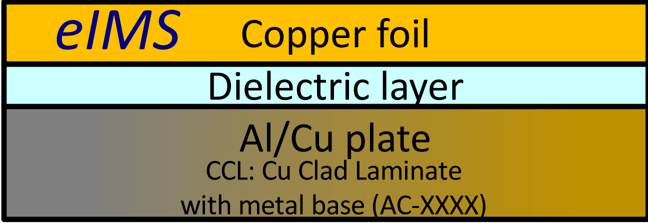
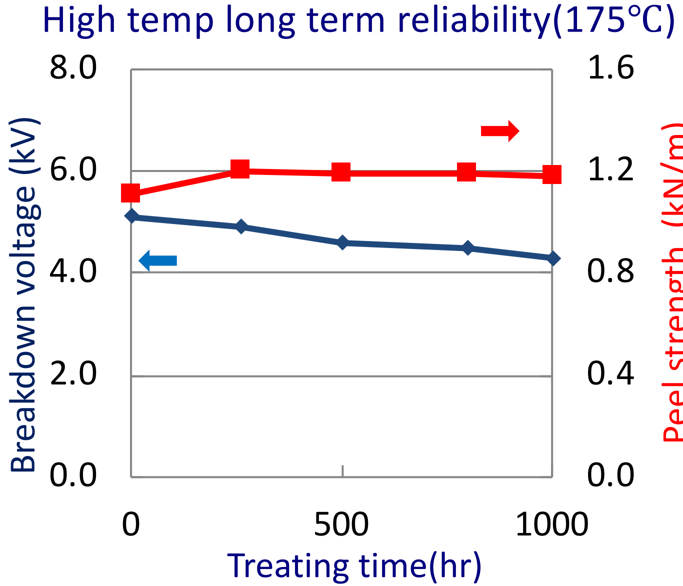
New Epoxy Resin Composite Dielectric:10W/mK

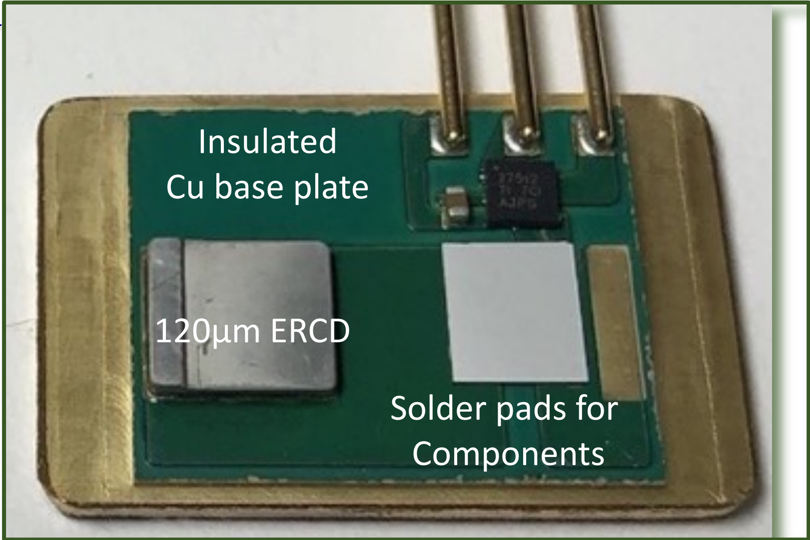


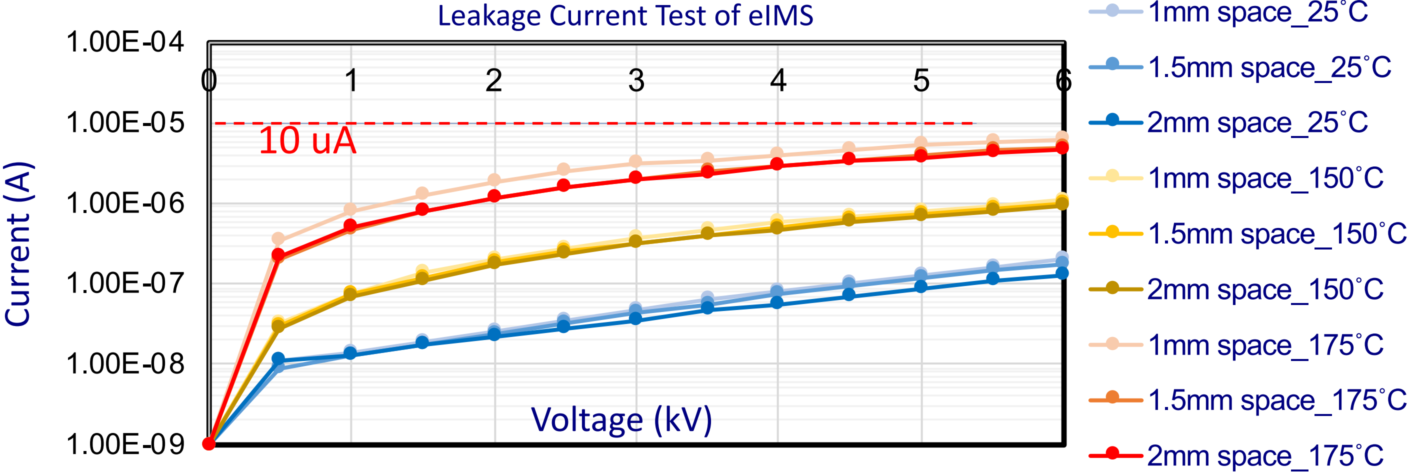
PROPERTIES

Product number	RISHO: AC-7210	
Dielectric layer thickness	120μm	
Thermal conductivity（W/mK）	**10**	Laser flush method
Tg（℃）	**270**	DMA method
Peel strength（kN/m）	1.2	1 oz copper
Solder limit（sec）	60＜	260℃
CTE（ppm/℃）α1	14/14/14	X/Y/Z
Breakdown V（kV_{ac}）(50/60Hz)	**> 5**	JIS C2110 (ASTM-D149)

http://www.risho.co.jp/english/product/products0/index.html







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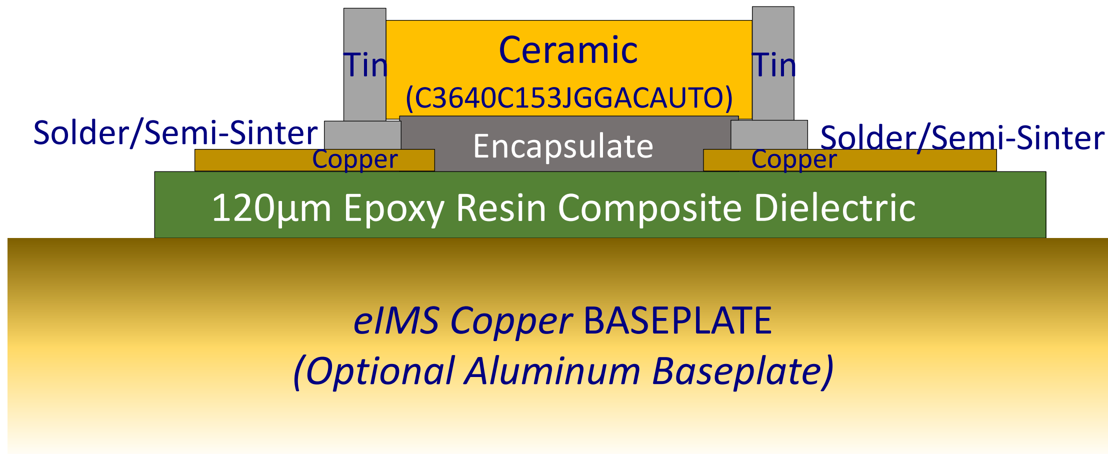
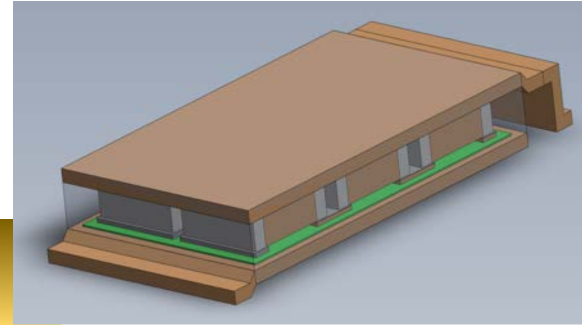
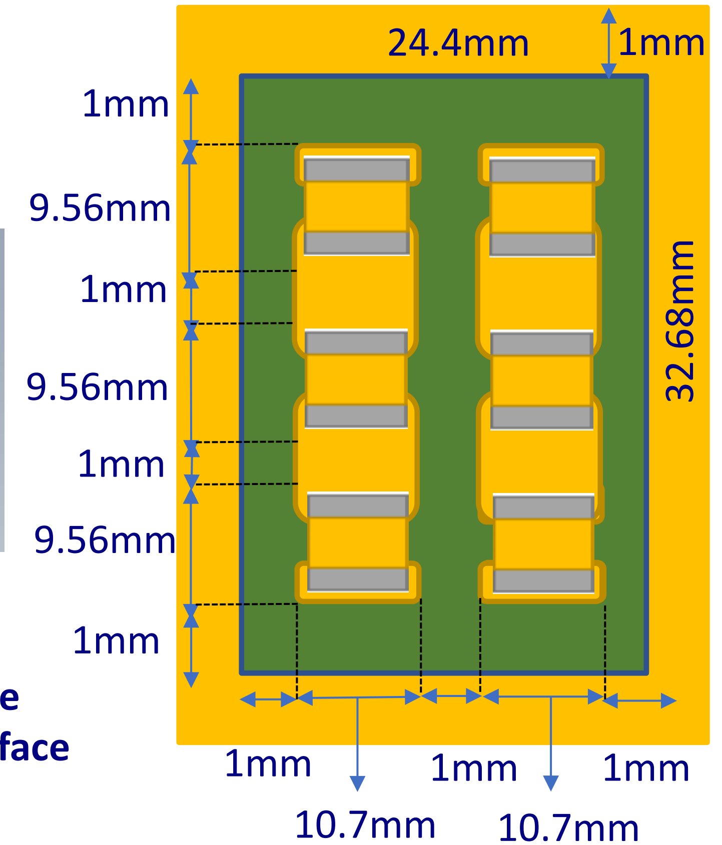
High Density (HD) Module for 3S,2P Capacitor Module – 120um ERCD, BV=5.2kV



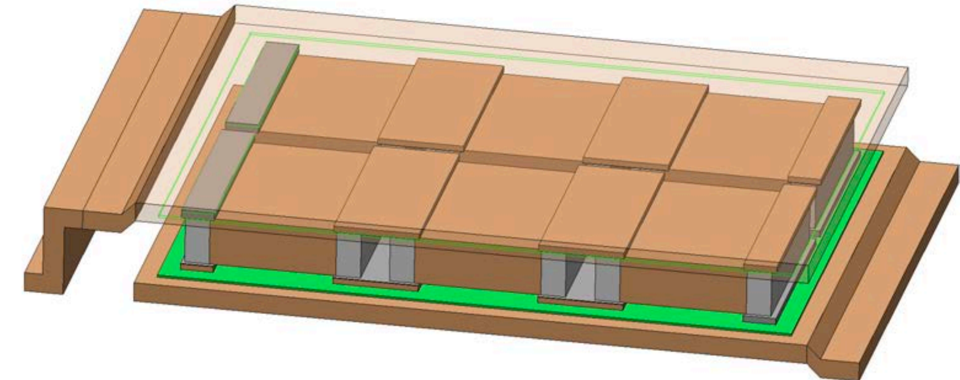




Geometry Information:

- 120um ERCD; BV – 5.2kV
- 1mm eIMS Cu plate (both sides), 300um Trace Thickness
- Capacitor – 9.1 x 10.2 x 2.5 (LxWxT)
- Six 0.015 uF, 5%, 2000 VDC, C0G, SMD, MLCC, Automotive Grade, 3640
- 4.5kV operating voltage (1.5kV per device
- Epoxy Underfill, 1.2W/mK

- *h* coefficient = **300 W/m²K top surface**
- *h* coefficient = **15 W/m²K bottom surface**
- Ambient Temperature, T_a = 25˚C
- P = 25W (entire module)



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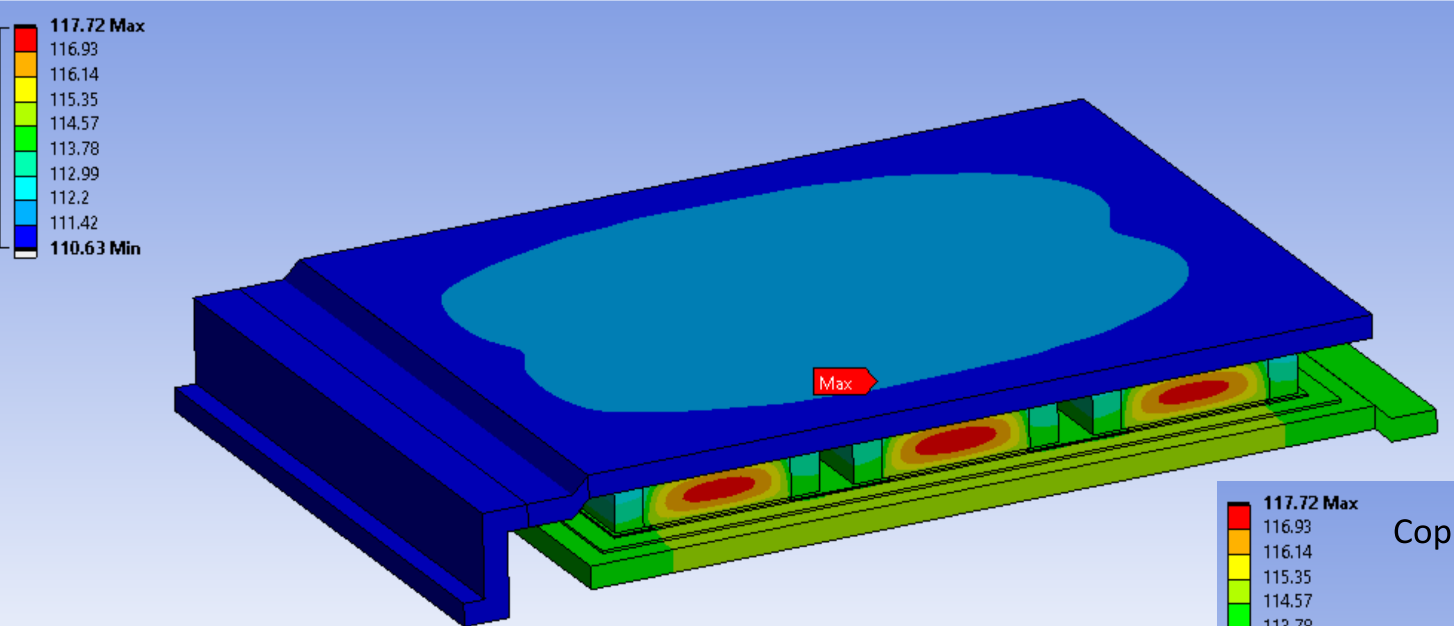
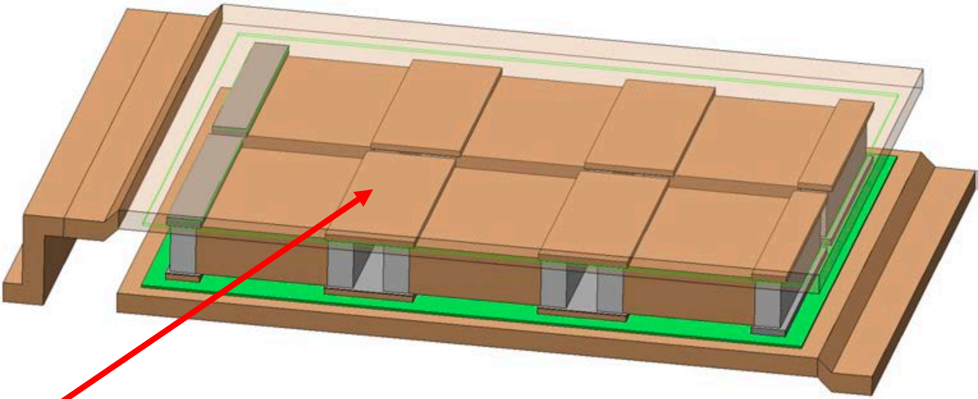
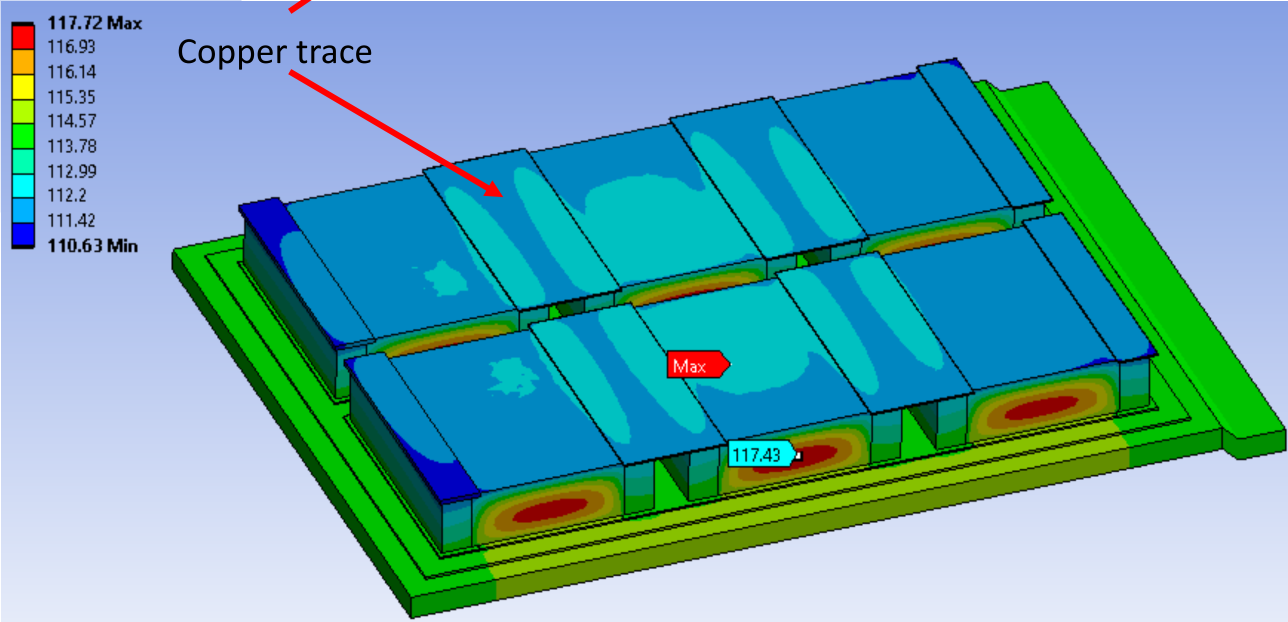
120um ERCD, 3S2P, HD, BV=5.2kV, P=25W







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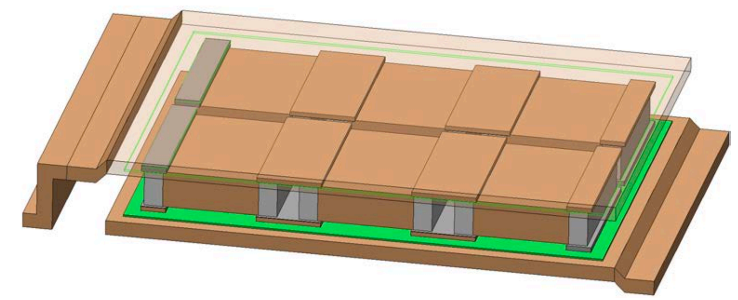
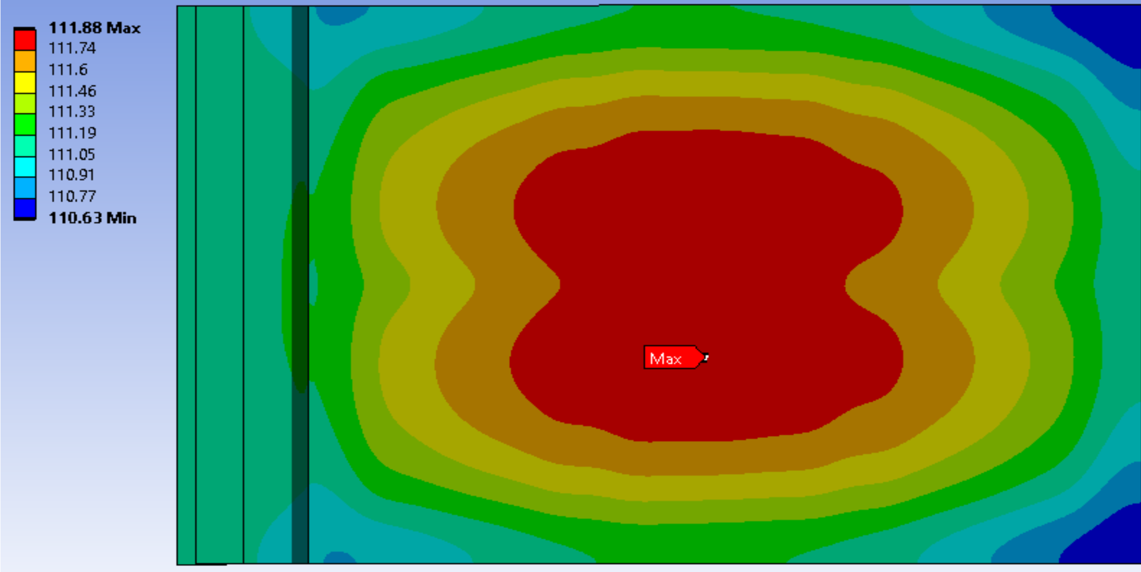
120um ERCD, 3S2P, HD, BV=5.2kV, P=25W





Bottom-side Top Cu/ lead frame

Cap center (d) to case (c), case to ambient (a)

Rth,d-c = $\frac{(T_{d,max}-T_c)}{P}$ and Rth,c-a = $\frac{(T_c-25)}{P}$

$T_{d,max}$ = 117.7˚C, T_c = 111.9˚C and P_{pkg} = 25W

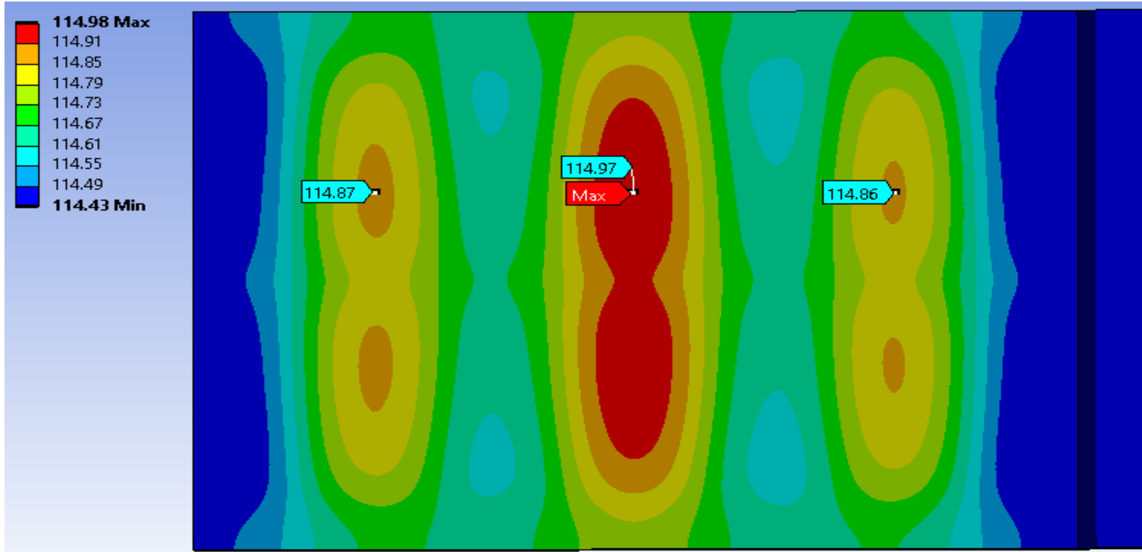
Rth,d-c = 0.2336˚C/W

Rth,c-a = 3.475˚C/W

Rth,d-a = 3.71˚C/W

Ambient Temperature = 25˚C

4.17W/chip



Bottom-side Bottom Cu/ lead frame

Rth,d-c = $\frac{(T_{d,max}-T_c)}{P}$ and Rth,c-a = $\frac{(T_c-25)}{P}$

$T_{d,max}$ = 117.7˚C, T_c = 115.0˚C and P_{pkg} = 25W

Rth,d-c = 0.1096˚C/W

Rth,c-a = 3.599˚C/W

Rth,d-a = 3.709˚C/W

h coefficient = 300 W/m^{2}K top surface

h coefficient = 15 W/m^{2}K bottom surface

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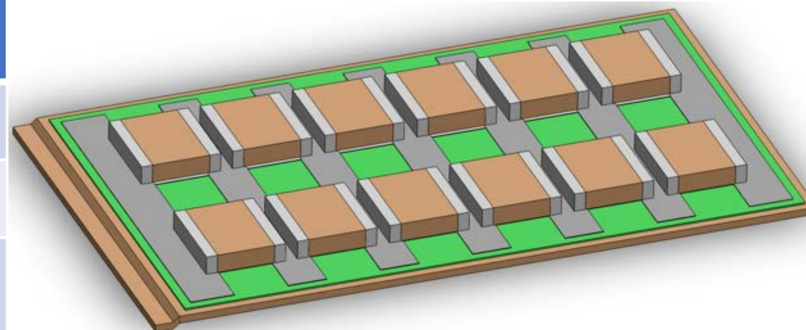
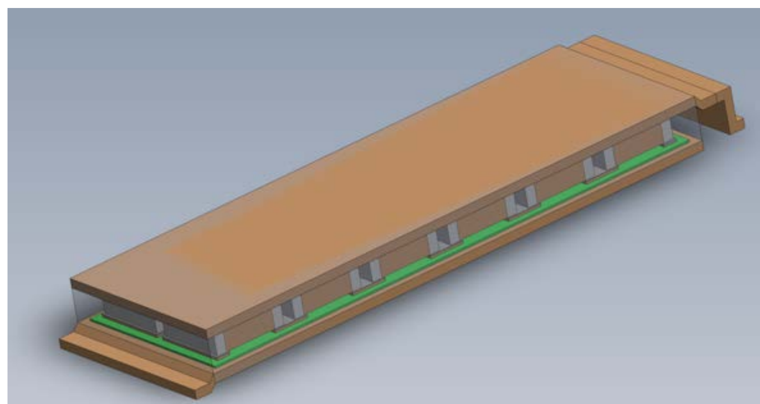
Near Optimum Thermal Layout – Six dies in series, Two rows (6S,2P), 240um ERCD; BV – 10.4kV

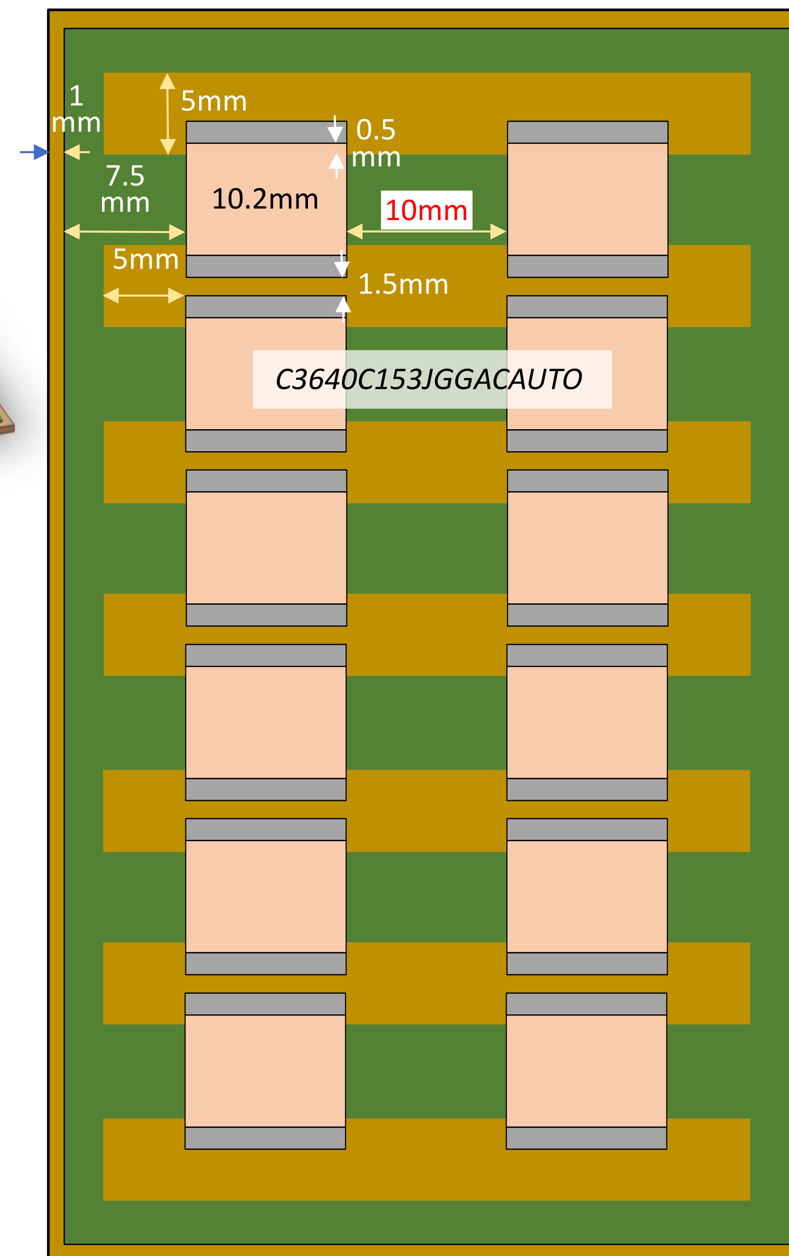
Material	Thermal Cond. (W/m.K)	Thickness (µm)
ERCD	10	240
Encapsulate	3	85
Copper (trace and baseplate)	391	34 (1oz) & 1mm
Tin	67	2500
Solder (Pb-Sn)	60	50
Capacitor	5	2500





Geometry Information:

- **240um ERCD; BV – 10.4kV**
- 1mm eIMS Cu plate (both sides), 34um Trace Thickness
- Capacitor – 9.1 x 10.2 x 2.5 (LxWxT)
- Twelve 0.015 uF, 5%, 2000 VDC, C0G, SMD, MLCC, Automotive Grade, 3640
- 9kV operating voltage (1.5kV per device)
- Epoxy Underfill, 1.2W/mK
- *h* coefficient = **300 W/m²K top surface**
- *h* coefficient = **15 W/m²K bottom surface**
- Ambient Temperature, T_a = 25°C
- P = 50W (entire module)



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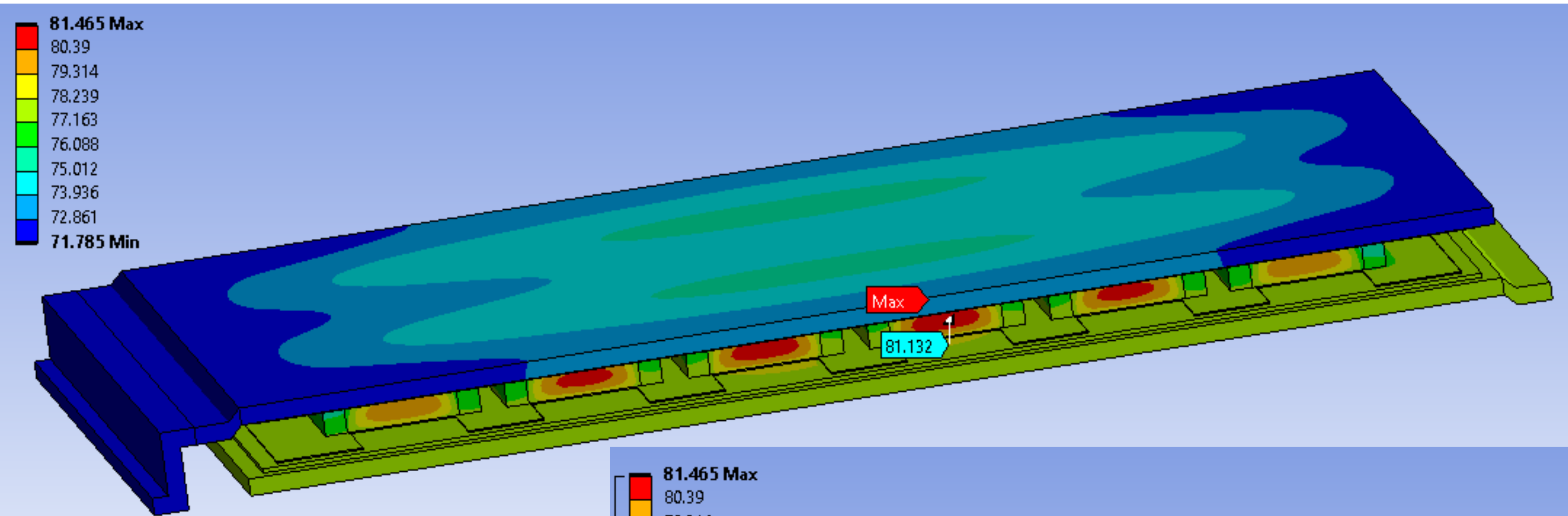
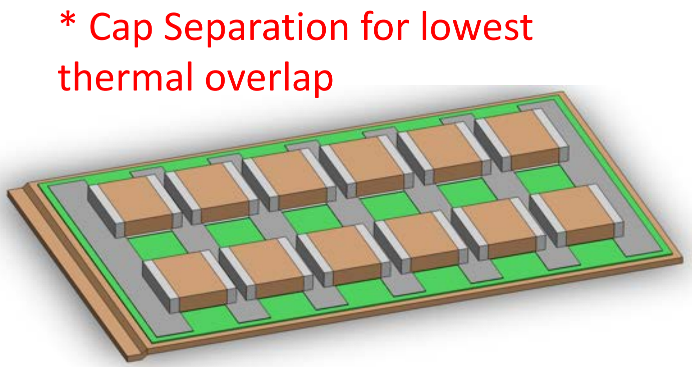
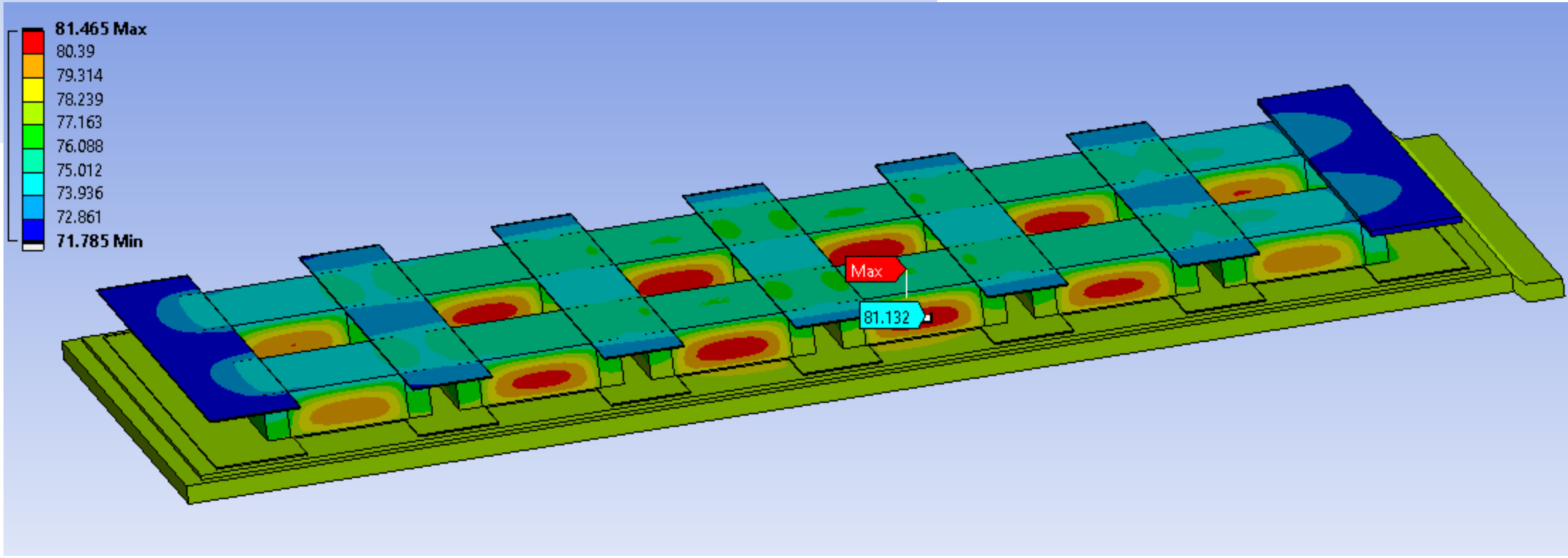
240um ERCD 6S,2P, Thermally Optimum*, BV=10.4kV, P=50W



* Cap Separation for lowest thermal overlap





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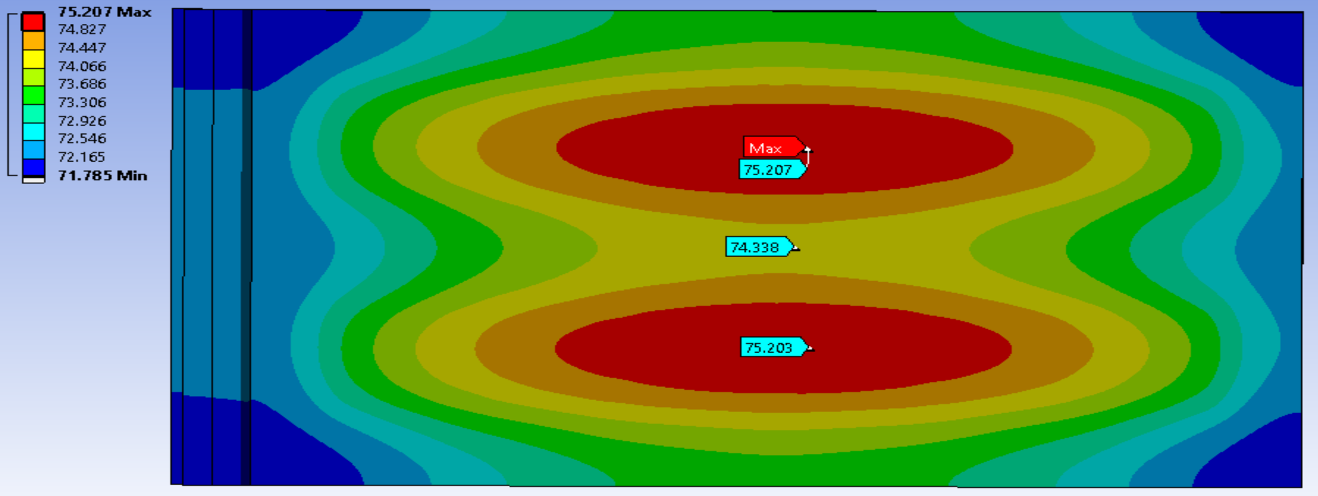
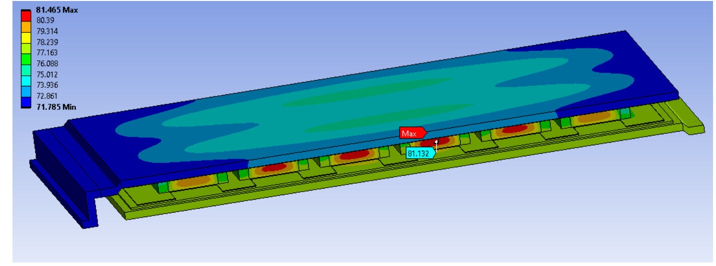
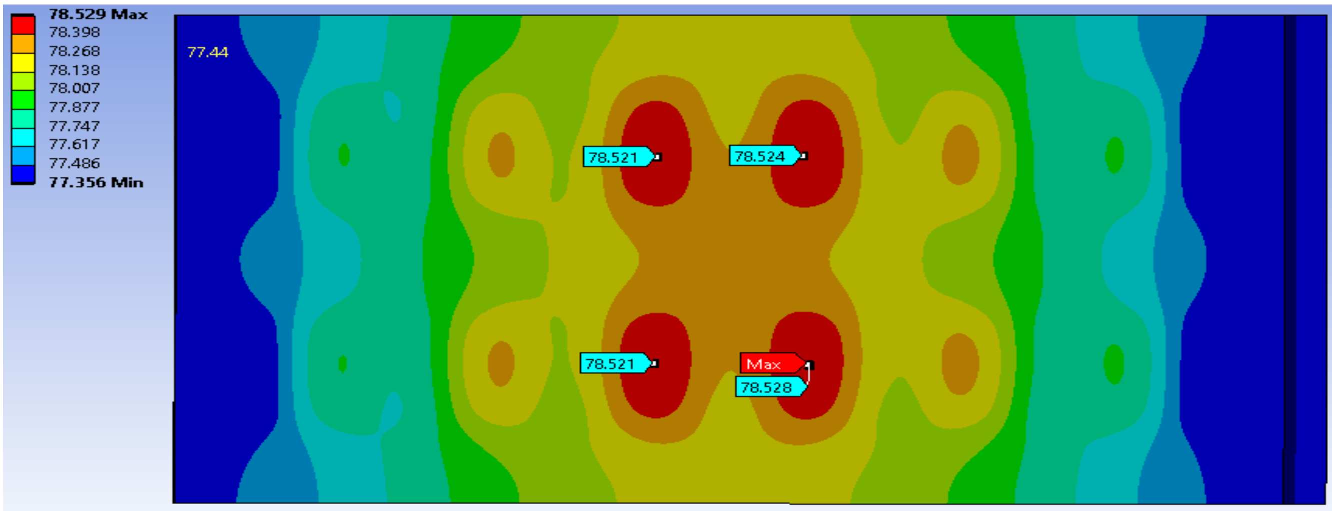
240um ERCD 6S,2P, Thermally Optimum, BV=10.4kV, P=50W

Bottom-side Top Cu/ lead frame





Bottom-side Bottom Cu/lead frame



Rth,d-c = $\frac{(T_{d,max} - T_c)}{P}$ and Rth,c-a = $\frac{(T_c - 25)}{P}$

$T_{d,max}$ = 81.47˚C, T_c = 75.21˚C and P = 50W

Rth,d-c = 0.125˚C/W

Rth,c-a = 1.004˚C/W

Rth,d-a = 01.13˚C/W

Ambient Temperature = 25˚C

4.17W/chip

Rth,d-c = $\frac{(T_{d,max} - T_c)}{P}$ and Rth,c-a = $\frac{(T_c - 25)}{P}$

$T_{d,max}$ = 81.47˚C, T_c = 78.53˚C and P =50W

Rth,d-c = 0.0587˚C/W

Rth,c-a = 1.071˚C/W

Rth,d-a = 1.13˚C/W

h coefficient = 300 W/m^{2}K top surface

h coefficient = 15 W/m^{2}K bottom surface

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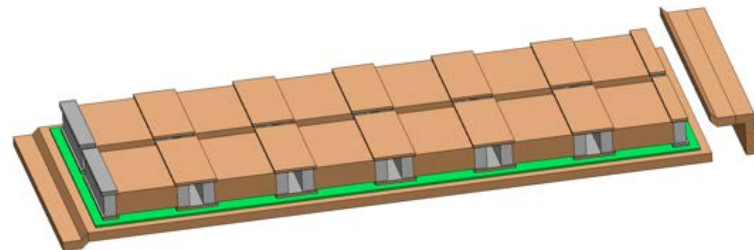
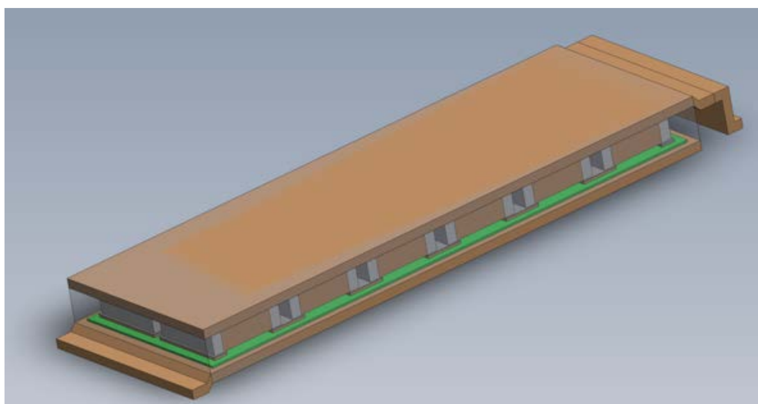
Thermal Layout – Six dies in series, Two rows (6S,2P), 240um ERCD; BV–10.4kV

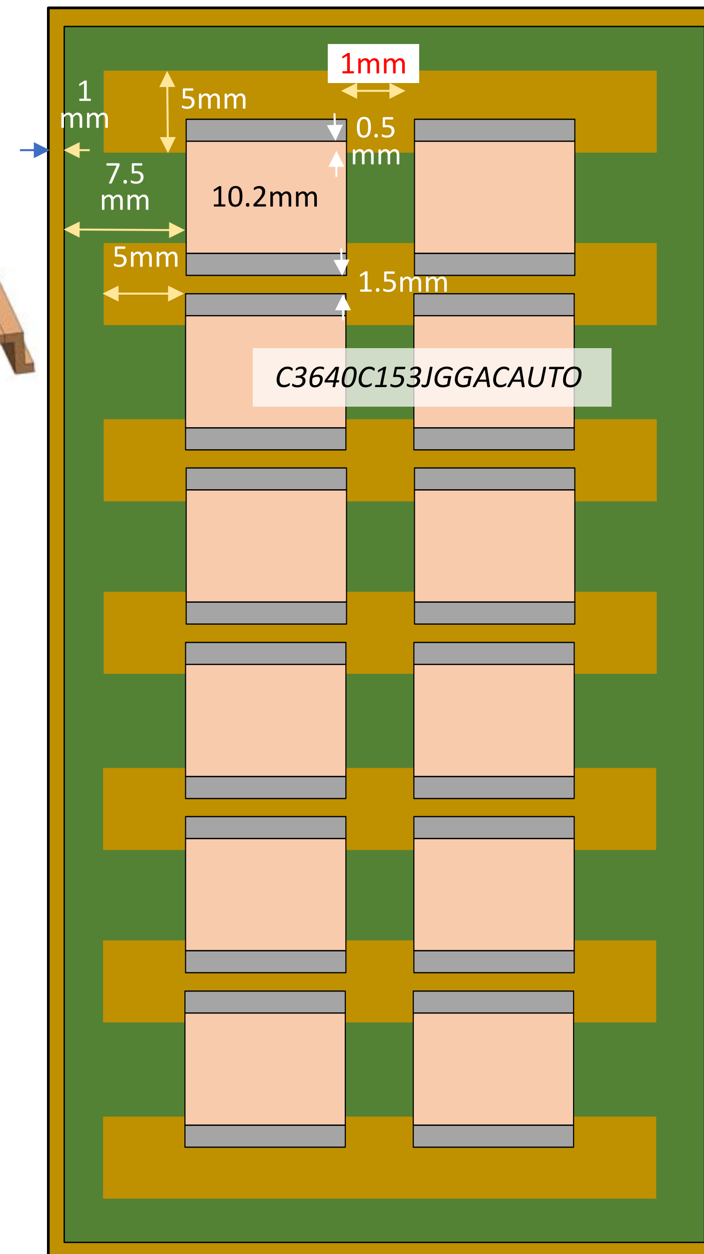
Material	Thermal Cond. (W/m.K)	Thickness (µm)
ERCD	10	240
Encapsulate	3	85
Copper (trace and baseplate)	391	34 (1oz) & 1mm
Tin	67	2500
Solder (Pb-Sn)	60	50
Capacitor	5	2500





Geometry Information :

- **240um ERCD**; BV – 10.4kV
- 1mm eIMS Cu plate (both sides), 300um Trace Thickness
- Capacitor – 9.1 x 10.2 x 2.5 (LxWxT)
- Twelve 0.015 uF, 5%, 2000 VDC, C0G, SMD, MLCC, Automotive Grade, 3640
- 9kV, operating voltage (1.5kV per device)
- Epoxy Underfill, 1.2W/mK
- *h* coefficient = **300 W/m²K top surface**
- *h* coefficient = **15 W/m²K bottom surface**
- Ambient Temperature, T_a = 25°C
- P = 50W (entire module)



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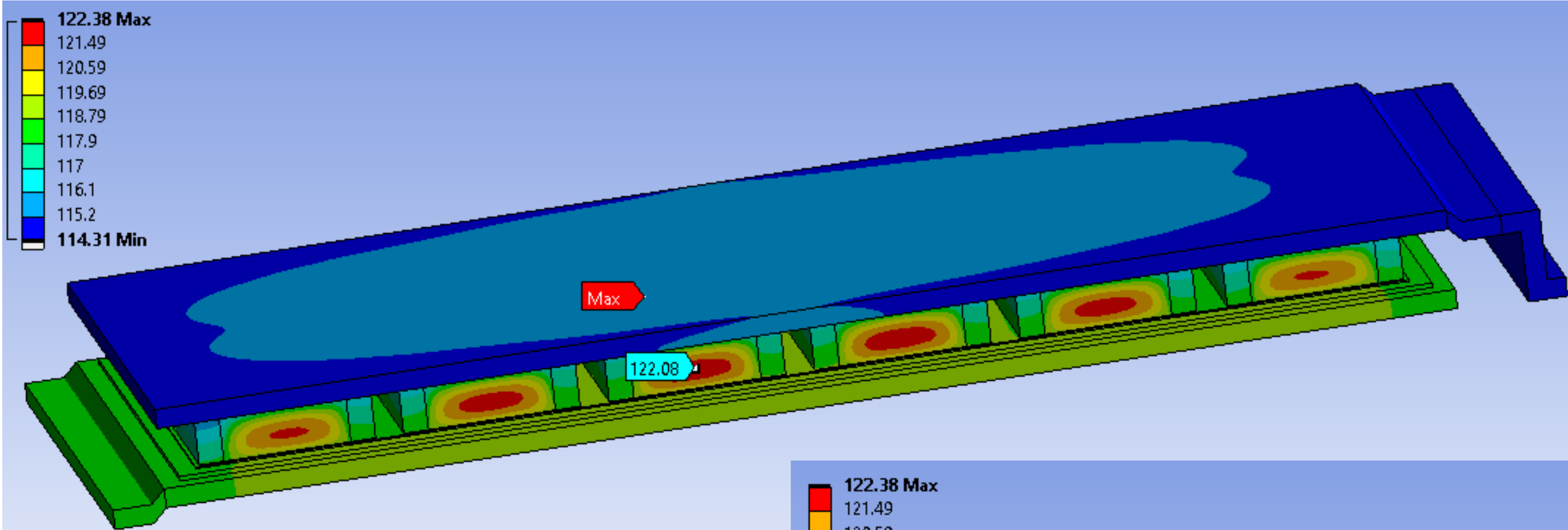
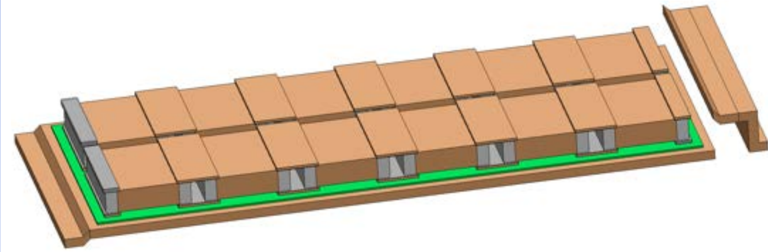
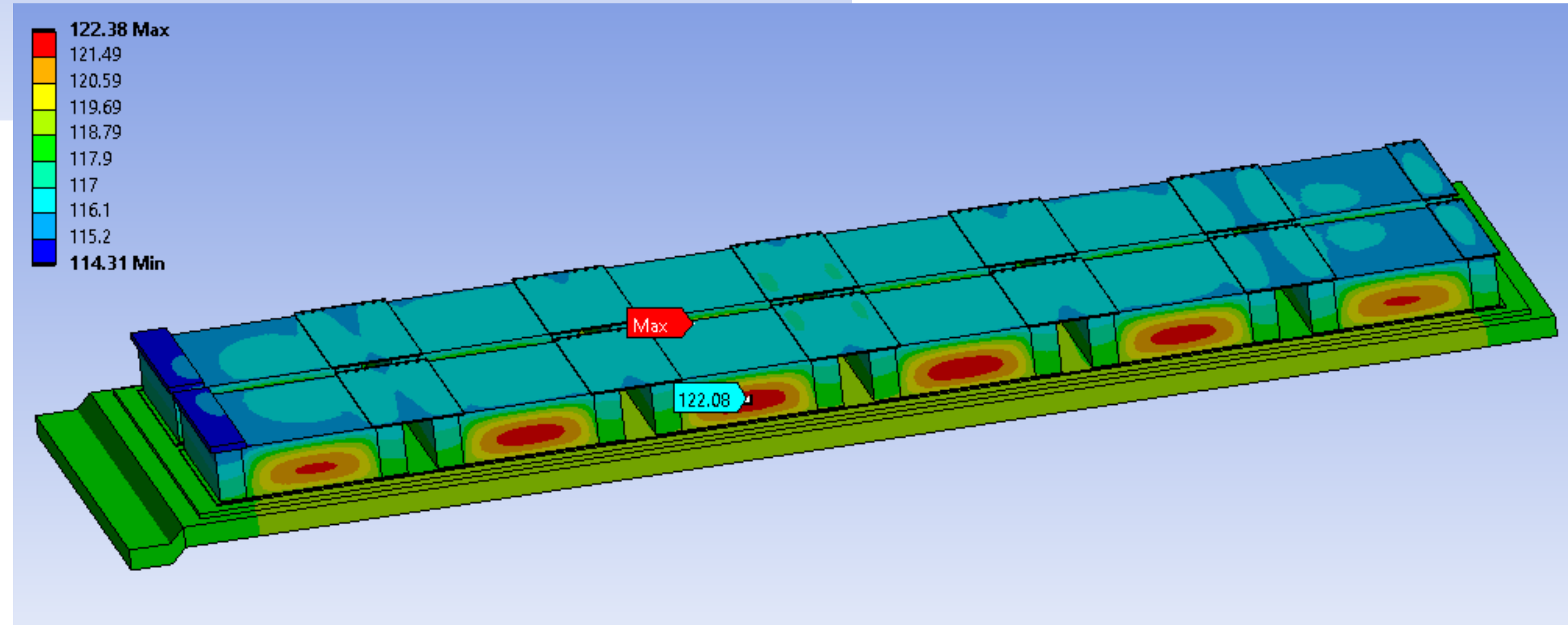
240um ERCD 6S,2P HD, BV=10.4kV, P=50W







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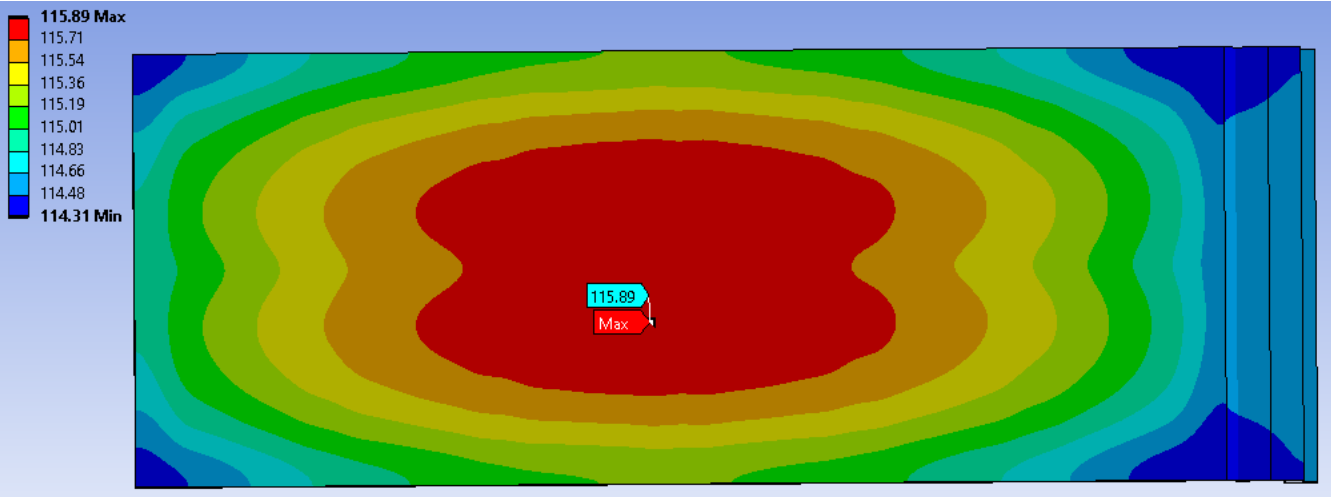
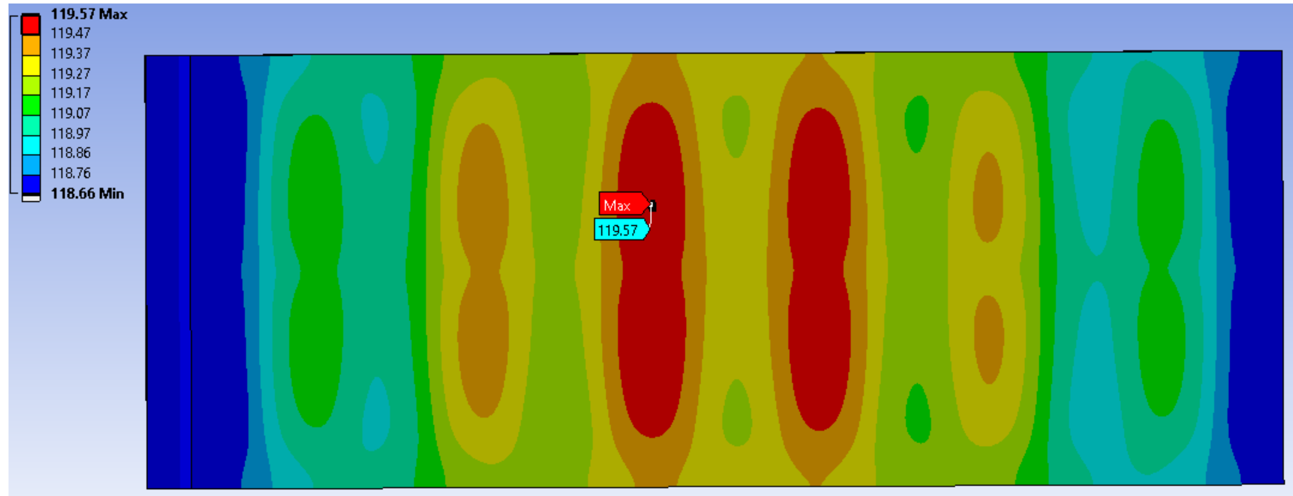
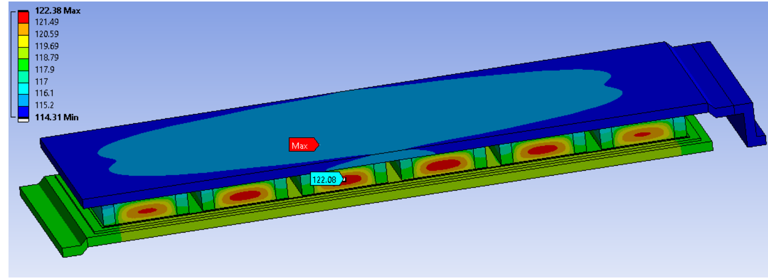
240um ERCD 6S,2P HD, BV=10.4kV, P=50W

Bottom-side Top Cu/ lead frame



Bottom-side Bottom Cu/lead frame





Rth,d-c = $\frac{(T_{d,max} - T_c)}{P}$ and Rth,c-a = $\frac{(T_c - 25)}{P}$

$T_{d,max}$ = 122.4˚C, T_c = 115.9˚C and P = 50W

Rth,d-c = 0.130˚C/W

Rth,c-a = 1.82˚C/W

Rth,d-a = 1.95˚C/W

Ambient Temperature = 25˚C

4.17W/chip

Rth,d-c = $\frac{(T_{d,max} - T_c)}{P}$ and Rth,c-a = $\frac{(T_c - 25)}{P}$

$T_{d,max}$ = 122.38˚C, T_c = 119.57˚C and P =50W

Rth,d-c = 0.0562˚C/W

Rth,c-a = 1.89 ˚C/W

Rth,d-a = 1.95˚C/W

h coefficient = 300 W/m^{2}K top surface

h coefficient = 15 W/m^{2}K bottom surface

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Resonant LLC Test Circuit for MLCC Testing

Musab Guven, M.Sc.
Prof. Dr. Douglas C Hopkins, Dr Bo Gao

(*Cr Resonant cap:* 440nF w/ serial CKC33C884KCGL- 880nF/500V)

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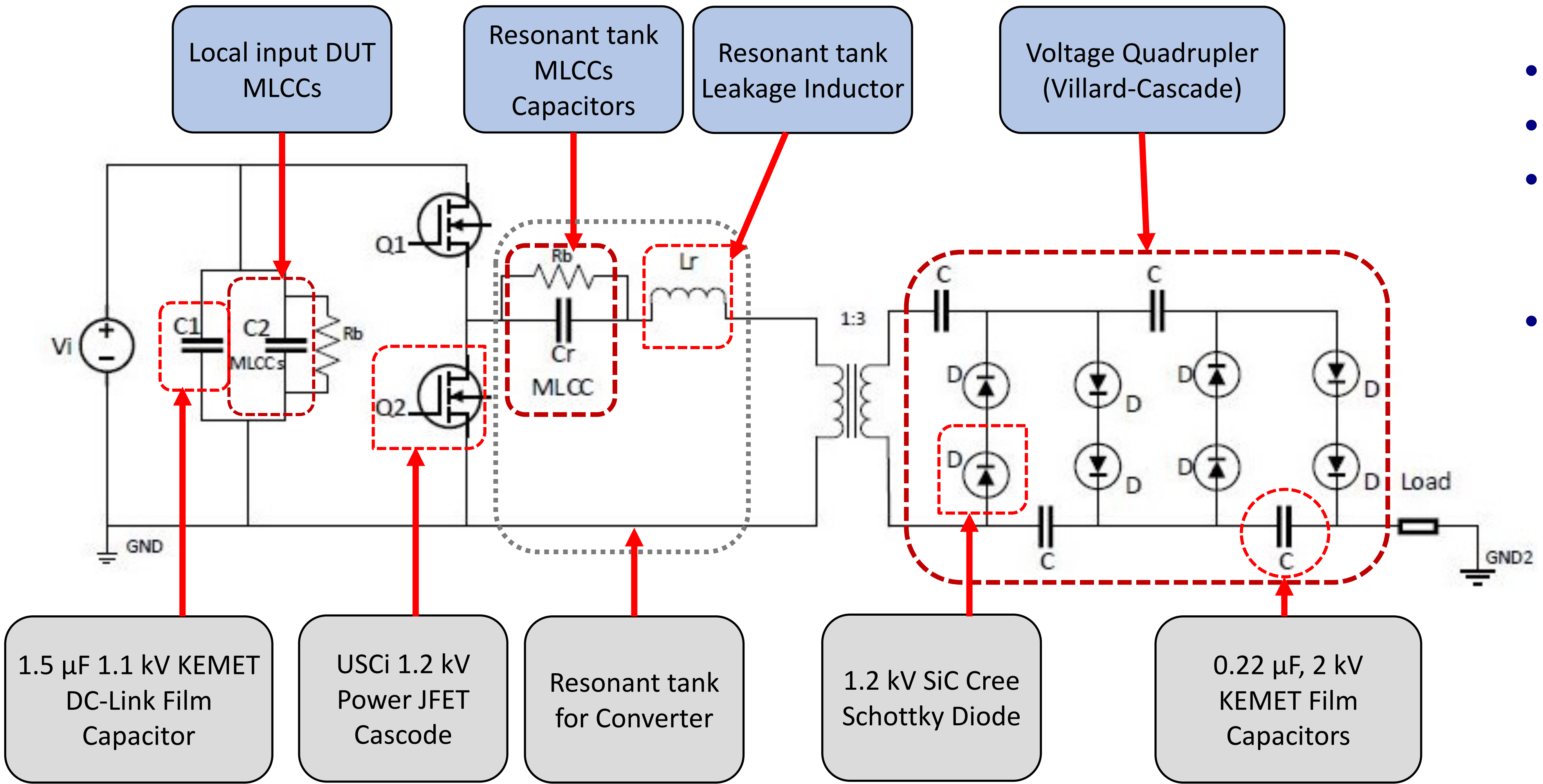
Circuit Design and Full Power Considerations

This research investigates MLCCs in a high frequency LLC converter for EV applications. The aim is to increase converter performance and examine electrical aspect of MLCCs.



Converter Design:

- Dual use test ckt
- 20 kW, ≧200 kHz
- 400-700 V_{in} - 50 A_{rms} Converter input and resonant tank current
- 4.2 kV_{out} – 8.33 A_{rms} (17.5 kW) Voltage Cascade Converter output

Cr Resonant cap:
440nF w/ serial CKC33C884KCGLC 880nF/500V, 4-chip stack of 3640 caps

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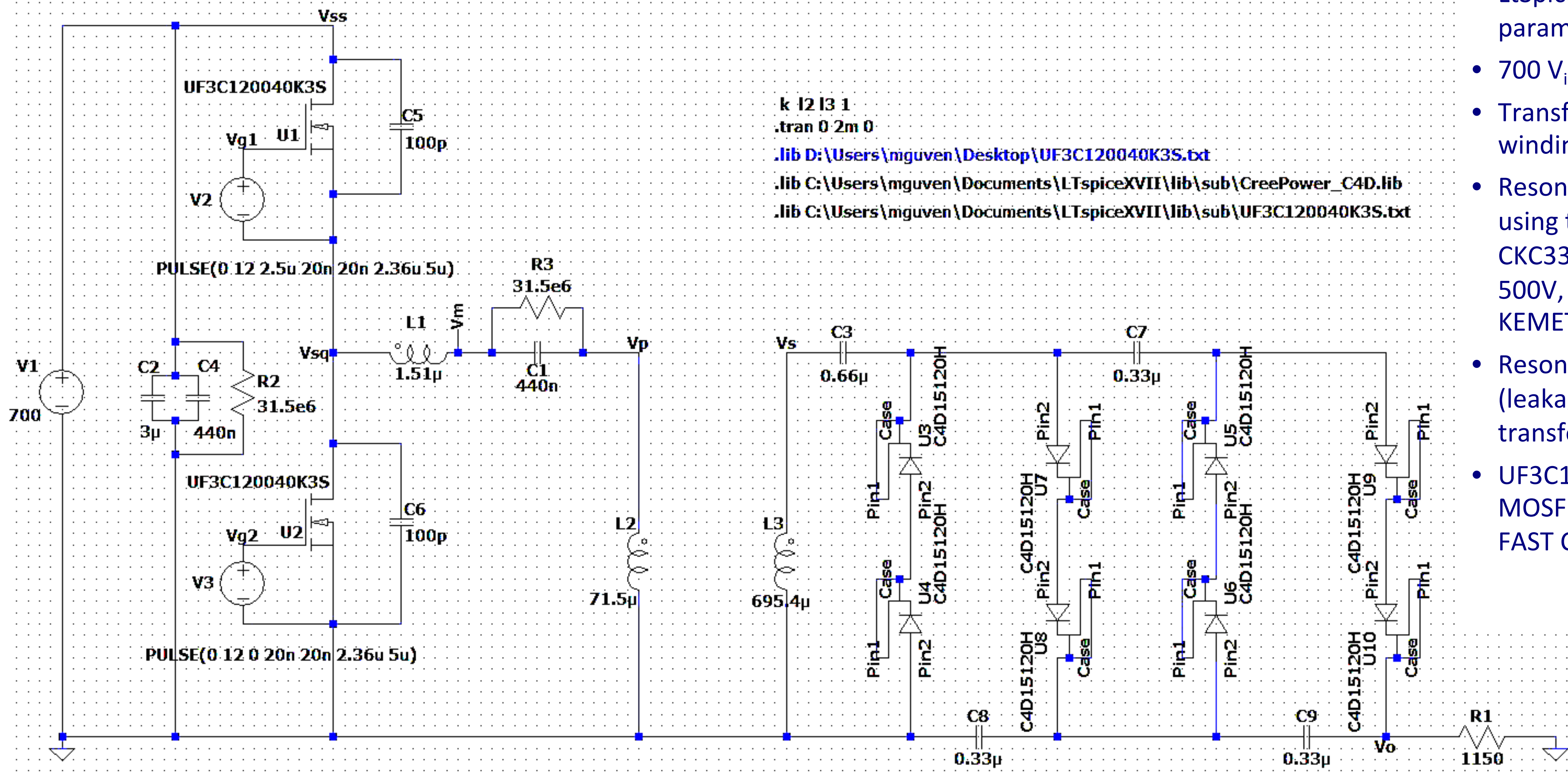
Designing Test Circuit of Resonant LLC Power Converter

- Resonant LLC Converter and Voltage Quadrupler Simulation with Component-Spice Model



- LtSpice simulation circuit parameter
- 700 V_{in}, 200 kHz
- Transformer ratio is 1:3, XFMR winding values (71.5:695 μH)
- Resonant cap value is 440nF using two serial CKC33C884KCGLC (880nF / 500V, 4-chip stack of 3640 KEMET MLCCs)
- Resonant tank inductance (leakage inductance of transformer) is 1.51 μH.
- UF3C120040K3S UnitedSiC MOSFET 1200V/40mOhm, SiC, FAST CASCODE, G3, TO-247-3L

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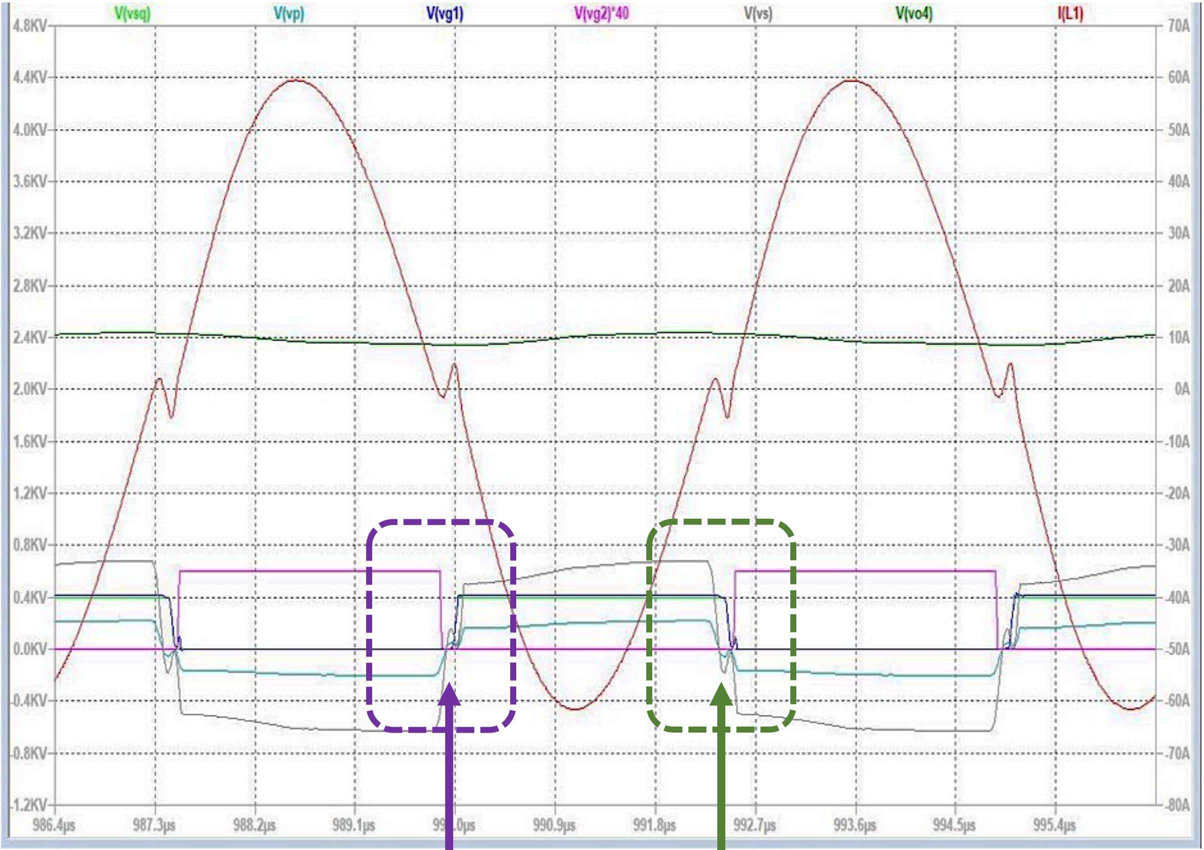
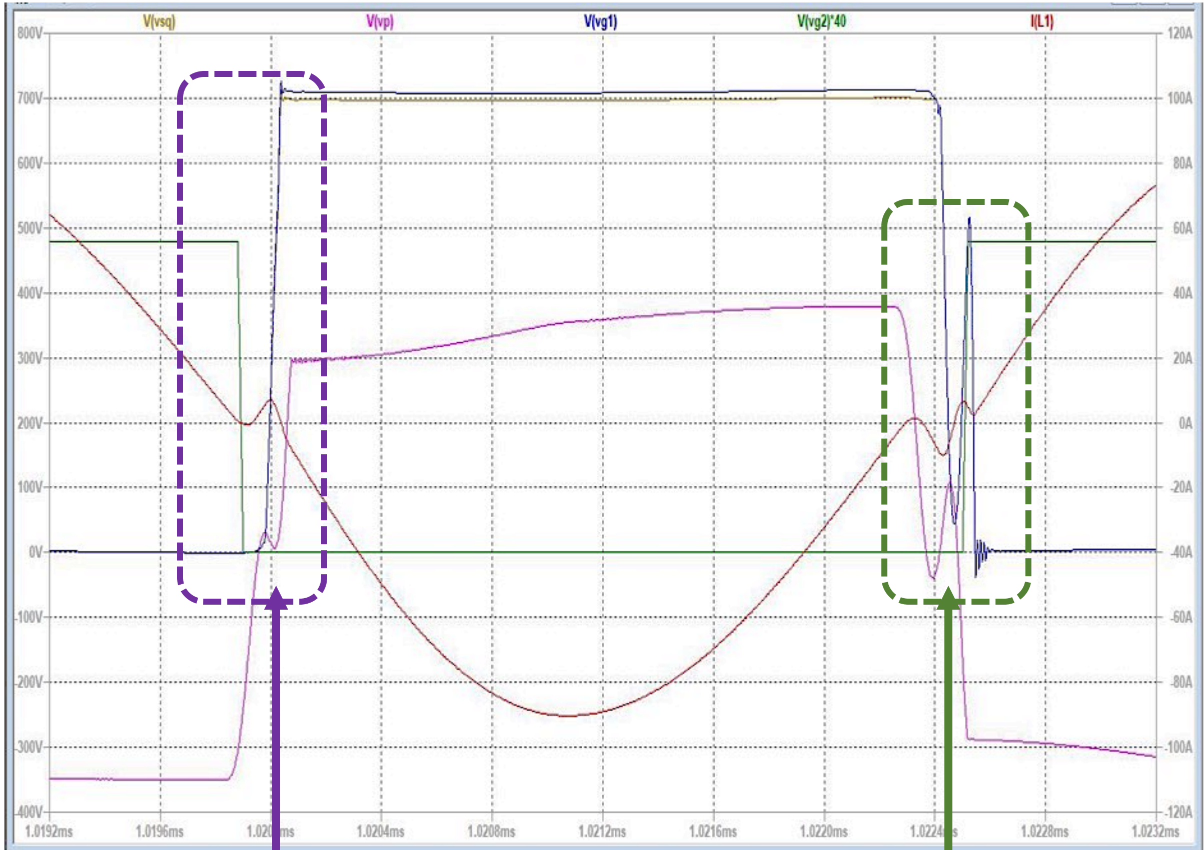
PREES Laboratory NC STATE UNIVERSITY PACKAGING RESEARCH IN ELECTRONIC ENERGY SYSTEMS

Simulation with Real-Spice Model for High Voltage Testing of Converter

Vin= 400 V @ f= 200 kHz



Vin= 700 V @ f= 200 kHz



High-side of the JFET turn-on

Low-side of the JFET turn-on

High-side of the JFET turn-on

Low-side of the JFET turn-on

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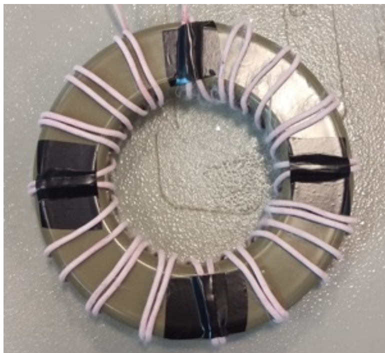
Design of Transformer (XFMR)

- $f_0 = \frac{1}{2\pi\sqrt{LC}}$ (Resonance frequency)

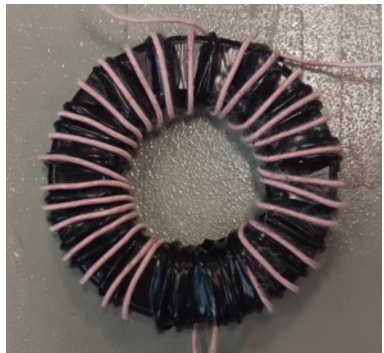
The transformer Design

- Turn ratio is designed 1:3, and the leakage inductance (resonance tank inductance) value is observed 1.51 μH at 200 kHz.
- Primary : Secondary inductance values are 71.5 : 695 μH.
- The leakage inductance decreases 1.28 μH at 220 kHz.

Leakage Inductance: Uncoupled magnetic flux on the secondary side, which is generated by primary side, is called 'Leakage Inductances'.



(a) 1st secondary layer winding



(b) Primary layer winding

(c) Final 1:3 ratio power transformer

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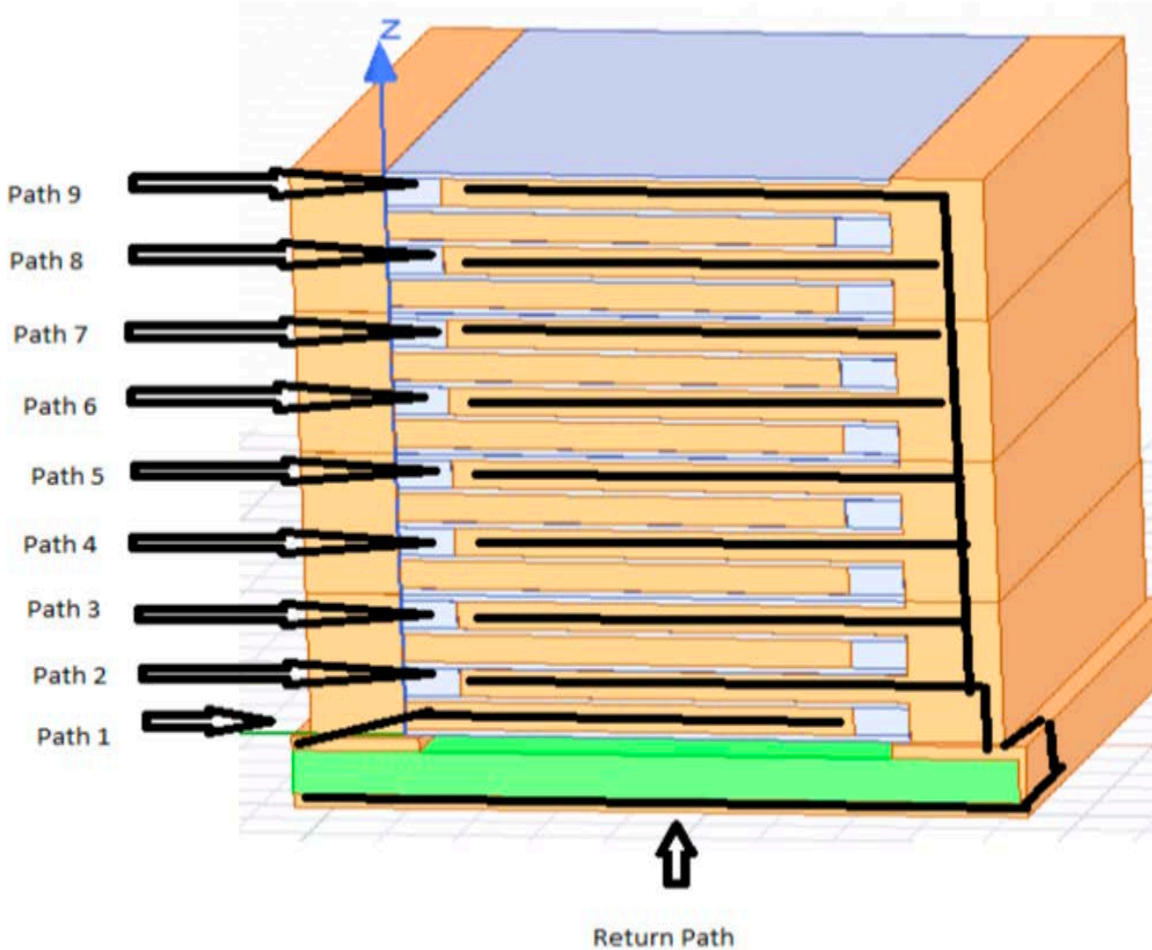
MLCCs Inductive loop investigation with Q3D Analysis (Sourish Sankar Sinha)



Ansys Q3D model of the 4 stack MLCCs

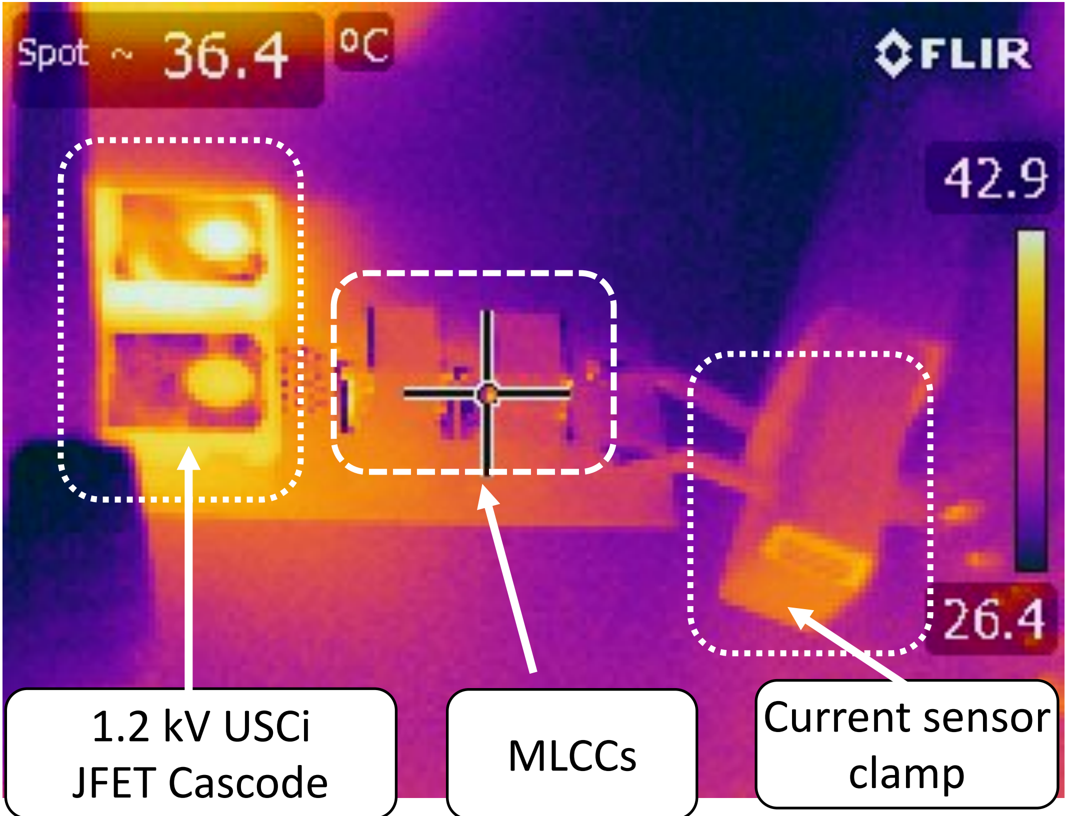
INDUCTANCE (nH)										
		Path 1	Path 2	Path 3	Path 4	Path 5	Path 6	Path 7	Path 8	Path 9
Geometry 1	1C	1.85	1.64	2.33	NA	NA	NA	NA	NA	NA
	2C	1.84	1.64	2.32	3.01	3.62	NA	NA	NA	NA
	3C	1.85	1.65	2.32	3.01	3.63	3.01	4.93	NA	NA
	4C	1.85	1.64	2.32	3.0	3.62	4.28	4.9	5.58	6.23

Resonant cap value is 440nF using two serial CKC33C884KCGLC (880nF / 500V, 4-chip stack of 3640 KEMET MLCCs)

Converter PCB Board and MLCC Configuration

440nF: Two serial
CKC33C884KCGLC
(880nF / 500V

400V - 1sec continuous testing



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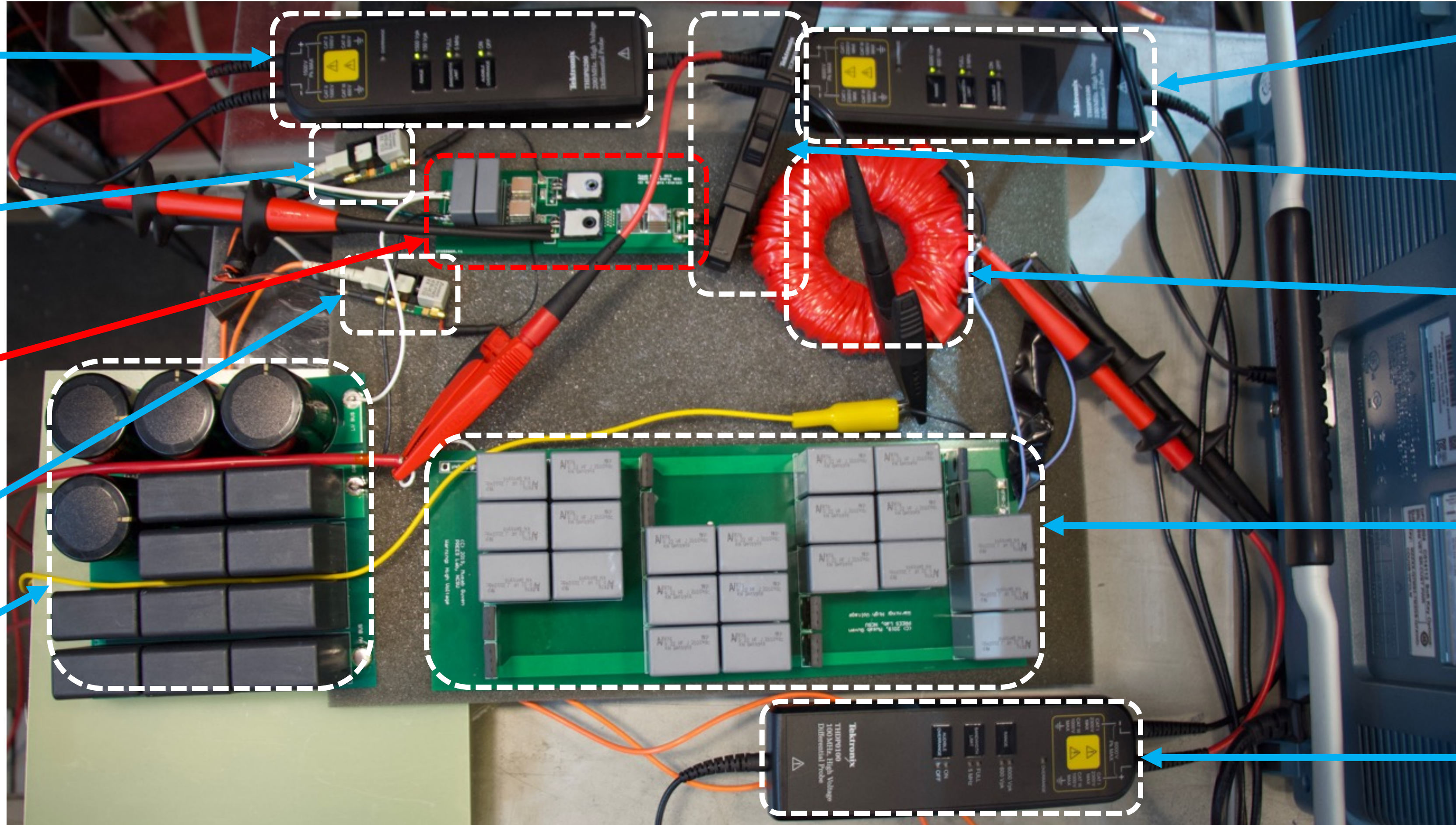
Converter Testing



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400V ZVS Pulse Test at 200 kHz

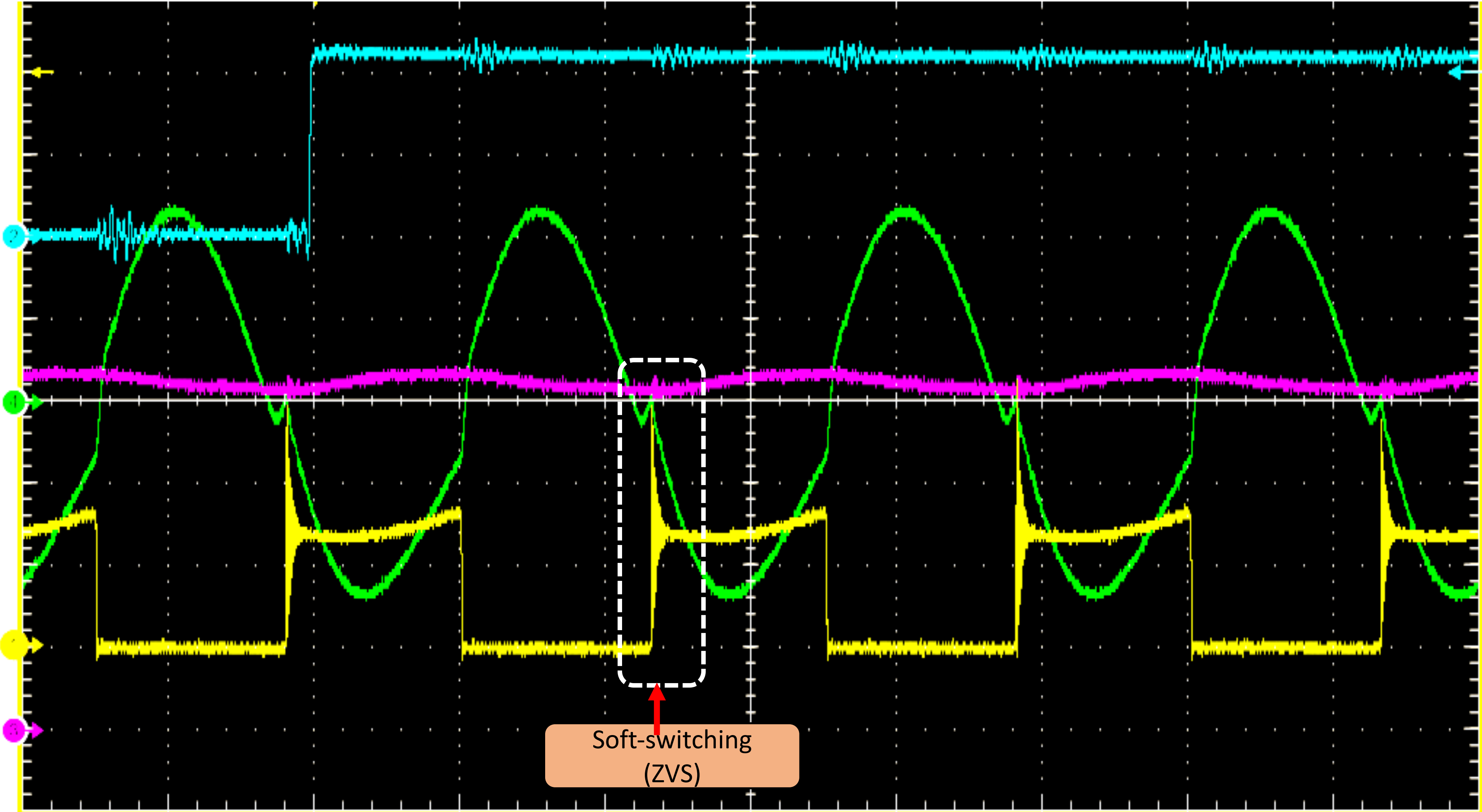
V_{in}= 400V
f= 200 kHz
t_{dead}= 80 ns

Channel 1
(Low-side D-S Voltage)
$V_{pk\text{-}pk}$= 600 V

Channel 4
(Resonant tank current)
I_{rms}= 33.94 A

Channel 2
(XFMR secondary side)
$V_s \cong$ 600 V (ideal)

Channel 3
(Output Voltage)
$V_s \cong$ 1.8 kV



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400V Hard-Switching Test at 200 kHz

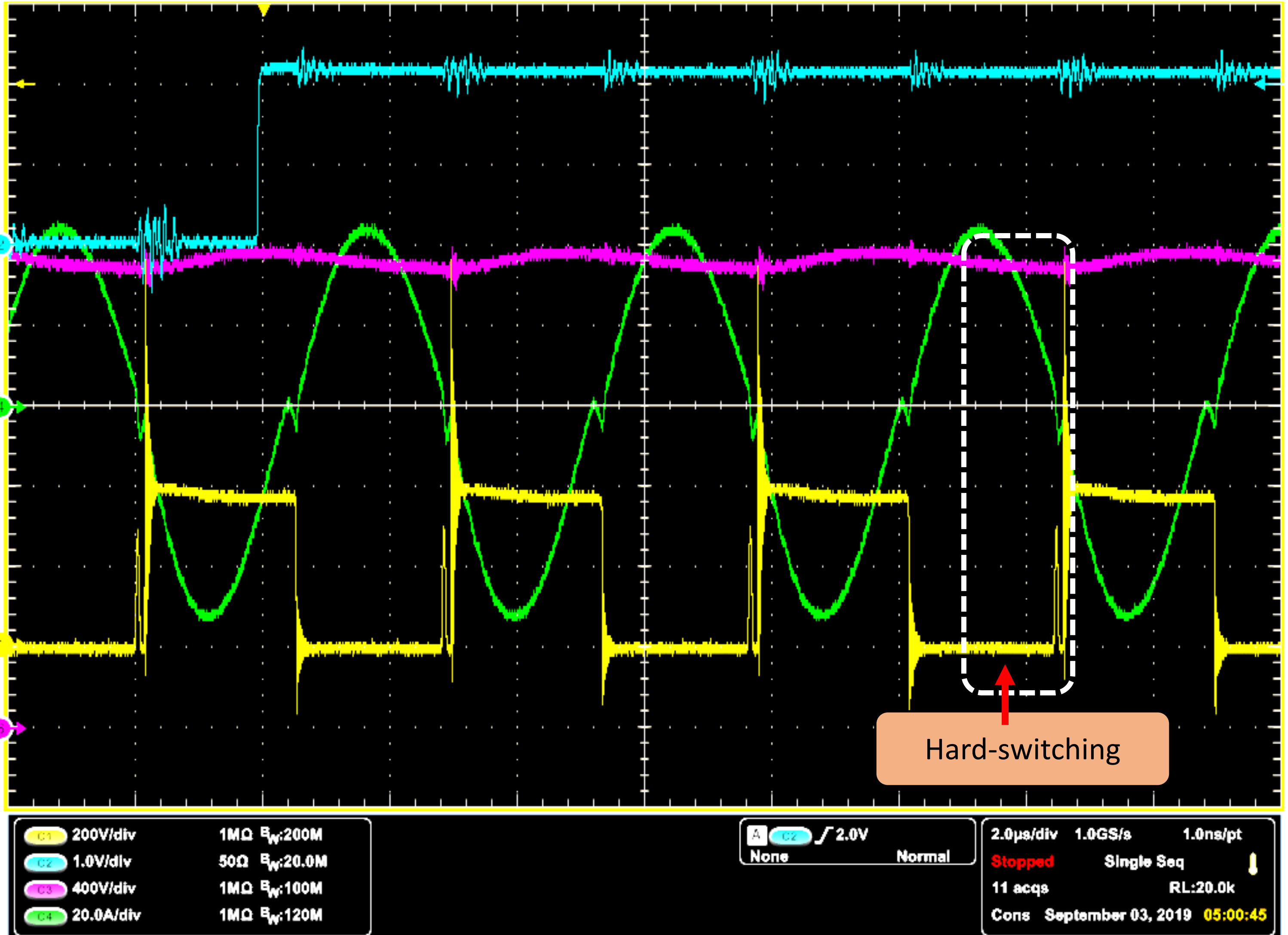
V_{in}= 400V
f= 200 kHz
t_{dead}= 120 ns

Channel 1
(Low-side D-S Voltage)
$V_{pk\text{-}pk}$= 1000 V

Channel 4
(Resonant tank current)
I_{rms}= 35.36 A

Channel 2
(XFMR secondary side)
$V_s \cong$ 600 V (ideal)

Channel 3
(Output Voltage)
$V_s \cong$ 1.7 kV



High Voltage testing of LLC resonant converter

- 400 V testing of converter efficiency is over 97%,
- 1 sec continuous testing at 400V is acceptable in terms of mechanical and thermal aspect,
- Thermal analysis of MLCCs shows relatively ambient temperature at continuous testing

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NC STATE UNIVERSITY

100 YEARS KEMET ESTABLISHED 1919

430 kVA Testing a 15nF 5S8P capacitor array (48nF) at 3.2kV$_{RMS}$/82A$_{RMS}$

Dr. Douglas C Hopkins & Dr. Wensong Yu

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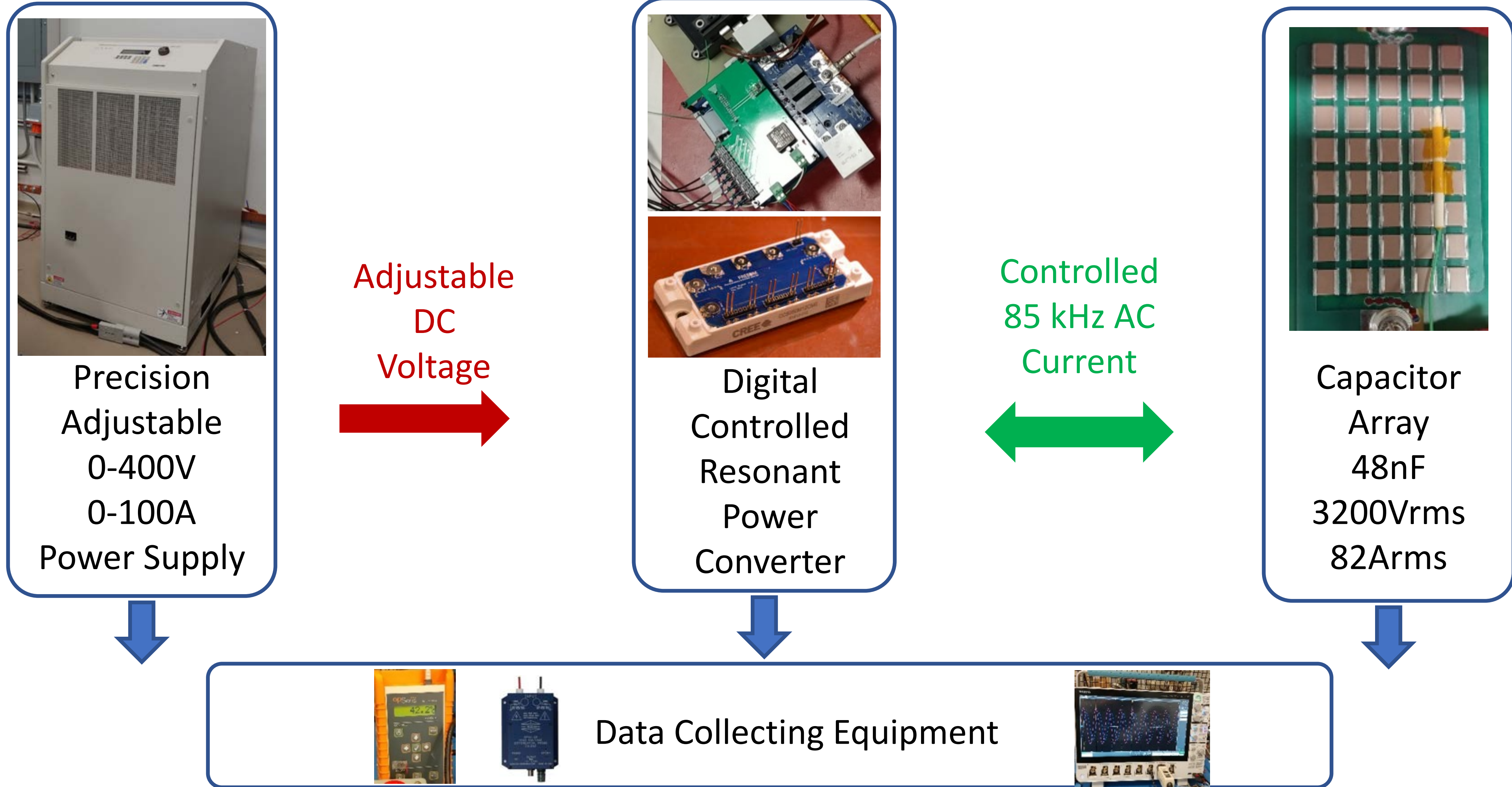
Test Method Using Resonant Power Recycling



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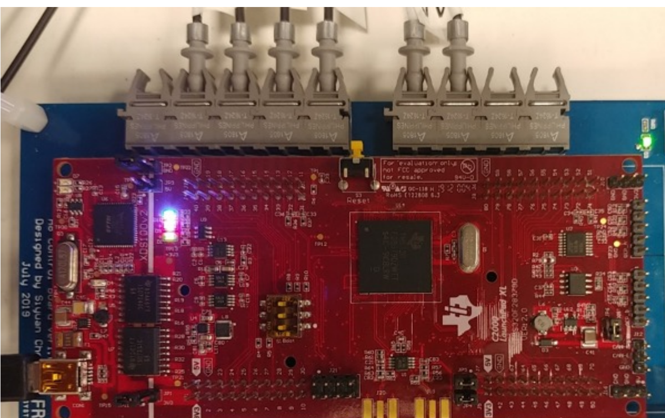
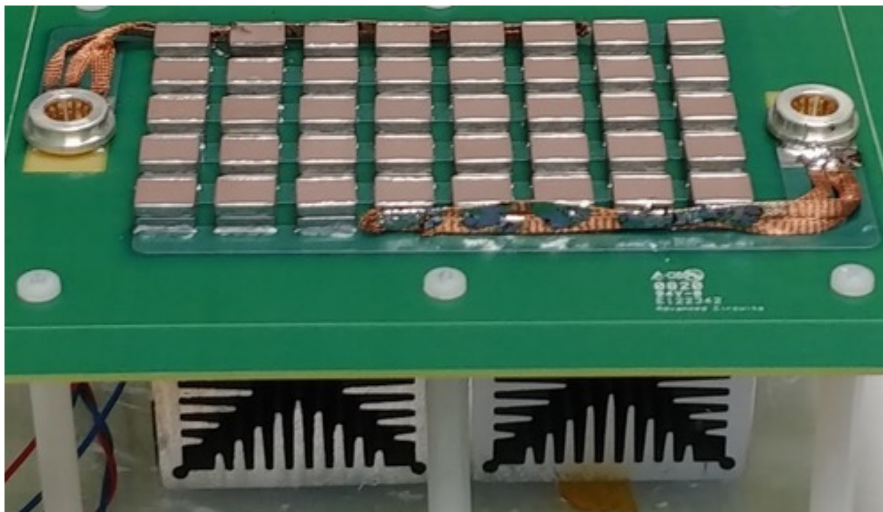
Resonant Converter Test System

Cree1.2 kV/150A SiC module


Fiber-optic digital controller


DUT Capacitor array with heatsink & fan

CIC Research, 1: 10,000

$20kV_{rms}$ HV differential V probe

Opsens Solutions, -40~250 ºC fiber optic temperature sensor

$20kV_{rms}$S HV isolated temperature probe

- Commercially available 1.2 kV SiC module (CCS050M12CM2, Cree) to realize high efficiency, while reducing the system cost
- Advanced digital controller (F28379D, Texas Instruments) integrated with fiber optic interface to achieve high resolution frequency adjustments and 20 kV isolation

C3640C153: DF < 0.1%, 15nF, 500V
3640 Pkg: 10.20 ±0.40 mm, 9.10 ±0.40 mm, 1.40 ± 0.15 mm

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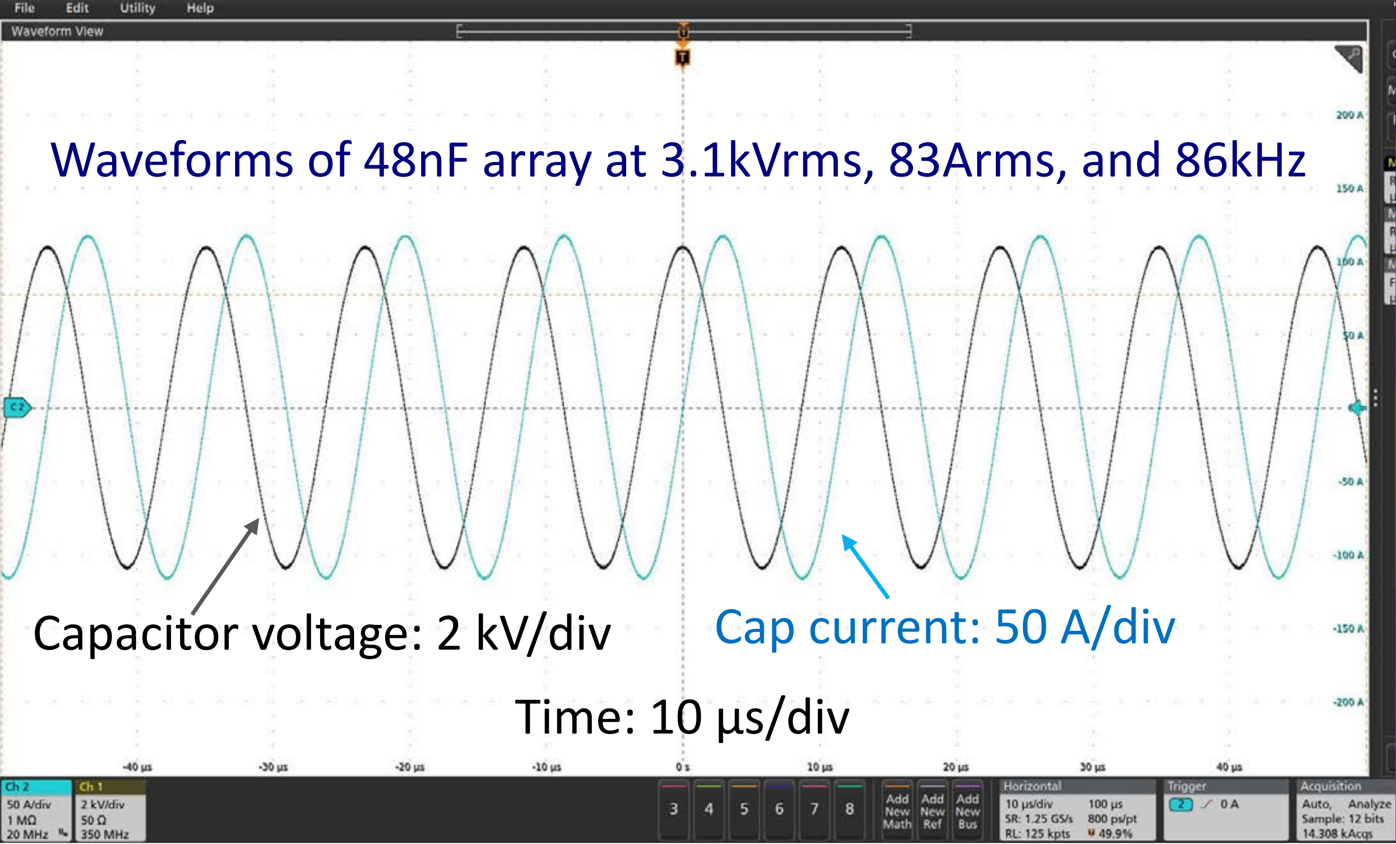
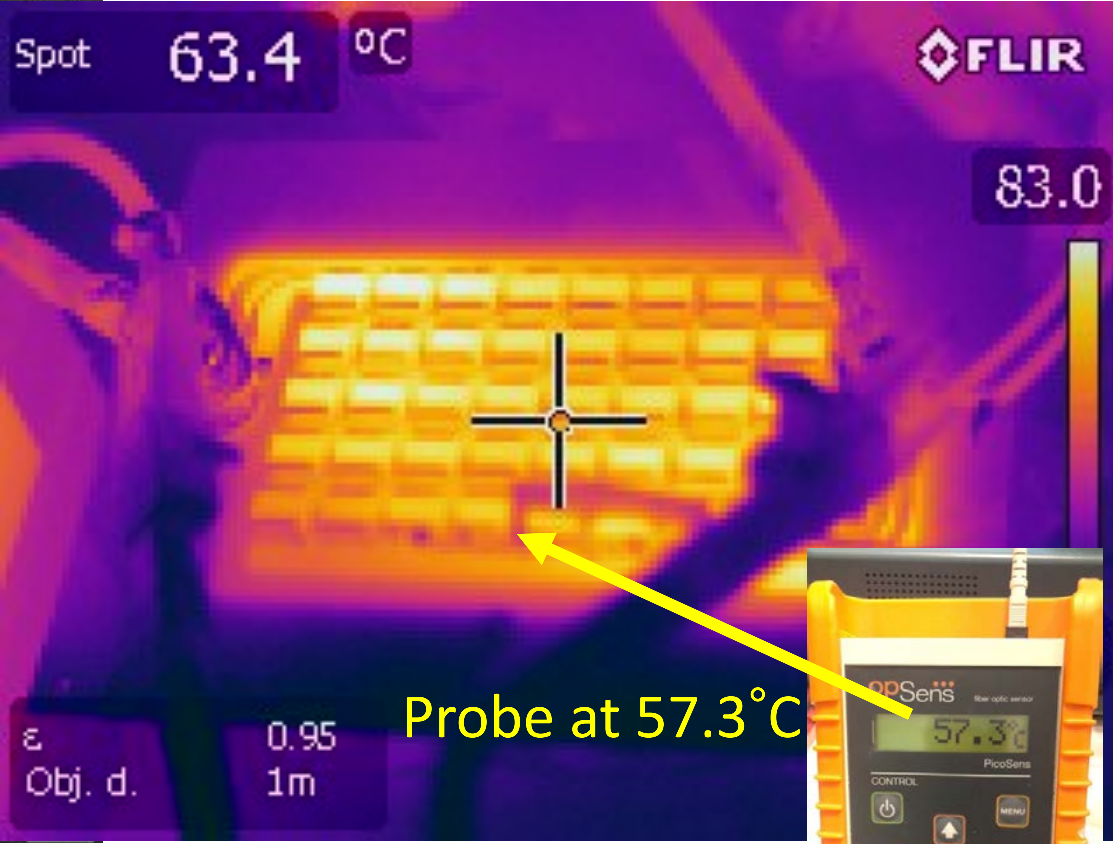
Testing Waveforms At 100% Rating

Temperature of 48nF array at 3.1kVrms, 83Arms, and 86kHz





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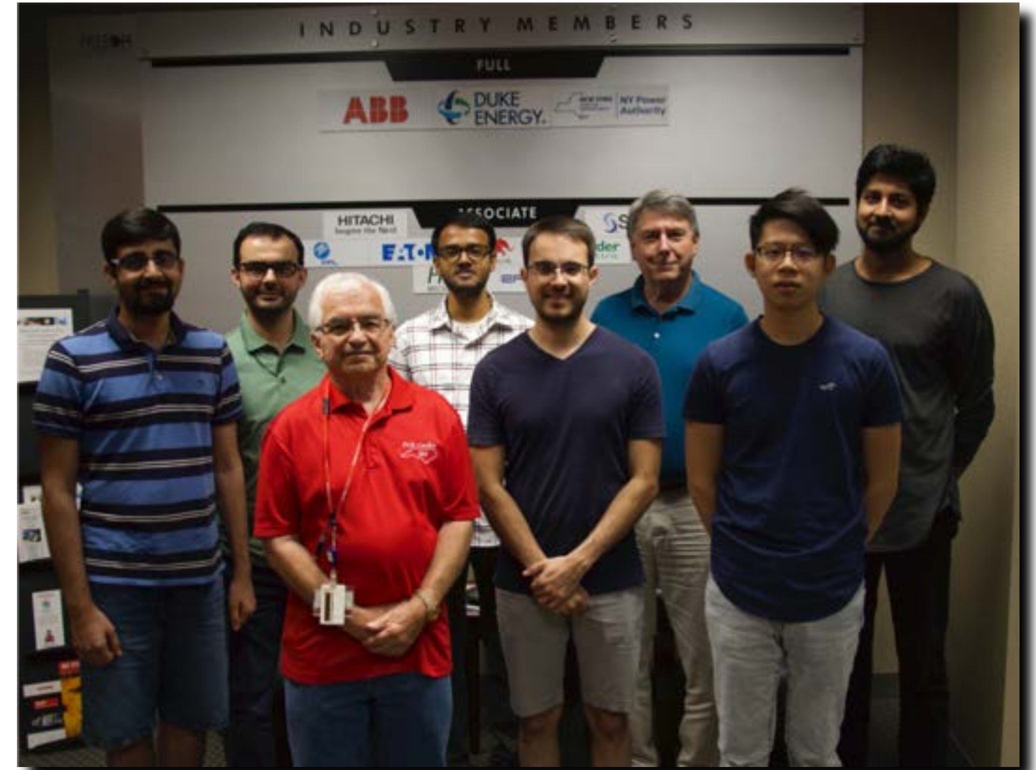

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